

Helping Customers Innovate, Improve & Grow




VX-705

## Description

The VX-705 is a Voltage Control Crystal Oscillator that operates at the fundamental frequency of the internal crystal. The crystal is a high-Q quartz device that enables the circuit to achieve low phase noise jitter performance over a wide operating temperature range. The VX-705 is housed in an industry standard hermetically sealed LCC package and is available in tape and reel.

## Features

- CMOS or LVPECL output VCXO
- Output Frequencies from 77.76 MHz to 170 MHz
- 3.3 V Operation
- Fundamental Crystal Design with Low Jitter Performance
- Output Disable Feature
- Excellent  $\pm 20$  ppm Temperature Stability,
- 0/70°C, -20/70°C or -40/85°C Operating Temperature
- Extended temperature range of -40/105°C available for LV-PECL
- Small Industry Standard Package, 5.0x7.0mm
- Product is free of lead and compliant to EC RoHS Directive 

## Applications

- LTE
- SONET/SDH/DWDM
- Ethernet, SyncE, GE
- xDSL, PCMA
- Digital Video
- Broadband Access
- Base Stations, Picocells
- Test and Measurement

## Block Diagram

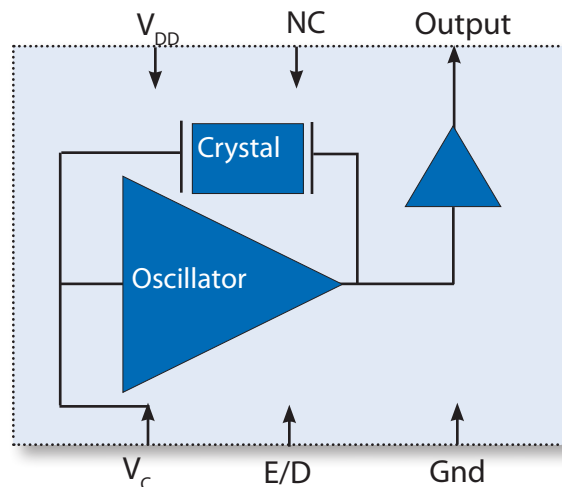


Figure 1. Block Diagram

# Performance Specifications

**Table 1. Electrical Performance - 3.3V CMOS**

Parameter	Symbol	Min	Typical	Max	Units
<b>Supply</b>					
Voltage <sup>1</sup>	$V_{DD}$	3.135	3.3	3.465	V
Current <sup>2</sup>	$I_{DD}$		10	25	mA
<b>Frequency</b>					
Nominal Frequency <sup>3</sup>	$f_N$	80.00		170.00	MHz
Absolute Pull Range <sup>2,6</sup> , <i>ordering option</i>	APR	$\pm 30$ or $\pm 50$			ppm
Linearity <sup>2</sup>	Lin		5		%
Gain Transfer <sup>2</sup>	$K_V$	+80			ppm/V
Temperature Stability	$f_{STAB}$		$\pm 20$		ppm
<b>Outputs</b>					
Output Logic Levels <sup>2</sup> Output Logic High Output Logic Low	$V_{OH}$ $V_{OL}$	$0.9 * V_{DD}$		$0.1 * V_{DD}$	V
Load	$I_{OUT}$			15	pF
Rise Time <sup>2,4</sup>	$t_R$			5	ns
Fall Time <sup>2,4</sup>	$t_F$			5	ns
Symmetry <sup>2</sup>	SYM	45	50	55	%
Jitter, RMS <sup>5,7</sup> (12kHz to 20 MHz)	$\phi_J$		80	200	fsec
Phase Noise <sup>8</sup> (122.88 MHz) 10Hz 100Hz 1kHz 10kHz 100kHz 1MHz 10MHz			-66 -98 -124 -138 -151 -158 -161		dBc/Hz
<b>Control Voltage</b>					
Control Voltage Range for Pull Range	$V_C$	0.3		3.0	V
Control Voltage Input Impedance	$Z_{IN}$	1			M $\Omega$
Control Voltage Modulation BW	BW	10			kHz
Output Enable/Disable <sup>9</sup> Output Enabled Output Disabled	$V_{IH}$ $V_{IL}$	$0.9 * V_{DD}$		$0.1 * V_{DD}$	V
Start-Up Time	$T_S$			10	ms
Operating Temp, Ordering Option	$T_{OP}$	0/70, -20/70 or -40/85			°C
Package Size		5.0 x 7.0 x 1.8			mm

- 1] The power supply should have by-pass capacitors as close to the supply and to ground as possible, for examples 0.1 and 0.01uF
- 2] Parameters are tested with production test circuit as shown in Figure 2.
- 3] See Standard Frequencies and Ordering Information tables for more specific information
- 4] Measured from 20% to 80% of a full output swing as shown in Figure 4.
- 5] Not tested in production, guaranteed by design, verified at qualification.
- 6] Tested with  $V_C = 0.3V$  to  $3.0V$  unless otherwise stated in part description
- 7] Broadband Period Jitter measured using Wavecrest SIA3300C, 90K samples.
- 8] Phase Noise is measured with an Agilent E5052A.
- 9] The Output is Enabled if the Enable/Disable is left open.

# Performance Specifications

**Table 2. Electrical Performance - 3.3V LVPECL**

Parameter	Symbol	Min	Typical	Max	Units
<b>Supply</b>					
Voltage <sup>1</sup>	$V_{DD}$	3.135	3.3	3.465	V
Current <sup>2</sup>	$I_{DD}$		50	90	mA
<b>Frequency</b>					
Nominal Frequency <sup>3</sup>	$f_N$	77.76		170.00	MHz
Absolute Pull Range <sup>2,6</sup> , <i>ordering option</i>	APR	$\pm 30, \pm 50$			ppm
Linearity <sup>2</sup>	Lin		5		%
Gain Transfer <sup>2</sup>	$K_V$	+80			ppm/V
Temperature Stability <sup>10</sup>	$f_{STAB}$		$\pm 20$		ppm
<b>Outputs</b>					
Output Logic Levels <sup>2</sup> Output Logic High Output Logic Low	$V_{OH}$ $V_{OL}$	$V_{DD} - 1.025$ $V_{DD} - 1.810$	$V_{DD} - 0.950$ $V_{DD} - 1.700$	$V_{DD} - 0.880$ $V_{DD} - 1.620$	V
Rise Time <sup>2,4</sup>	$t_R$		0.6	1	ns
Fall Time <sup>2,4</sup>	$t_F$		0.6	1	ns
Symmetry <sup>2</sup> Symmetry <sup>2</sup> (-40 °C to 105 °C)	SYM	45 40	50 50	55 60	% %
Jitter, RMS <sup>5,8</sup> (12kHz to 20 MHz)	$\phi_J$		0.3	1	ps
Jitter, RMS <sup>5,8</sup> (10kHz to 1MHz)	$\phi_J$		0.2	0.3	ps
Phase Noise <sup>8</sup> 10Hz 100Hz 1kHz 10kHz 100kHz 1MHz 10MHz			-60 -88 -118 -131 -145 -153 -156		dBc/Hz
<b>Control Voltage</b>					
Control Voltage Range for Pull Range	$V_C$	0.3		3.0	V
Control Voltage Input Impedance	$Z_{IN}$	1			M $\Omega$
Control Voltage Modulation BW	BW	10			kHz
Output Enable/Disable <sup>9</sup> Output Enabled, Option A Output Disabled, Option A	$V_{IH}$ $V_{IL}$	$0.9 * V_{DD}$		$0.1 * V_{DD}$	V
Start-Up Time	$T_S$			10	ms
Operating Temp, <i>Ordering Option</i>	$T_{OP}$	0/70, -20/70, -40/85 or -40/105			°C
Package Size		5.0 x 7.0 x 1.8			mm

1] The power supply should have by-pass capacitors as close to the supply and to ground as possible, for examples 0.1 and 0.01 $\mu$ F

2] Parameters are tested with production test circuit below as shown in Figure 3.

3] See Standard Frequencies and Ordering Information tables for more specific information

4] Measured from 20% to 80% of a full output swing as shown in Figure 4.

5] Not tested in production, guaranteed by design, verified at qualification.

6] Tested with  $V_C = 0V$  to 3.3V unless otherwise stated in part description

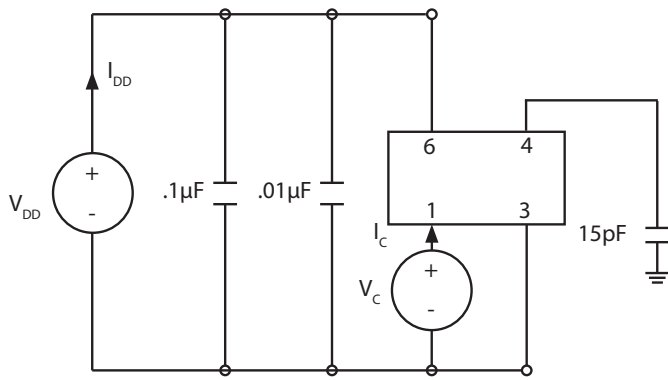
7] Broadband Period Jitter measured using Wavecrest SIA3300C, 90K samples.

8] Phase Noise is measured with an Agilent E5052A.

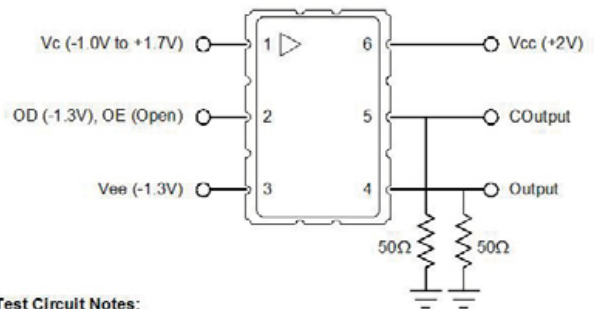
9] The Output is Enabled if the Enable/Disable is left open.

10]  $\pm 20$ ppm temperature stability is not available for -40 °C to 105 °C operating temperature range.

## Test Circuits



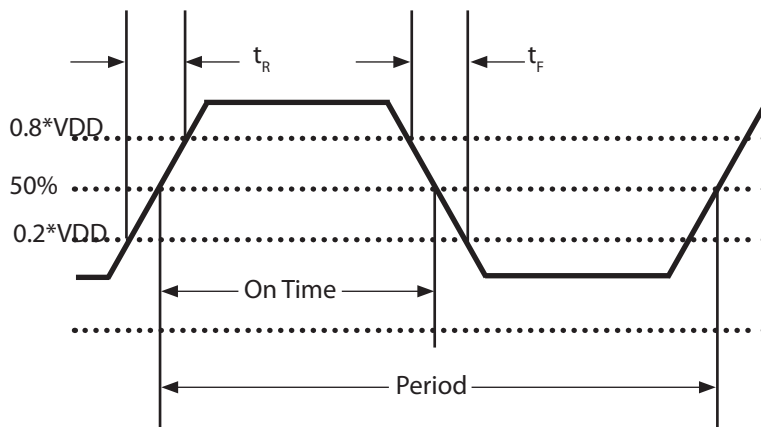
**Figure 2. CMOS Test Circuit**



**Test Circuit Notes:**  
 1) To Permit 50Ω Measurement of Outputs, all DC Inputs are Biased Down 1.3V.  
 2) All Voltage Sources Contain Bypass Capacitors to Minimize Supply Noise.  
 3) 50Ω Terminations are Within Test Equipment.

**Figure 3. LVPECL Test Circuit**

## Waveform



**Figure 4. Output Waveform**

**Table 3. Absolute Maximum Ratings**

Parameter	Symbol	Ratings	Unit
Power Supply	$V_{DD}$	0 to 6	V
Voltage Control Range	$V_C$	0 to $V_{CC}$	V
Storage Temperature	TS	-55 to 125	°C
Soldering Temp/Time	$T_{LS}$	260 / 20	°C / sec

Stresses in excess of the absolute maximum ratings can permanently damage the device. Functional operation is not implied at these or any other conditions in excess of conditions represented in the operational sections of this datasheet. Exposure to absolute maximum ratings for extended periods may adversely affect device reliability. Permanent damage is also possible if OD or Vc is applied before Vcc.

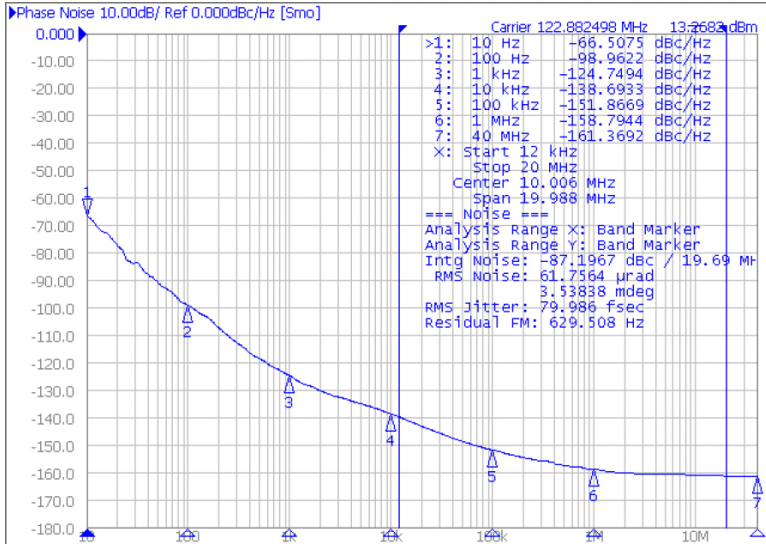


Figure 5A. Typical Phase Noise - 122.88 MHz CMOS

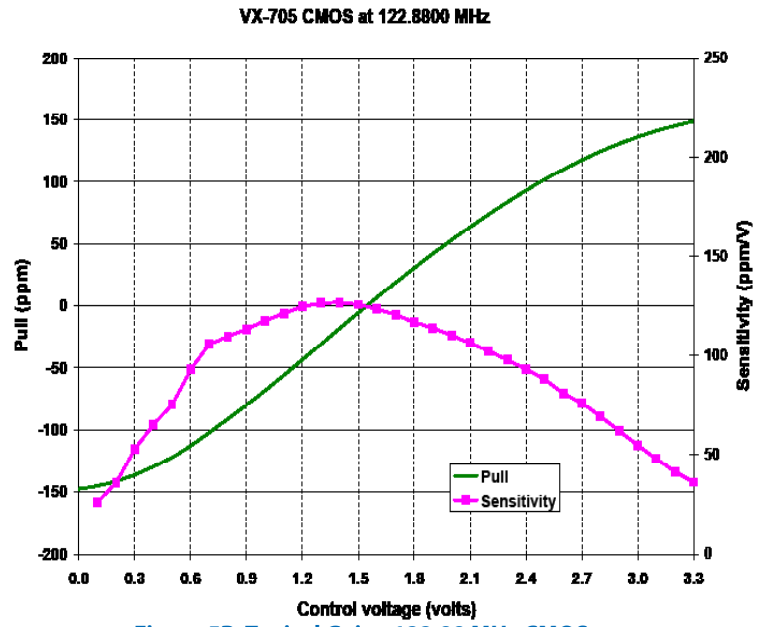


Figure 5B. Typical Gain - 122.88 MHz CMOS

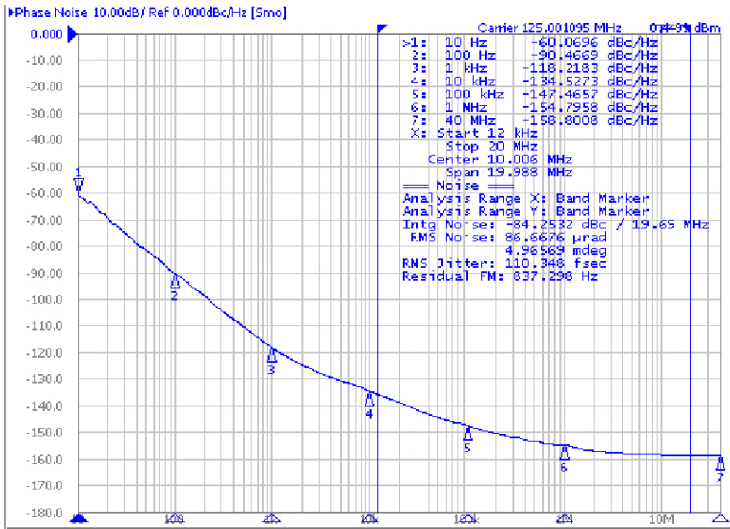


Figure 6A. Typical Phase Noise - 125.00 MHz PECL

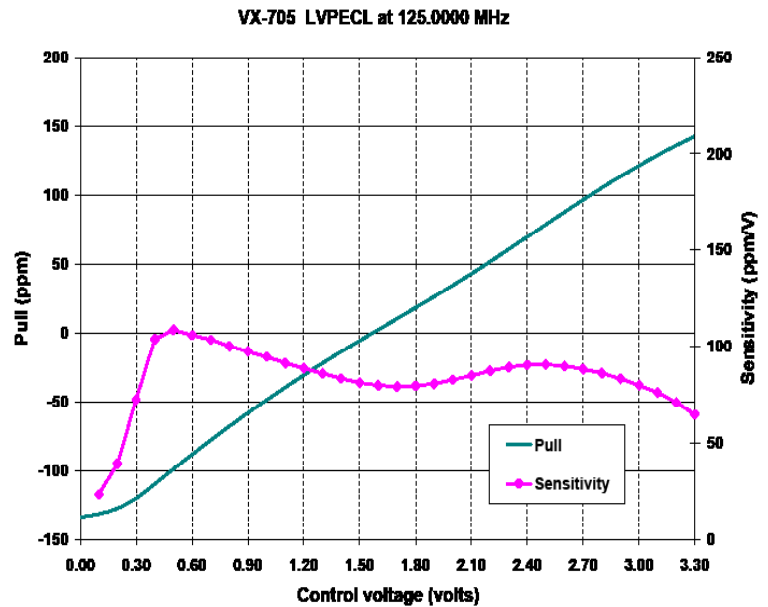


Figure 6B. Typical Gain - 125.00 MHz PECL

# Reliability

VI qualification includes aging at various extreme temperatures, shock and vibration, temperature cycling, and IR reflow simulation. The VX-705 family is capable of meeting the following qualification tests:

**Table 4. Environmental Compliance**

Parameter	Conditions
Mechanical Shock	MIL-STD-883, Method 2002
Mechanical Vibration	MIL-STD-883, Method 2007
Solderability	MIL-STD-883, Method 2003
Gross and Fine Leak	MIL-STD-883, Method 1014
Resistance to Solvents	MIL-STD-883, Method 2015
Moisture Sensitivity Level	MSL 1
Contact Pads	Gold over Nickel

# Handling Precautions

Although ESD protection circuitry has been designed into the VX-705 proper precautions should be taken when handling and mounting. VI employs a human body model (HBM) and a charged device model (CDM) for ESD susceptibility testing and design protection evaluation.

**Table 5. ESD Ratings**

Model	Minimum	Conditions
Human Body Model	500V	MIL-STD-883, Method 3015
Charged Device Model	500V	JESD22-C101

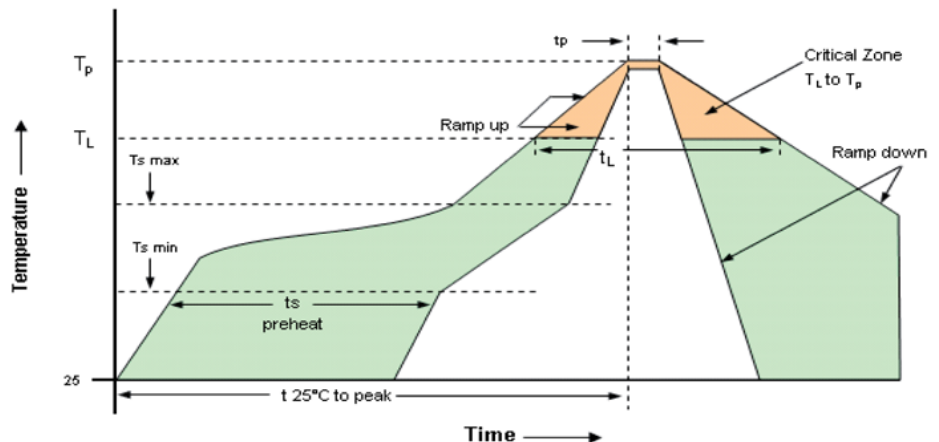
**Table 6. Reflow Profile**

Parameter	Symbol	Value
PreHeat Time Ts-min Ts-max	$t_s$	60 sec Min, 180 sec Max 150°C 200°C
Ramp Up	$R_{UP}$	3 °C/sec Max
Time Above 217 °C	$t_L$	60 sec Min, 150 sec Max
Time To Peak Temperature	$T_{AMB-P}$	480 sec Max

### Solderprofile:

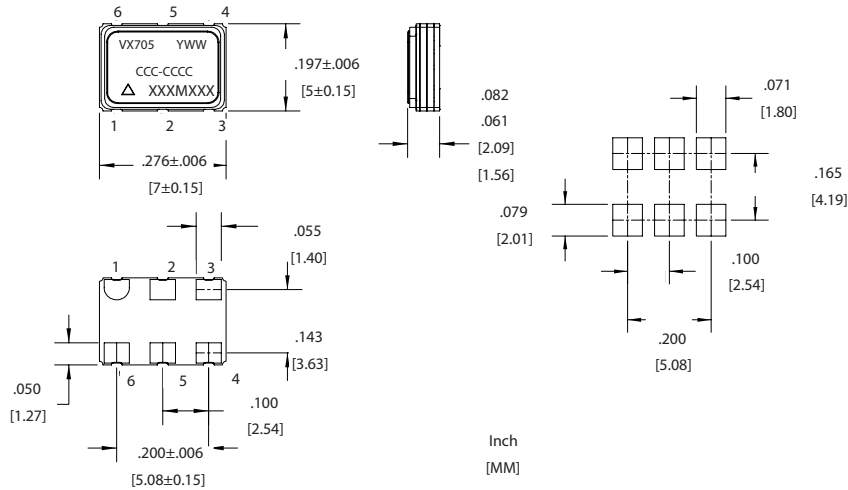
The device is qualified to meet the JEDEC standard for Pb-Free assembly. The temperatures and time intervals listed are based on the Pb-Free small body requirements. The VX-705 device is hermetically sealed so an aqueous wash is not an issue.

Termination Plating:  
Electroless Gold Plate over Nickel Plate



**Figure 7. Recommended Reflow Profile**

## Outline Drawing & Pad Layout



**Figure 8. Outline Drawing and Pad Layout**

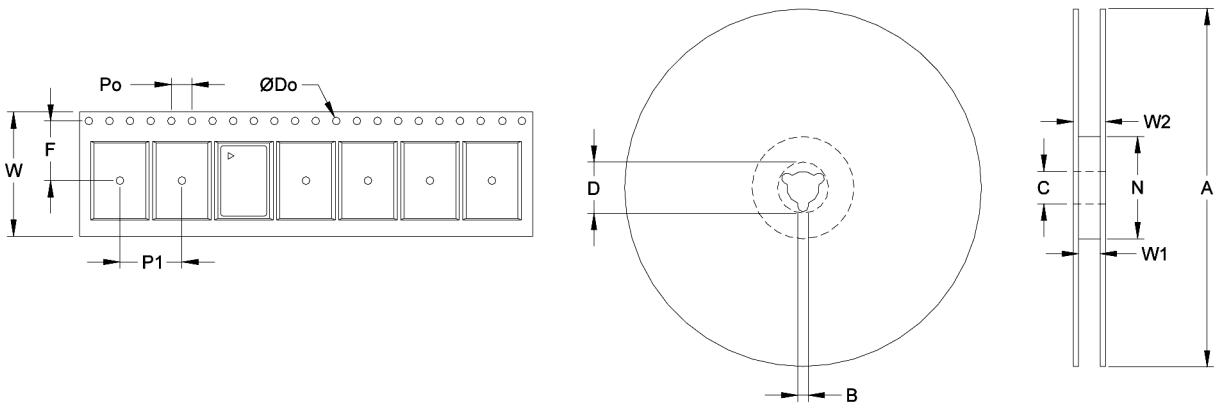
**Table 7a. Pin Out - 3.3V CMOS Option**

Pin	Symbol	Function
1	$V_C$	VCXO Control Voltage
2	E/D	Enable Disable ** See Ordering Options**
3	GND	Case and Electrical Ground
4	Output	Output
5	N/C	No Connect
6	$V_{DD}$	Power Supply Voltage

**Table 7b. Pin Out - 3.3V LVPECL Option**

Pin	Symbol	Function
1	$V_C$	VCXO Control Voltage
2	E/D	Enable Disable **See Ordering Options**
3	GND	Case and Electrical Ground
4	Output	Output
5	COutput	Complementary Output
6	$V_{DD}$	Power Supply Voltage

## Tape & Reel (EIA-481-2-A)



**Figure 9. Tape and Reel Drawing**

**Table 8. Tape and Reel Information**

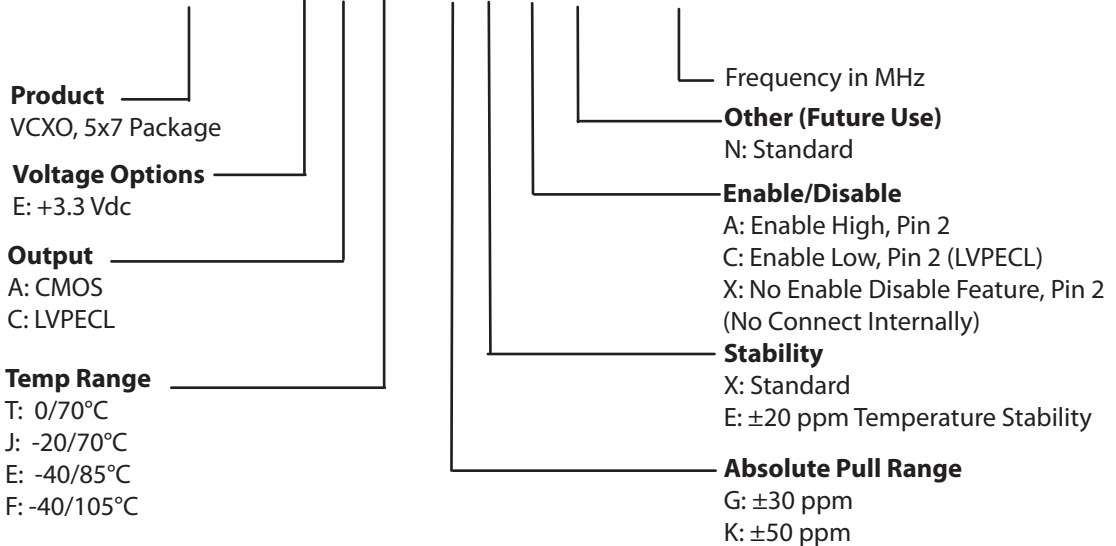
Dimension	Tape Dimensions (mm)					Reel Dimensions (mm)							# Per Reel
	W	F	Do	Po	P1	A	B	C	D	N	W1	W2	
Tolerance	Typ	Typ	Typ	Typ	Typ	Typ	Min	Typ	Min	Min	Typ	Max	
VX-705	16	5.5	1.5	4	8	178	1.78	13	20.6	55	12.4	22.4	500



Table 9. Standard Output Frequencies (MHz)							
89.60000	96.00000	100.00000	120.00000	122.88000	125.00000	127.79520	148.50000
153.60000	155.52000	156.25000	161.13280				

## Ordering Information

### VX-705- E A T - K X A N- 122M880000



**Example: VX-705-EAT-KXAN-122M880000**

*\*Note: not all combination of options are available. Other specifications may be available upon request. Consult with factory.*

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## Revision History

Revision Date	Approved	Description
January 21, 2015	VN	Included Extended temperature Range of -40/105°C for LV-PECL. Added revision history table.