

Applications

- Low voltage, high density systems with Intermediate Bus Architectures (IBA)
- Point-of-load regulators for high performance DSP, FPGA, ASIC, and microprocessors
- Desktops, servers, and portable computing
- Broadband, networking, optical, and communications systems

Benefits

- Integrates digital power conversion with intelligent power management
- Eliminates the need for external power management components
- Completely programmable via industry-standard I²C communication bus
- One part that covers all applications
- Reduces board space, system cost and complexity, and time to market

Description

Power-One's point-of-load converters are recommended for use with regulated bus converters in an Intermediate Bus Architecture (IBA). The ZY8110 is an intelligent, fully programmable multiphase step-down point-of-load DC-DC module integrating digital power conversion and intelligent power management. When used with ZM7000 Series Digital Power Managers, the ZY8110 completely eliminates the need for external components for sequencing, tracking, protection, monitoring, and reporting. All parameters of the ZY8110 are programmable via the industry-standard I²C communication bus and can be changed by a user at any time during product development and service.

Reference Documents:

- ZM7300 Digital Power Manager. Data Sheet
- ZM7300 Digital Power Manager. Programming Manual
- Z-One® Graphical User Interface
- ZM00056-KIT USB to I²C Adapter Kit. User Manual

Features

- RoHS lead free and lead-solder-exempt products are available
- Wide input voltage range: 8V–14V
- High continuous output current: 10A
- Programmable output voltage range: 0.5V–5.5V
- Efficiency greater than 92%
- Single-wire serial communication bus for frequency synchronization, programming, and monitoring
- Real time voltage, current, and temperature measurements, monitoring, and reporting
- Optimal voltage positioning with programmable slope of the VI line
- Overcurrent, overvoltage, undervoltage, and overtemperature protections with programmable thresholds and types
- Programmable fixed switching frequency 0.5-1.0MHz
- Programmable turn-on and turn-off delays
- Programmable turn-on and turn-off voltage slew rates with tracking protection
- Programmable feedback loop compensation
- Power Good signal with programmable limits
- Programmable fault management
- Start up into the load pre-biased up to 100%
- Current sink capability
- Industry standard size through-hole single-in-line package: 1.2"x0.26"
- Low height of 0.84"
- Wide operating temperature range: 0 to 70°C
- UL 60950-1/CSA 22.2 No. 60950-1-07 Second Edition, IEC 60950-1: 2005, and EN 60950-1:2006

1. Ordering Information

| ZY | 81 | 10 | y | - | zz |
|--|---|-------------------------------|--|-------------|--|
| Product family: Z-One Module | Series: Intelligent POL Converter | Output Current: 10A | RoHS compliance: No suffix - RoHS compliant with Pb solder exemption ¹ G - RoHS compliant for all six substances | Dash | Packaging Option²: R1 – 48 pcs Tray Q1 – 1 pc sample for evaluation only |

¹ The solder exemption refers to all the restricted materials except lead in solder. These materials are Cadmium (Cd), Hexavalent chromium (Cr6+), Mercury (Hg), Polybrominated biphenyls (PBB), Polybrominated diphenylethers (PBDE), and Lead (Pb) used anywhere except in solder.

² Packaging option is used only for ordering and not included in the part number printed on the POL converter label.

³ Z-One evaluation board is available in only one configuration: ZM7300-KIT-HKS.

Example: **ZY8110G-R1**: A 48-piece tray of RoHS compliant POL converters. Each POL converter is labeled ZY8110G.

2. Absolute Maximum Ratings

Stresses in excess of the absolute maximum ratings may cause performance degradation, adversely affect long-term reliability, and cause permanent damage to the converter.

| Parameter | Conditions/Description | Min | Max | Units |
|-----------------------|-----------------------------|-----|-----|-------|
| Operating Temperature | Controller case temperature | 0 | 105 | °C |
| Input Voltage | 250ms Transient | | 15 | VDC |

3. Environmental and Mechanical Specifications

| Parameter | Conditions/Description | Min | Nom | Max | Units |
|---|--|--------------------|-----|-----|------------------------------|
| Ambient Temperature Range | | 0 | | 70 | °C |
| Storage Temperature (Ts) | | -55 | | 125 | °C |
| Weight | | | | 6 | grams |
| Operating Vibration (sinusoidal) | Frequency Range Magnitude Sweep Rate Repetitions in each axis (Min-Max-Min Sweep) | 5 0.5 1 2 | | 500 | Hz G oct/min sweeps |
| Non-Operating Shock (half sine) | Acceleration Duration Number of shocks in each axis | 50 11 10 | | | G ms |
| MTBF | Calculated Per Telcordia Technologies SR-332 | 42.6 | | | MHrs |
| Peak Reflow Temperature | ZY8110 | | | 220 | °C |
| Peak Reflow Temperature | ZY8110G | | 245 | 260 | °C |
| Lead Plating | ZY8110 and ZY8110G | 100% Matte Tin | | | |
| Moisture Sensitivity Level per JEDEC J-STD-020C | ZY8110 ZY8110G | 2 3 | | | |

4. Electrical Specifications

Specifications apply at the input voltage from 8V to 14V, output load from 0 to 10A, ambient temperature from 0°C to 70°C, output capacitance consisting of 3x22μF low ESR ceramic, and default performance parameters settings unless otherwise noted.

4.1 Input Specifications

| Parameter | Conditions/Description | Min | Nom | Max | Units |
|----------------------------|------------------------|-----|-----|-----|-------|
| Input voltage (V_{IN}) | | 8 | | 14 | VDC |
| Input Current (at no load) | $V_{IN}=12V$ | | 31 | | mADC |

4.2 Output Specifications

| Parameter | Conditions/Description | Min | Nom | Max | Units |
|--|---|--|--|-------|--------------------------------------|
| Output Voltage Range (V_{OUT}) | Programmable ¹ Default (no programming) | 0.5 | 0.5 | 5.5 | VDC VDC |
| Output Voltage Setpoint Accuracy | $V_{IN}=12V$, $I_{OUT}=0.5 \cdot I_{OUT\ MAX}$, $F_{SW}=500kHz$, room temperature | $\pm 1.5\%$ or 10mV whichever is greater | | | $\%V_{O\ SET}$ |
| Output Current (I_{OUT}) | $V_{IN\ MIN}$ to $V_{IN\ MAX}$ | -10 ² | | 10 | ADC |
| Line Regulation | $V_{IN\ MIN}$ to $V_{IN\ MAX}$ | | ± 0.5 | | $\%V_{OUT}$ |
| Load Regulation | 0 to $I_{OUT\ MAX}$ | | ± 0.5 | | $\%V_{OUT}$ |
| Dynamic Regulation Peak Deviation Settling Time | 50 - 100% load step, Slew rate 2.5A/μs $C_{OUT}=110\mu F$, $F_{SW}=1MHz$ to 10% of peak deviation | | 170 40 | | mV μs |
| Output Voltage Peak-to-Peak Ripple and Noise BW=20MHz Full Load | $V_{IN}=12V$, $V_{OUT}\leq 1.0V$ $V_{IN}=12V$, $V_{OUT}=2.5V$ $V_{IN}=12V$, $V_{OUT}=5.0V$ | | 20 25 30 | | mV mV mV |
| Efficiency $V_{IN}=12V$ $F_{SW}=500kHz$ Full Load Room temperature | $V_{OUT}=0.5V$ $V_{OUT}=0.75V$ $V_{OUT}=1.0V$ $V_{OUT}=1.2V$ $V_{OUT}=1.8V$ $V_{OUT}=2.5V$ $V_{OUT}=3.3V$ $V_{OUT}=5.0V$ | | 64.2 71.6 76.2 78.8 83.8 86.7 88.8 91.6 | | % % % % % % % % |
| Temperature Coefficient | $V_{IN}=12V$, $V_{OUT}=2.5V$, $I_{OUT}=0.5 \cdot I_{OUT\ MAX}$ | | 20 | | ppm/°C |
| Switching Frequency | Default Programmable, 250kHz steps | 500 | 500 | 1,000 | kHz kHz |
| Duty Cycle | Default Programmable, 0.5% steps | 0 | 90.5 | 95 | % % |

¹ ZY8110 is a step-down converter, thus the output voltage is always lower than the input voltage.

² At the negative output current (bus terminator mode) efficiency of the ZY8110 degrades resulting in increased internal power dissipation. Therefore maximum allowable negative current under specific conditions is 20% lower than the current determined from the derating curves shown in paragraph 5.5.

4.3 Protection Specifications

| Parameter | Conditions/Description | Min | Nom | Max | Units |
|---|---|---|-----|------|--|
| Output Overcurrent Protection | | | | | |
| Type | Default Programmable | Non-Latching, 130ms period Latching/Non-Latching | | | |
| Threshold | Default Programmable in 11 steps | 40 | 140 | 140 | %I _{OUT} %I _{OUT} |
| Threshold Accuracy | | -25 | | 25 | %I _{OCP.SET} |
| Output Overvoltage Protection | | | | | |
| Type | Default Programmable | Non-Latching, 130ms period Latching/Non-Latching | | | |
| Threshold | Default Programmable in 10% steps | 110 ¹ | 130 | 130 | %V _{O.SET} %V _{O.SET} |
| Threshold Accuracy | Measured at V _{O.SET} =2.5V | -2 | | 2 | %V _{OVP.SET} |
| Delay | From instant when threshold is exceeded until the turn-off command is generated | | 6 | | μs |
| Output Undervoltage Protection | | | | | |
| Type | Default Programmable | Non-Latching, 130ms period Latching/Non-Latching | | | |
| Threshold | Default Programmable in 5% steps | 75 | 75 | 90 | %V _{O.SET} %V _{O.SET} |
| Threshold Accuracy | Measured at V _{O.SET} =2.5V | -2 | | 2 | %V _{UVP.SET} |
| Delay | From instant when threshold is exceeded until the turn-off command is generated | | 6 | | μs |
| Overtemperature Protection | | | | | |
| Type | Default Programmable | Non-Latching, 130ms period Latching/Non-Latching | | | |
| Turn Off Threshold | Temperature is increasing | | 120 | | °C |
| Turn On Threshold | Temperature is decreasing after the module was shut down by OTP | | 110 | | °C |
| Threshold Accuracy | | -5 | | 5 | °C |
| Delay | From instant when the controller junction temperature reaches the OTP threshold until the turn-off command is generated | | 2 | | ms |
| Tracking Protection (when Enabled) | | | | | |
| Type | Default Programmable | Disabled Latching/Non-Latching, 130ms period | | | |
| Threshold | Enabled during output voltage ramping up | | | ±250 | mVDC |
| Threshold Accuracy | | -50 | | 50 | mVDC |
| Delay | From instant when threshold is exceeded until the turn-off command is generated | | 6 | | μs |

| Overtemperature Warning | | | | | |
|-------------------------------|---|----|-------------|----|--|
| Threshold | Always enabled, reported in Status register | | 120 | | °C |
| Threshold Accuracy | | -5 | | 5 | °C |
| Hysteresis | | | 3 | | °C |
| Delay | From instant when threshold is exceeded until the warning signal is generated | | 6 | | µs |
| Power Good Signal (PGOOD pin) | | | | | |
| Logic | V _{OUT} is inside the PG window V _{OUT} is outside the PG window | | High Low | | N/A |
| Lower Threshold | Default Programmable in 5% steps | 90 | 90 | 95 | %V _{O.SET} %V _{O.SET} |
| Upper Threshold | | | 110 | | %V _{O.SET} |
| Delay | From instant when threshold is exceeded until status of PG signal changes | | 6 | | µs |
| Threshold Accuracy | Measured at V _{O.SET} =2.5V | -2 | | 2 | %V _{O.SET} |

¹ Minimum OVP threshold is 1.0V

4.4 Feature Specifications

| Parameter | Conditions/Description | Min | Nom | Max | Units |
|---|---|------|------|--------------------|------------------|
| Interleave | | | | | |
| Interleave (Phase Shift) | Default Programmable in 11.25° steps | 0 | 0 | 348.75 | Degree degree |
| Sequencing | | | | | |
| Turn ON Delay | Default Programmable in 1ms steps | 0 | 0 | 255 | ms ms |
| Turn OFF Delay | Default Programmable in 1ms steps | 0 | 0 | 63 | ms ms |
| Tracking | | | | | |
| Turn ON Slew Rate | Default Programmable in 7 steps | 0.1 | 0.1 | 8.33 ¹ | V/ms V/ms |
| Turn OFF Slew Rate | Default Programmable in 7 steps | -0.1 | -0.1 | -8.33 ¹ | V/ms V/ms |
| Optimal Voltage Positioning | | | | | |
| Load Regulation | Default Programmable in 7 steps | 0 | 0 | 13.2 | mV/A mV/A |
| Feedback Loop Compensation | | | | | |
| Zero1 (Effects phase lead and increases gain in mid-band) | Programmable | 0.05 | | 50 | kHz |
| Zero 2 (Effects phase lead and increases gain in mid-band) | Programmable | 0.05 | | 50 | kHz |
| Pole 1 (Integrator Pole, effects loop gain) | Programmable | 0.05 | | 50 | kHz |
| Pole 2 (Effects phase lag and limits gain in mid-band) | Programmable | 1 | | 1000 | kHz |
| Pole 3 (High frequency low- pass filter to limit PWM noise) | Programmable | 1 | | 1000 | kHz |

| Monitoring | | | | | |
|---------------------------------|--|--------------------------------|--|-------------------------------|-------------------|
| Voltage Monitoring Accuracy | 1 LSB=22mV | -1%V _{OUT} - 1 LSB | | 1%V _{OUT} + 1 LSB | mV |
| Current Monitoring Accuracy | 30% I _{OUT NOM} < I _{OUT} ≤ I _{OUT NOM} | -20 | | +20 | %I _{OUT} |
| Temperature Monitoring Accuracy | Junction temperature of POL controller | -5 | | +5 | °C |

¹ Achieving fast slew rates under specific line and load conditions may require feedback loop adjustment

4.5 Signal Specifications

| Parameter | Conditions/Description | Min | Nom | Max | Units |
|----------------------------------|---|------------|-----|------------|------------------|
| VDD | Internal supply voltage | 3.15 | 3.3 | 3.45 | V |
| SYNC/DATA Line (SD pin) | | | | | |
| ViL_sd | LOW level input voltage | -0.5 | | 0.3 x VDD | V |
| ViH_sd | HIGH level input voltage | 0.75 x VDD | | VDD + 0.5 | V |
| Vhyst_sd | Hysteresis of input Schmitt trigger | 0.25 x VDD | | 0.45 x VDD | V |
| VoL | LOW level sink current @ 0.5V | 14 | | 60 | mA |
| Tr_sd | Maximum allowed rise time 10/90%VDD | | | 300 | ns |
| Cnode_sd | Added node capacitance | | 5 | 10 | pF |
| Ipu_sd | Pull-up current source at Vsd=0V | 0.3 | | 1.0 | mA |
| Freq_sd | Clock frequency of external SD line | 475 | | 525 | kHz |
| Tsynq | Sync pulse duration | 22 | | 28 | % of clock cycle |
| T0 | Data=0 pulse duration | 72 | | 78 | % of clock cycle |
| ADDR0...ADDR4 Inputs | | | | | |
| ViL_x | LOW level input voltage | -0.5 | | 0.3 x VDD | V |
| ViH_x | HIGH level input voltage | 0.7 x VDD | | VDD+0.5 | V |
| Vhyst_x | Hysteresis of input Schmitt trigger | 0.1 x VDD | | 0.3 x VDD | V |
| RdnL_ADDR | External pull down resistance ADDRX forced low | | | 10 | kOhm |
| Power Good and OK Inputs/Outputs | | | | | |
| Iup_PG | Pull-up current source input forced low PG | 25 | | 110 | μA |
| Iup_OK | Pull-up current source input forced low OK | 175 | | 725 | μA |
| ViL_x | LOW level input voltage | -0.5 | | 0.3 x VDD | V |
| ViH_x | HIGH level input voltage | 0.7 x VDD | | VDD+0.5 | V |
| Vhyst_x | Hysteresis of input Schmitt trigger | 0.1 x VDD | | 0.3 x VDD | V |
| IoL | LOW level sink current at 0.5V | 4 | | 20 | mA |

5. Typical Performance Characteristics

5.1 Efficiency Curves

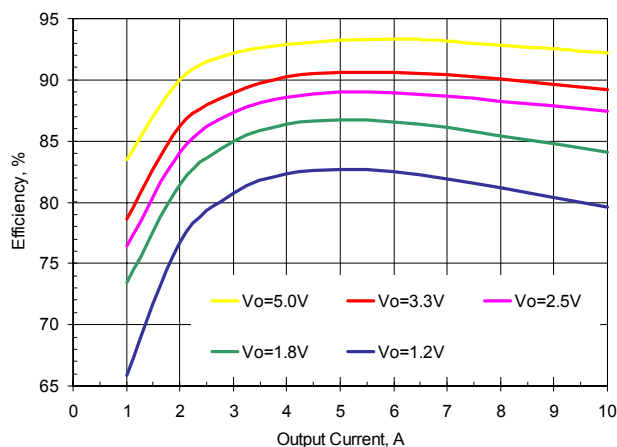


Figure 1. Efficiency vs. Load. Vin=9.6V, Fsw=500kHz

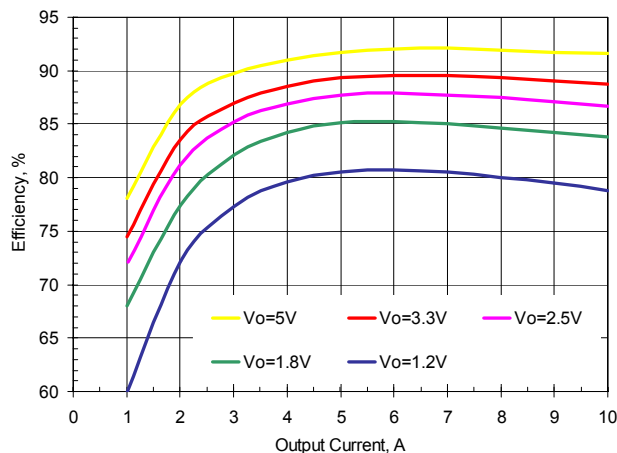


Figure 2. Efficiency vs. Load. Vin=12V, Fsw=500kHz

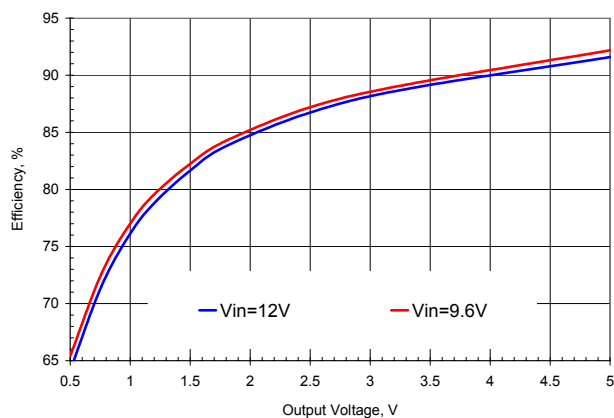


Figure 3. Efficiency vs. Output Voltage, Iout=10A, Fsw=500kHz

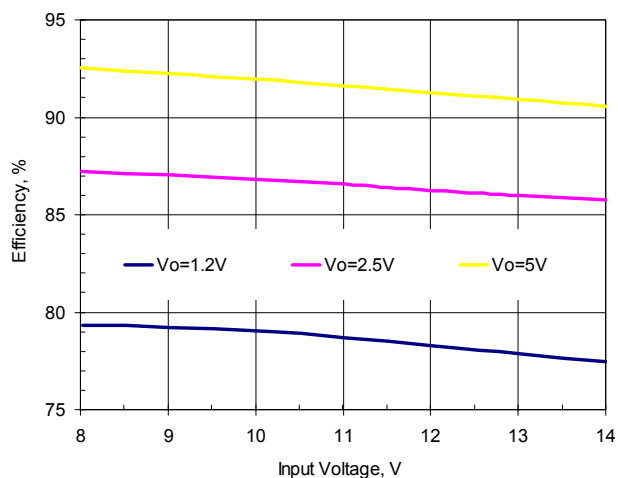


Figure 4. Efficiency vs. Input Voltage. Iout=10A, Fsw=500kHz

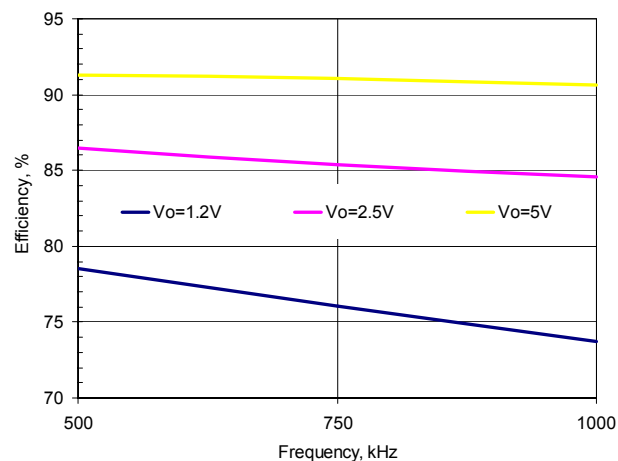


Figure 5. Efficiency vs. Switching Frequency. Iout=10A

5.2 Turn-On Characteristics

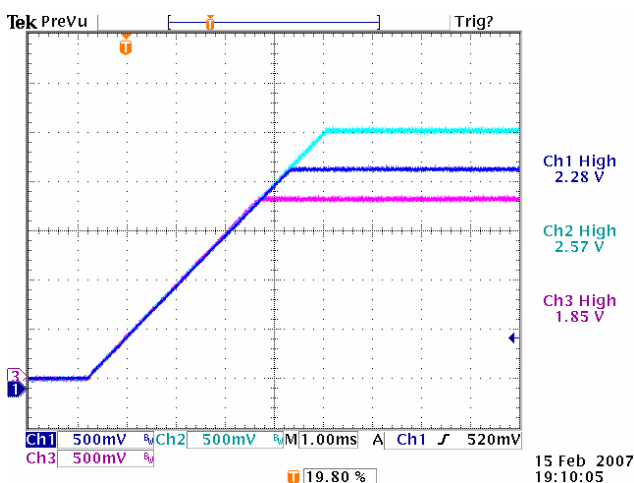


Figure 6. Tracking Turn-On. Rising Slew Rate is Programmed at 0.5V/ms.
Vin=12V, Ch1 - V1, Ch2 - V2, Ch3 - V3

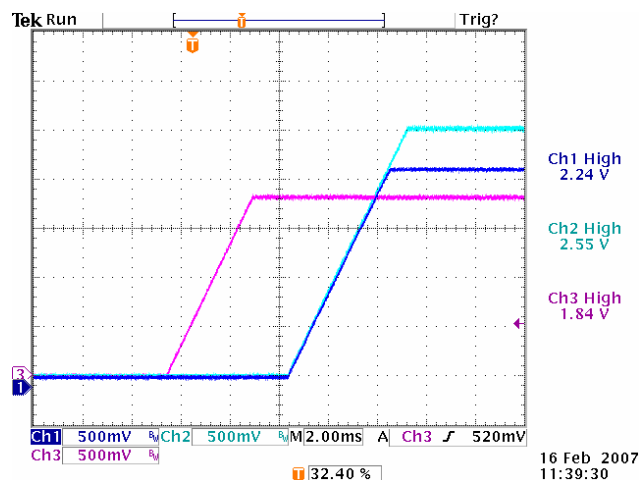


Figure 8. Turn On with Sequencing and Tracking. Rising Slew Rate Programmed at 0.5V/ms, V1 and V2 delays are programmed at 5ms.
Vin=12V, Ch1 - V1, Ch2 - V2, Ch3 - V3

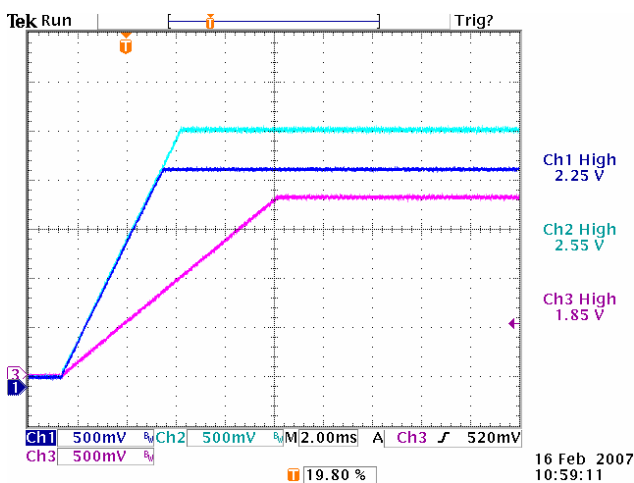


Figure 7. Turn-On with Different Rising Slew Rates.
Rising Slew Rates are Programmed as follows: V1- and V2-0.5V/ms, V3-0.2V/ms.
Vin=12V, Ch1 - V1, Ch2 - V2, Ch3 - V3

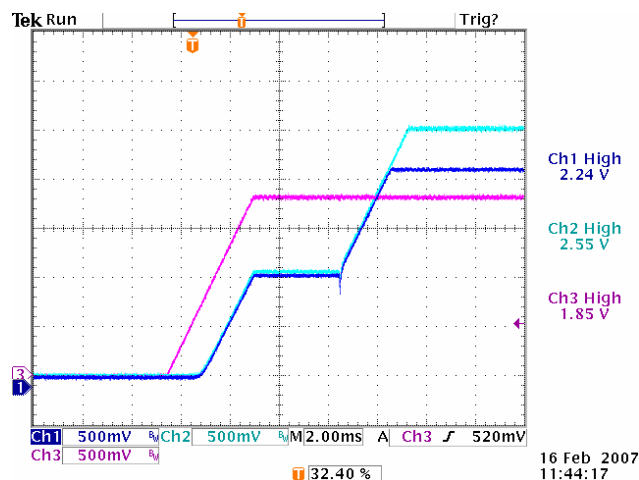


Figure 9. Turn On into Prebiased Load. V1 and V2 are Prebiased by V3 via a Diode.
Vin=12V, Ch1 - V1, Ch2 - V2, Ch3 - V3

5.3 Turn-Off Characteristics

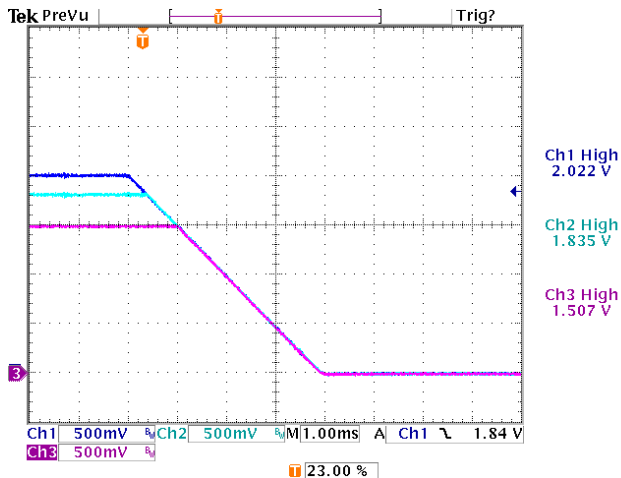


Figure 10. Tracking Turn-Off. Falling Slew Rate is Programmed at 0.5V/ms.
Vin=12V, Ch1 - V1, Ch2 - V2, Ch3 - V3

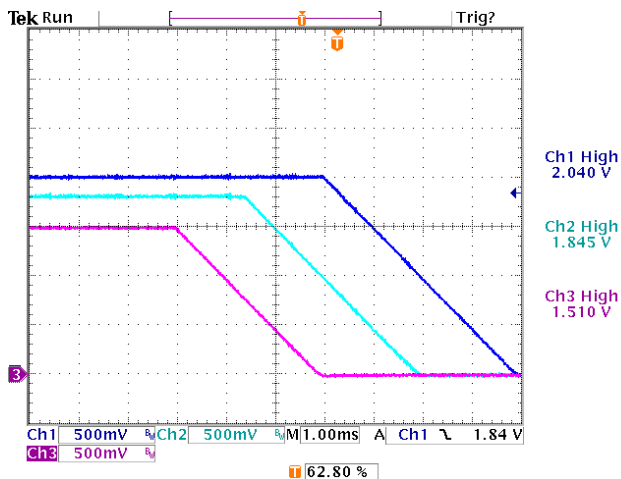


Figure 11. Turn-Off with Tracking and Sequencing. Falling Slew Rate is Programmed at 0.5V/ms.
Vin=12V, Ch1 - V1, Ch2 - V2, Ch3 - V3

5.4 Transient Response

The pictures below show the deviation of the output voltage in response to the 50-100-50% step load at 2.5A/μs. In all tests the ZY8110 converters operated at switching frequency of 1MHz and had a total 110μF of tantalum and ceramic capacitors connected across the output pins. Bandwidth of the feedback loop was programmed for faster transient response.

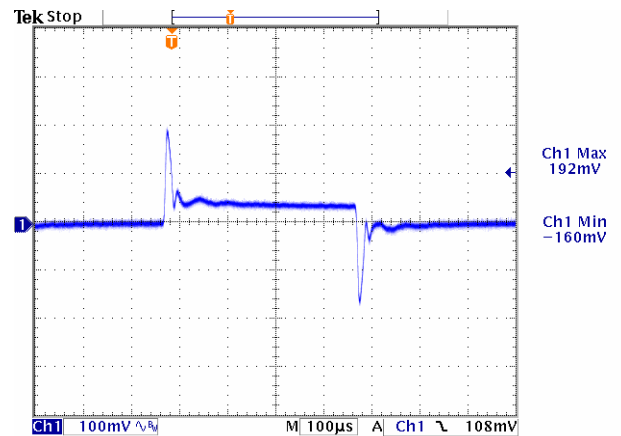


Figure 12. Vin=12V, Vout=5.0V

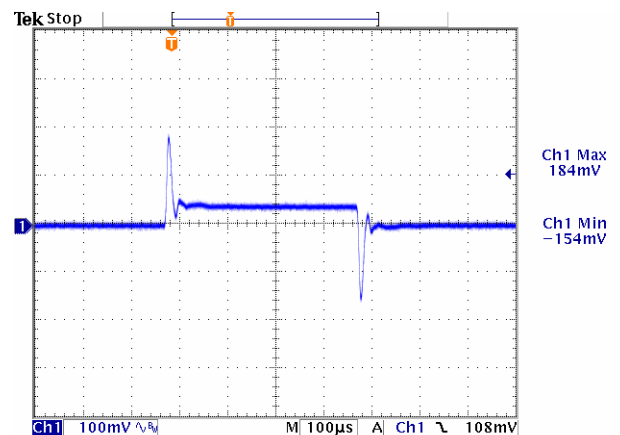


Figure 13. Vin=12V, Vout=2.5V

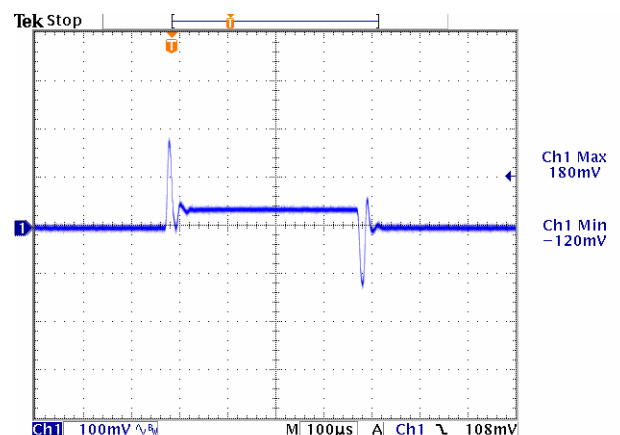


Figure 14. Vin=12V, Vout=1.0V

5.5 Thermal Derating Curves

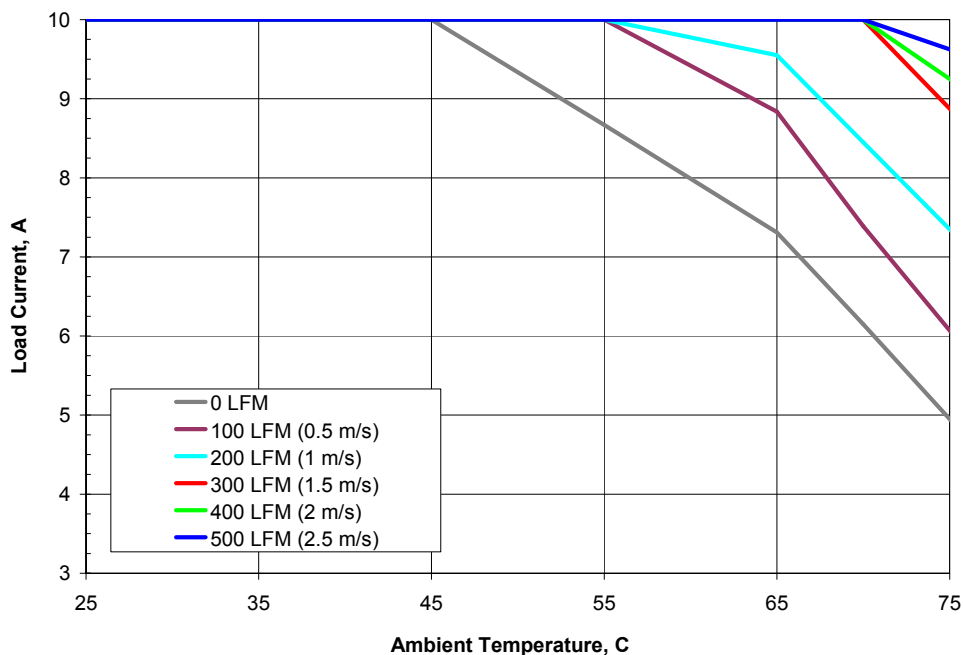


Figure 15. Thermal Derating Curves. $V_{in}=12V$, $V_{out}=5.0V$, $F_{sw}=500kHz$

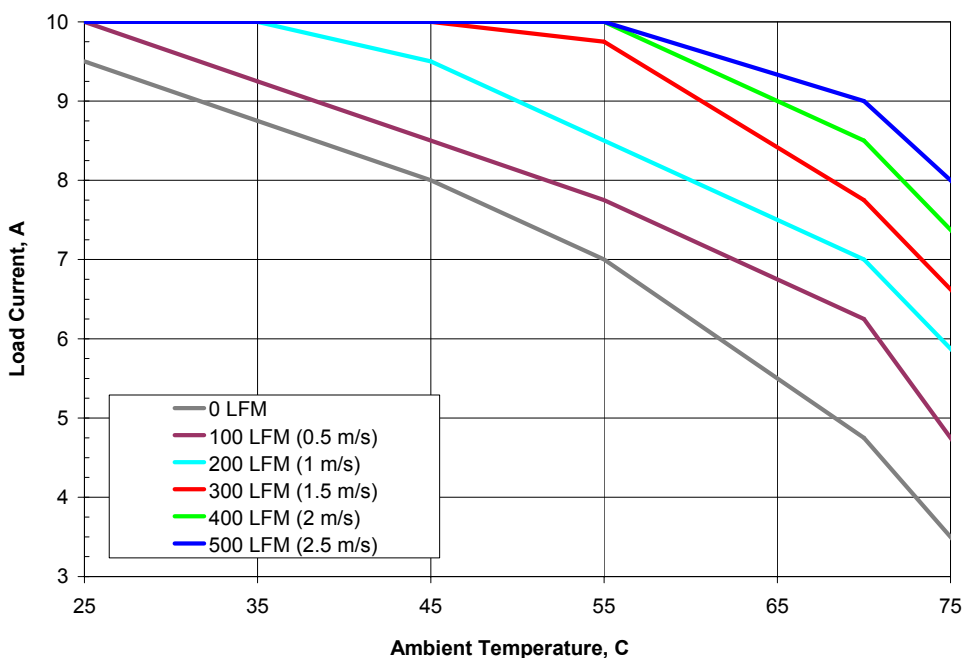


Figure 16. Thermal Derating Curves. $V_{in}=12V$, $V_{out}=5.0V$, $F_{sw}=1MHz$

6. Typical Application

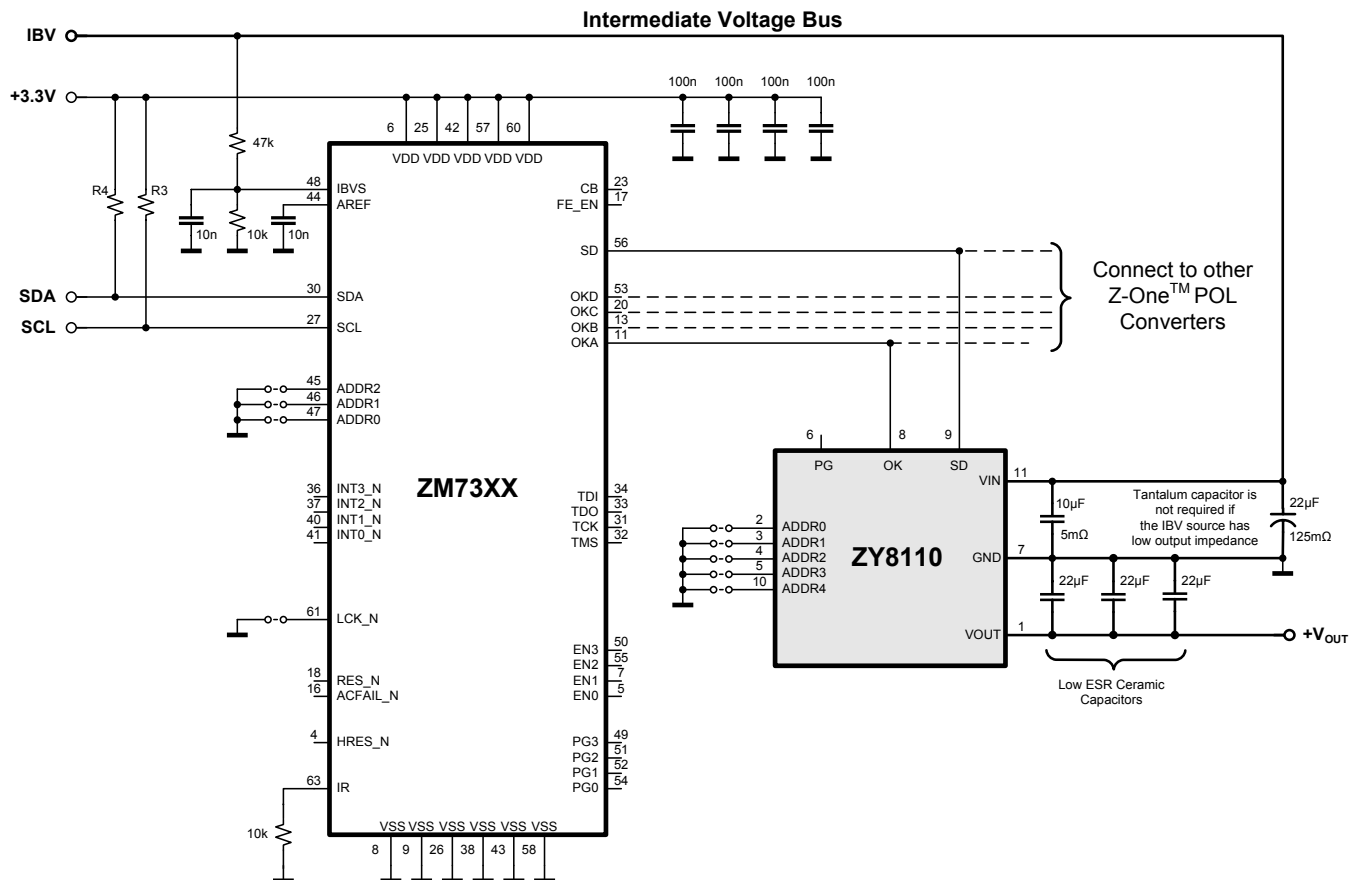


Figure 17. Block Diagram of Typical Application with Digital Power Manager and I²C Interface

The schematic of a typical application of ZY8110 point-of-load converters (POL) is shown in Figure 17. The system includes a ZM7300 series Digital Power Manager (DPM), a ZY8110 POL, and may include additional ZY8110 POLs and other Z-One® series POLs. All POLs are connected to the DPM and to each other via a single-wire SD (sync/data) line. The line provides synchronization of all POLs to the master clock generated by the DPM and simultaneously performs data transfer between POLs and the DPM. Each POL has a unique 5-bit address programmed by grounding respective address pins. To enable the current share, CS pins of POLs connected in parallel are interconnected.

In addition to the SD line, OK pins of the POLs are connected to the respective OK pins of the DPM. A number of POLs connected to the same OK pin of the DPM forms a group. Grouping of POLs enables users to program, control, and monitor multiple POLs simultaneously and execute advanced fault management schemes.

The type, value, and the number of output capacitors shown in the schematic are required to meet the specifications published in the data sheet. However, ZY8110 POLs are fully operational with different parameters of output capacitors. The feedback loop compensation may need to be adjusted to optimize performance of the POLs for specific parameters of the output capacitors.

7. Pin Assignments and Description

| Pin Name | Pin Number | Pin Type | Buffer Type | Pin Description | Notes |
|----------|------------|----------|-------------|------------------------|--|
| OK | 8 | I/O | PU | Fault/Status Condition | Connect to OK pin of other Z-POL and/or DPM. Leave floating, if not used |
| SD | 9 | I/O | PU | Sync/Data Line | Connect to SD pin of DPM |
| PGOOD | 6 | I/O | PU | Power Good | |
| ADDR4 | 10 | I | PU | POL Address Bit 4 | Tie to GND for 0 or leave floating for 1 |
| ADDR3 | 5 | I | PU | POL Address Bit 3 | Tie to GND for 0 or leave floating for 1 |
| ADDR2 | 4 | I | PU | POL Address Bit 2 | Tie to GND for 0 or leave floating for 1 |
| ADDR1 | 3 | I | PU | POL Address Bit 1 | Tie to GND for 0 or leave floating for 1 |
| ADDR0 | 2 | I | PU | POL Address Bit 0 | Tie to GND for 0 or leave floating for 1 |
| VOUT | 1 | P | | Output Voltage | |
| GND | 7 | P | | Power Ground | |
| VIN | 11 | P | | Input Voltage | |

Legend: I=input, O=output, I/O=input/output, P=power, A=analog, PU=internal pull-up

8. Programmable Features

Performance parameters of ZY8110 POL converters can be programmed via the industry standard I²C communication bus without replacing any components or rewiring PCB traces. Each parameter has a default value stored in the volatile memory registers detailed in Table 1. The setup registers 00h through 14h are programmed at the system power-up. When the user programs new performance parameters, the values in the registers are overwritten. Upon removal of the input voltage, the default values are restored.

Table 1. ZY8110 Memory Registers

| Register | Content | Address |
|----------|--|---------|
| PC1 | Protection Configuration 1 | 00h |
| PC2 | Protection Configuration 2 | 01h |
| PC3 | Protection Configuration 3 | 02h |
| DON | Turn-On Delay | 05h |
| DOF | Turn-Off Delay | 06h |
| TC | Tracking Configuration | 03h |
| INT | Interleave Configuration and Frequency Selection | 04h |
| RUN | RUN Register | 15h |
| ST | Status Register | 16h |
| VOS | Output Voltage Setpoint | 07h |
| CLS | Current Limit Setpoint | 08h |
| DCL | Duty Cycle Limit | 09h |
| B1 | Dig Controller Denominator z^{-1} Coefficient | 0Ah |
| B2 | Dig Controller Denominator z^{-2} Coefficient | 0Bh |
| B3 | Dig Controller Denominator z^{-3} Coefficient | 0Ch |
| C0L | Dig Controller Numerator z^0 Coefficient, Low Byte | 0Dh |
| C0H | Dig Controller Numerator z^0 Coefficient, High Byte | 0Eh |
| C1L | Dig Controller Numerator z^{-1} Coefficient, Low Byte | 0Fh |
| C1H | Dig Controller Numerator z^{-1} Coefficient, High Byte | 10h |
| C2L | Dig Controller Numerator z^{-2} Coefficient, Low Byte | 11h |
| C2H | Dig Controller Numerator z^{-2} Coefficient, High Byte | 12h |
| C3L | Dig Controller Numerator z^{-3} Coefficient, Low Byte | 13h |
| C3H | Dig Controller Numerator z^{-3} Coefficient, High Byte | 14h |
| VOM | Output Voltage Monitoring | 17h |
| IOM | Output Current Monitoring | 18h |
| TMP | Temperature Monitoring | 19h |

ZY8110 converters can be programmed using the Graphical User Interface or directly via the I²C bus by using high and low level commands as described in the "DPM Programming Manual".

ZY8110 parameters can be reprogrammed at any time during the system operation and service except for the digital filter coefficients, the switching frequency and the duty cycle limit, that can only be changed when the POL output is turned off.

8.1 Output Voltage

The output voltage can be programmed in the GUI Output Configuration window shown in the Figure 18 or directly via the I²C bus by writing into the VOS register shown in Figure 19.

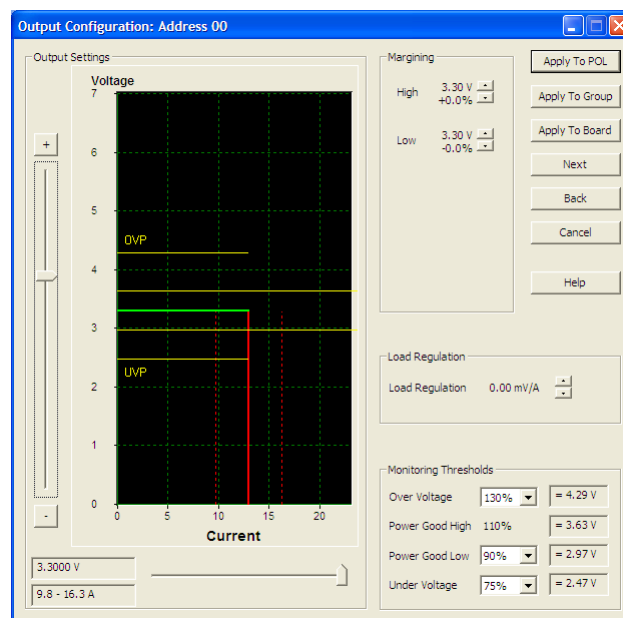


Figure 18. Output Configuration Window

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|--|-------|-------|-------|--|-------|-------|-------|
| VOS7 | VOS6 | VOS5 | VOS4 | VOS3 | VOS2 | VOS1 | VOS0 |
| Bit 7 | | | | Bit 0 | | | |
| Bit 7:0 VOS[7:0] . Output voltage setting | | | | <div>R = Readable bit W = Writable bit U = Unimplemented bit, read as '0' - n = Value at POR reset</div> | | | |
| 00h: corresponds to 0.5000V | | | | | | | |
| 01h: corresponds to 0.5125V | | | | | | | |
| ... | | | | | | | |
| 77h: corresponds to 1.9875V | | | | | | | |
| 78h: corresponds to 2.0000V | | | | | | | |
| 79h: corresponds to 2.025V | | | | | | | |
| ... | | | | | | | |
| F9h: corresponds to 5.225V | | | | | | | |
| FAh: corresponds to 5.250V | | | | | | | |
| FBh: corresponds to 5.300V | | | | | | | |
| ... | | | | | | | |
| FFh: corresponds to 5.500V | | | | | | | |

Figure 19. Output Voltage Setpoint Register VOS

8.1.1 Output Voltage Setpoint

The output voltage programming range is from 0.5V to 5.5V. To improve the resolution of the output voltage settings, the voltage range is divided into sub-ranges as shown in Table 2.

Table 2. Output Voltage Adjustment Resolution

| V _{OUT} MIN, V | V _{OUT} MAX, V | Resolution, mV |
|-------------------------|-------------------------|----------------|
| 0.500 | 2.000 | 12.5 |
| 2.025 | 5.25 | 25 |
| 5.3 | 5.5 | 50 |

8.1.2 Output Voltage Margining

If the output voltage needs to be varied by a certain percentage, the margining function can be utilized. The margining can be programmed in the GUI Output Configuration window or directly via the I²C bus using high level commands as described in the "DPM Programming Manual".

In order to properly margin POLs that are connected in parallel, the POLs must be members of one of the Parallel Buses. Refer to the GUI System Configuration Window shown in Figure 44.

8.1.3 Optimal Voltage Positioning

Optimal voltage positioning increases the voltage regulation window by properly positioning the output voltage setpoint. Positioning is determined by the load regulation that can be programmed in the GUI Output Configuration window shown in Figure 18 or directly via the I²C bus by writing into the CLS register shown in Figure 29.

Figure 20 illustrates optimal voltage positioning concept. If no load regulation is programmed, the headroom (voltage differential between the output voltage setpoint and a regulation limit) is approximately half of the voltage regulation window. When load regulation is programmed, the output voltage will decrease as the output current increases, so the VI characteristic will have a negative slope. Therefore, by properly selecting the operating point, it is possible to increase the headroom as shown in the picture.

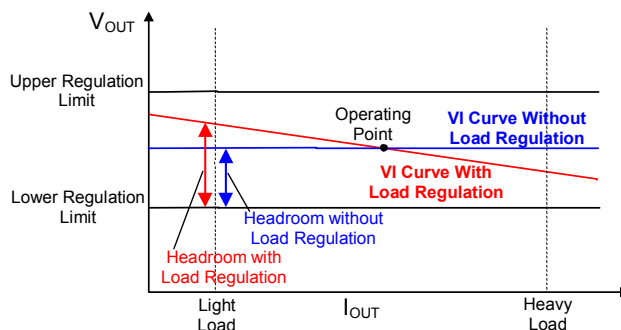


Figure 20. Concept of Optimal Voltage Positioning

Increased headroom allows tolerating larger voltage deviations. For example, the step load change from light to heavy load will cause the output voltage to drop. If the optimal voltage positioning is utilized, the output voltage will stay within the regulation window. Otherwise, the output voltage will drop below the lower regulation limit. To compensate for the voltage drop external output capacitance will need to be added, thus increasing cost and complexity of the system.

The effect of optimal voltage positioning is shown in Figure 21 and Figure 22. In this case, switching output load causes large peak-to-peak deviation of the output voltage. By programming load regulation, the peak to peak deviation is dramatically reduced.

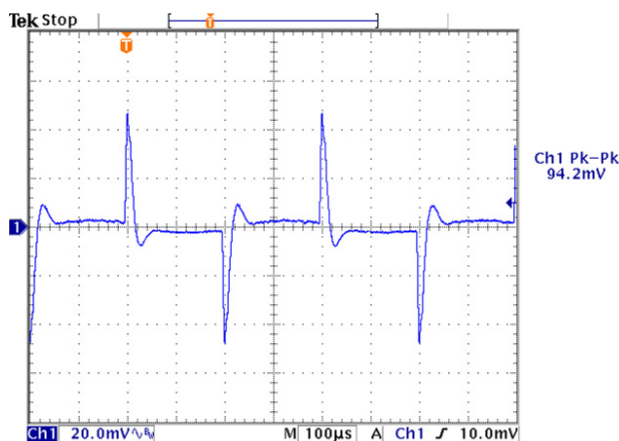


Figure 21. Transient Response without Optimal Voltage Positioning

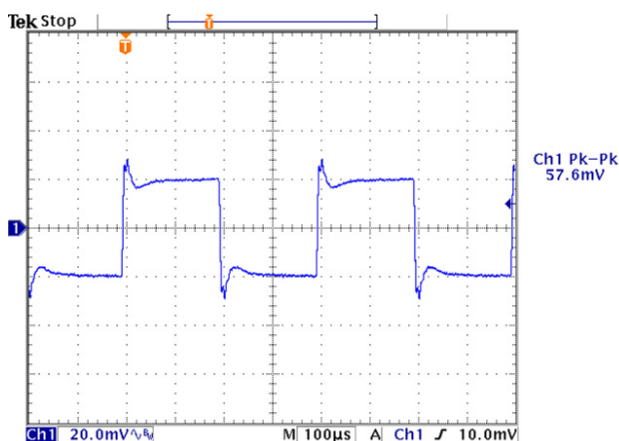


Figure 22. Transient Response with Optimal Voltage Positioning

8.2 Sequencing and Tracking

Turn-on delay, turn-off delay, and rising and falling output voltage slew rates can be programmed in the GUI Sequencing/Tracking window shown in Figure 23 or directly via the I²C bus by writing into the DON, DOF, and TC registers, respectively. The registers are shown in Figure 24, Figure 25, and Figure 27.

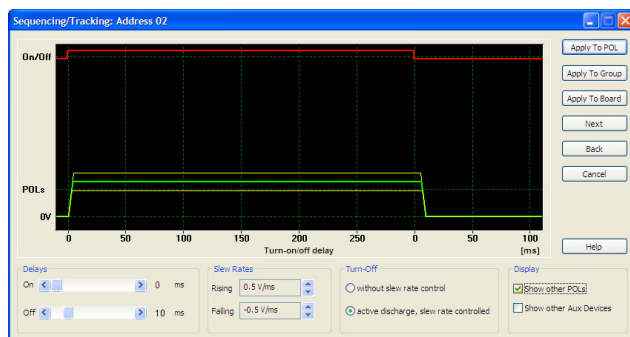


Figure 23. Sequencing/Tracking Window

8.2.1 Turn-On Delay

Turn-on delay is defined as an interval from the application of the Turn-On command until the output voltage starts ramping up.

| | | | | | | | |
|-------|-------|-------|-------|-------|-------|-------|-------|
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| DON7 | DON6 | DON5 | DON4 | DON3 | DON2 | DON1 | DON0 |
| Bit 7 | | | | Bit 0 | | | |

Bit 7:0 **DON[7:0]**: Turn-on delay time
00h: corresponds to 0ms delay after turn-on command has occurred
...
FFh: corresponds to 255ms delay after turn-on command has occurred

Figure 24. Turn-On Delay Register DON

8.2.2 Turn-Off Delay

| U | U | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|-------|-----|-------|-------|-------|-------|-------|-------|
| --- | --- | DOF5 | DOF4 | DOF3 | DOF2 | DOF1 | DOF0 |
| Bit 7 | | Bit 0 | | | | | |

Bit 7:6 **Unimplemented**, read as '0'

Bit 5:0 **DOF[5:0]**: Turn-off delay time

00h: corresponds to 0ms delay after turn-off command has occurred

...

3Fh: corresponds to 63ms delay after turn-off command has occurred

Figure 25. Turn-Off Delay Register DOF

Turn-off delay is defined as an interval from the application of the Turn-Off command until the output voltage reaches zero (if the falling slew rate is programmed) or until both high side and low side switches are turned off (if the slew rate is not programmed). Therefore, for the slew rate controlled turn-off the ramp-down time is included in the turn-off delay as shown in Figure 26.

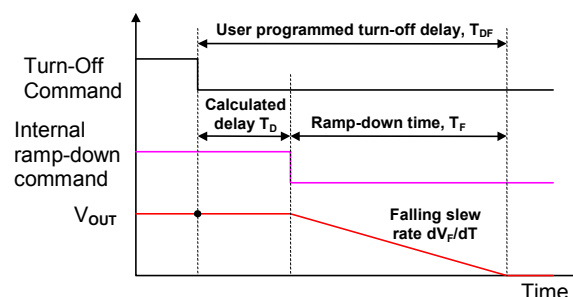


Figure 26. Relationship between Turn-Off Delay and Falling Slew Rate

As it can be seen from the figure, the internally calculated delay T_D is determined by the equation below.

$$T_D = T_{DF} - \frac{V_{OUT}}{dV_F/dT}$$

For proper operation T_D shall be greater than zero. The appropriate value of the turn-off delay needs to be programmed to satisfy the condition.

If the falling slew rate control is not utilized, the turn-off delay only determines an interval from the application of the Turn-Off command until both high side and low side switches are turned off. In this case, the output voltage ramp-down process is determined by load parameters.

8.2.3 Rising and Falling Slew Rates

The output voltage tracking is accomplished by programming the rising and falling slew rates of the output voltage. To achieve programmed slew rates, the output voltage is being changed in 12.5mV steps where duration of each step determines the slew rate. For example, ramping up a 1.0V output with a slew rate of 0.5V/ms will require 80 steps duration of 25µs each.

Duration of each voltage step is calculated by dividing the master clock frequency generated by the DPM. Since all POLs in the system are synchronized to the master clock, the matching of voltage slew rates of different outputs is very accurate as it can be seen in Figure 6 and Figure 10.

During the turn on process, a POL not only delivers current required by the load (I_{LOAD}), but also charges the load capacitance. The charging current can be determined from the equation below:

$$I_{CHG} = C_{LOAD} \times \frac{dV_R}{dt}$$

Where, C_{LOAD} is load capacitance, dV_R/dt is rising voltage slew rate, and I_{CHG} is charging current.

When selecting the rising slew rate, a user needs to ensure that

$$I_{LOAD} + I_{CHG} < I_{OCP}$$

Where I_{OCP} is the overcurrent protection threshold of the ZY8110. If the condition is not met, then the overcurrent protection will be triggered during the turn-on process. To avoid this, dV_R/dt and the overcurrent protection threshold should be programmed to meet the condition above.

| U | R/W-0 | R/W-0 | R/W-0 | R/W-1 | R/W-0 | R/W-0 | R/W-0 |
|---|-------|-------|-------|---|-------|-------|-------|
| --- | R2 | R1 | R0 | SC | F2 | F1 | F0 |
| Bit 7 | | | | Bit 0 | | | |
| Bit 7 Unimplemented , read as '0' | | | | <div>R = Readable bit W = Writable bit U = Unimplemented bit, read as '0' - n = Value at POR reset</div> | | | |
| Bit 6:4 R[2:0] : Value of Vo rising slope | | | | | | | |
| 0: corresponds to 0.1V/ms (default) | | | | | | | |
| 1: corresponds to 0.2V/ms | | | | | | | |
| 2: corresponds to 0.5V/ms | | | | | | | |
| 3: corresponds to 1.0V/ms | | | | | | | |
| 4: corresponds to 2.0V/ms | | | | | | | |
| 5: corresponds to 5.0V/ms | | | | | | | |
| 6: corresponds to 8.3V/ms | | | | | | | |
| 7: corresponds to 8.3V/ms | | | | | | | |
| Bit 3 SC , Slew rate control at turn-off | | | | | | | |
| 0: Slew rate control is disabled | | | | | | | |
| 1: Slew rate control is enabled | | | | | | | |
| Bit 2:0 F[2:0] : Value of Vo falling slope | | | | | | | |
| 0: corresponds to -0.1V/ms (default) | | | | | | | |
| 1: corresponds to -0.2V/ms | | | | | | | |
| 2: corresponds to -0.5V/ms | | | | | | | |
| 3: corresponds to -1.0V/ms | | | | | | | |
| 4: corresponds to -2.0V/ms | | | | | | | |
| 5: corresponds to -5.0V/ms | | | | | | | |
| 6: corresponds to -8.3V/ms | | | | | | | |
| 7: corresponds to -8.3V/ms | | | | | | | |

Figure 27. Tracking Configuration Register TC

8.3 Protections

ZY8110 Series converters have a comprehensive set of programmable protections. The set includes the output over- and undervoltage protections, overcurrent protection, overtemperature protection, tracking protection, overtemperature warning, and Power Good signal. Status of protections is stored in the ST register shown in Figure 28.

| | | | | | | | | |
|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| R-1 | R-0 | R-1 | R-1 | R-1 | R-1 | R-1 | R-1 | R-1 |
| TP | PG | TR | OT | OC | UV | OV | PV | |

Bit 7

Bit 7 **TP**: Temperature Warning

Bit 6 **PG**: Power Good Warning

Bit 5 **TR**: Tracking Fault

Bit 4 **OT**: Overtemperature Fault

Bit 3 **OC**: Overcurrent Fault

Bit 2 **UV**: Undervoltage Fault

Bit 1 **OV**: Overvoltage Error

Bit 0 **PV**: Phase Voltage Error (Not Active)

R = Readable bit
W = Writable bit
U = Unimplemented bit, read as '0'
- n = Value at POR reset

Note:
- An activated warning/fault/error is encoded as '0'

Figure 28. Protection Status Register ST

Thresholds of overcurrent, over- and undervoltage protections, and Power Good limits can be programmed in the GUI Output Configuration window or directly via the I²C bus by writing into the CLS and PC2 registers shown in Figure 29 and Figure 30.

| R/W-0 | R/W-0 | R/W-0 | R/W-1 | R/W-1 | R/W-0 | R/W-1 | R/W-1 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| LR2 | LR1 | LR0 | TCE | CLS3 | CLS2 | CLS1 | CLS0 |
| Bit 7 | | | | Bit 0 | | | |

Bit 7:5 **LR[2:0]**, Load regulation configuration

| | |
|------|--------------|
| 000: | 0 V/A/Ohm |
| 001: | 0.39 V/A/Ohm |
| 010: | 0.78 V/A/Ohm |
| 011: | 1.18 V/A/Ohm |
| 100: | 1.57 V/A/Ohm |
| 101: | 1.96 V/A/Ohm |
| 110: | 2.35 V/A/Ohm |
| 111: | 2.75 V/A/Ohm |

R = Readable bit
W = Writable bit
U = Unimplemented bit, read as '0'
- n = Value at POR reset

Bit 4 **TCE**, Temperature compensation enable

0: disabled
1: enabled

Bit 3:0 **CLS[3:0]**, Current limit setting

0h: corresponds to 37%
1h: corresponds to 47%
...
Bh: corresponds to 140%
Values higher than Bh are translated to Bh (140%)

Figure 29. Current Limit Setpoint Register CLS

| U | U | U | R/W-0 | R/W-1 | R/W-0 | R/W-0 | R/W-0 |
|--|-----|-----|--|-------|-------|-------|-------|
| --- | --- | --- | PGLL | OVPL1 | OVPL0 | UVPL1 | UVPL0 |
| Bit 7 | | | Bit 0 | | | | |
| Bit 7:5 Unimplemented , read as '0' | | | <div>R = Readable bit W = Writable bit U = Unimplemented bit, read as '0' - n = Value at POR reset</div> | | | | |
| Bit 4 PGLL : Set Power Good Low Level 1 = 95% of Vo 0 = 90% of Vo (Default) | | | | | | | |
| Bit 3:2 OVPL[1:0] : Set Over Voltage Protection Level 00 = 110% of Vo 01 = 120% of Vo 10 = 130% of Vo (Default) 11 = 130% of Vo | | | | | | | |
| Bit 1:0 UVPL[1:0] : Set Under Voltage Protection Level 00 = 75% of Vo (Default) 01 = 80% of Vo 10 = 85% of Vo 11 = 90% of Vo | | | | | | | |

Figure 30. Protection Configuration Register PC2

Note that the overvoltage and undervoltage protection thresholds and Power Good limits are defined as percentages of the output voltage. Therefore, the absolute levels of the thresholds change when the output voltage setpoint is changed either by output voltage adjustment or by margining.

In addition, a user can change type of protections (latching or non-latching) or disable certain protections. These settings are programmed in the GUI Fault Management window shown in Figure 31 or directly via the I²C by writing into the PC1 register shown in Figure 32.

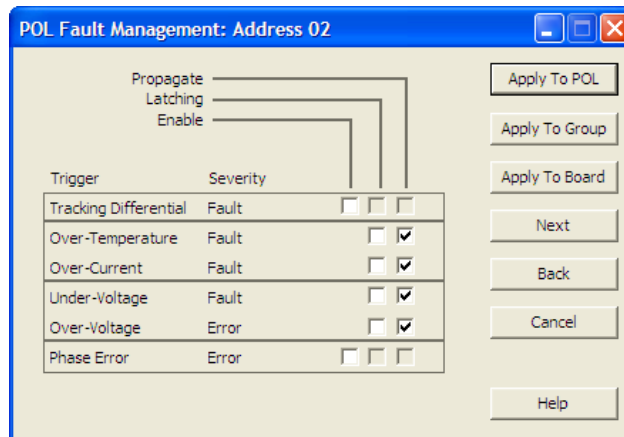


Figure 31. Fault Management Window

| R/W-0 | R/W-1 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-1 | R/W-1 |
|-------|---|-------|-------|-------|-------|--|-------|
| TRE | PVE | TRP | OTP | OCP | UVP | OVP | PVP |
| Bit 7 | | | | | | | Bit 0 |
| Bit 7 | TRE : Tracking fault enable 1 = enabled 0 = disabled | | | | | <div>R = Readable bit W = Writable bit U = Unimplemented bit, read as '0' - n = Value at POR reset</div> | |
| Bit 6 | PVE : Phase voltage error enable 1 = enabled 0 = disabled | | | | | | |
| Bit 5 | TRP : Tracking fault protection 1 = latching 0 = non latching | | | | | | |
| Bit 4 | OTP : Overtemperature protection configuration 1 = latching 0 = non latching | | | | | | |
| Bit 3 | OCP : Overcurrent protection configuration 1 = latching 0 = non latching | | | | | | |
| Bit 2 | UVP : Undervoltage protection configuration 1 = latching 0 = non latching | | | | | | |
| Bit 1 | OVP : Overvoltage protection configuration 1 = latching 0 = non latching | | | | | | |
| Bit 0 | PVP : Phase Voltage Protection (Not Active) 1 = latching 0 = non latching | | | | | | |

Figure 32. Protection Configuration Register PC1

If the non-latching protection is selected, a POL will attempt to restart every 130ms until the condition that triggered the protection is removed. When restarting, the output voltages follow tracking and sequencing settings.

If the latching type is selected, a POL will turn off and stay off. The POL can be turned on after 130ms, if the condition that caused the fault is removed and the respective bit in the ST register was cleared, or the Turn On command was recycled, or the input voltage was recycled.

All protections can be classified into three groups based on their effect on system operation: warnings, faults, and errors.

8.3.1 Warnings

This group includes Overtemperature Warning and Power Good Signal. The warnings do not turn off POLs but rather generate signals that can be transmitted to a host controller via the I²C bus.

8.3.1.1 Overtemperature Warning

The Overtemperature Warning is generated when temperature of the controller exceeds 120°C. The Overtemperature Warning changes the PT bit of the status register ST to 0 and sends the signal to the DPM. Reporting is enabled in the GUI Fault Management window or directly via the I²C by writing into the PC3 register shown in Figure 34. When the temperature falls below 117°C, the PT bit is cleared and the Overtemperature Warning is removed.

8.3.1.2 Power Good

Power Good is an open collector output that is pulled low, if the output voltage is outside of the Power Good window. The window is formed by the Power Good High threshold that is equal to 110% of the output voltage and the Power Good Low threshold that can be programmed at 90 or 95% of the output voltage.

The Power Good protection is only enabled after the output voltage reaches its steady state level. The PGOOD pin is pulled low during transitions of the output voltage from one level to other as shown in Figure 33.

The Power Good Warning pulls the Power Good pin low and changes the PG bit of the status register ST to 0. It sends the signal to the DPM, if the reporting is enabled. When the output voltage returns within the Power Good window, the PG pin is pulled high, the PG bit is cleared and the Power Good Warning is removed. The Power Good pin can also be pulled low by an external circuit to initiate the Power Good Warning.

Note: To retrieve status information, Status Monitoring in the GUI POL Group Configuration Window should be enabled (refer to Digital Power Manager Data Sheet). The DPM will retrieve the status information from each POL on a continuous basis.

8.3.2 Faults

This group includes overcurrent, overtemperature, undervoltage, and tracking protections. Triggering any protection in this group will turn off the POL.

8.3.2.1 Overcurrent Protection

Overcurrent protection is active whenever the output voltage of the POL exceeds the prebias voltage (if any). When the output current reaches the OC threshold, the output voltage will start decreasing. As soon as the output voltage decreases below the undervoltage protection threshold, the OC fault signal is generated, the POL turns off and the OC bit in the register ST is changed to 0. Both high side and low side switches of the POL are turned off instantly (fast turn-off).

The temperature compensation is added to keep the OC threshold approximately constant at temperatures above room temperature. Note that the temperature compensation can be disabled in the GUI Output Configuration window or directly via the I²C by writing into the CLS register. However, it is recommended to keep the temperature compensation enabled.

8.3.2.2 Undervoltage Protection

The undervoltage protection is only active during steady state operation of the POL to prevent nuisance tripping. If the output voltage decreases below the UV threshold and there is no OC fault, the UV fault signal is generated, the POL turns off, and the UV bit in the register ST is changed to 0. The output voltage is ramped down according to sequencing and tracking settings (regular turn-off).

8.3.2.3 Overtemperature Protection

Overtemperature protection is active whenever the POL is powered up. If temperature of the controller exceeds 120°C, the OT fault is generated, POL turns off, and the OT bit in the register ST is changed to 0. The output voltage is ramped down according to sequencing and tracking settings (regular turn-off).

If non-latching OTP is programmed, the POL will restart as soon as the temperature of the controller decreases below the Overtemperature Warning threshold of 110°C.

8.3.2.4 Tracking Protection

Tracking protection is active only when the output voltage is ramping up. The purpose of the protection is to ensure that the voltage differential between multiple rails being tracked does not exceed 250mV. This protection eliminates the need for external clamping diodes between different voltage rails which are frequently recommended by ASIC manufacturers.

When the tracking protection is enabled, the POL continuously compares actual value of the output voltage to its programmed value as defined by the output voltage and its rising slew rate. If absolute

value of the difference exceeds 250mV, the tracking fault signal is generated, the POL turns off, and the TR bit in the register ST is changed to 0. Both high side and low side switches of the POL are turned off instantly (fast turn-off).

The tracking protection can be disabled, if it contradicts requirements of a particular system (for example turning into high capacitive load where rising slew rate is not important). It can be disabled in the GUI Fault Management window or directly via the I²C bus by writing into the PC1 register.

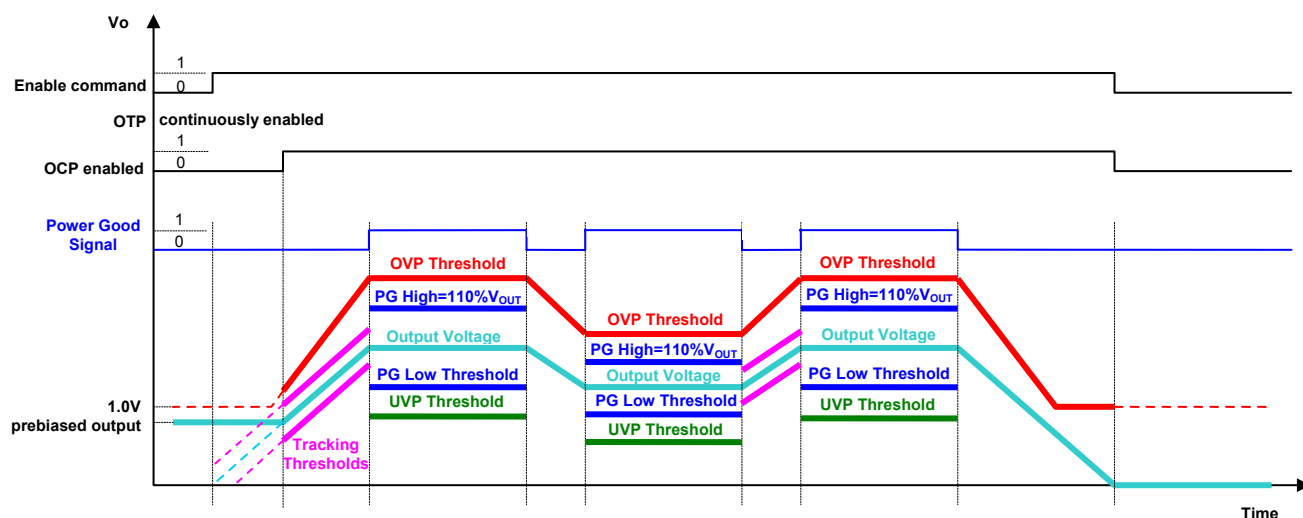


Figure 33. Protections Enable Conditions

8.3.3 Errors

The group includes overvoltage protection and the phase voltage error. The phase voltage error is not available in ZY8110.

8.3.3.1 Overvoltage Protection

The overvoltage protection is active whenever the output voltage of the POL exceeds the pre-bias voltage (if any). If the output voltage exceeds the overvoltage protection threshold, the overvoltage error signal is generated, the POL turns off, and the OV bit in the register ST is changed to 0. The high side switch is turned off instantly, and simultaneously the low side switch is turned on to ensure reliable protection of sensitive loads. The low side switch provides low impedance path to quickly dissipate

energy stored in the output filter and achieve effective voltage limitation.

The OV threshold can be programmed from 110% to 130% of the output voltage setpoint, but not lower than 1.0V.

8.3.4 Faults and Errors Propagation

The feature adds flexibility to the fault management scheme by giving users control over propagation of fault signals within and outside of the system. The propagation means that a fault in one POL can be programmed to turn off other POLs and devices in the system, even if they are not directly affected by the fault.

8.3.4.1 Grouping of POLs

Z-Series POLs can be arranged in several groups to simplify fault management. A group of POLs is defined as a number of POLs with interconnected OK pins. A group can include from 1 to 32 POLs. If fault propagation within a group is desired, the propagation bit needs to be checked in the GUI Fault Management Window. The parameters can also be programmed directly via the I²C bus by writing into the PC3 register shown in Figure 34.

When propagation is enabled, the faulty POL pulls its OK pin low. A low OK line initiates turn-off of other POLs in the group.

| R/W-0 | R/W-0 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 |
|-------|--|-------|-------|-------|-------|-------|-------|-------|
| PTM | PGM | TRP | OTP | OCP | UVP | OVP | PVP | |
| Bit 7 | | | | | | | | Bit 0 |
| Bit 7 | PTM : Temperature warning Message 1 = enabled 0 = disabled | | | | | | | |
| Bit 6 | PGM : Power good message 1 = enabled 0 = disabled | | | | | | | |
| Bit 5 | TRP : Tracking fault propagation 1 = enabled 0 = disabled | | | | | | | |
| Bit 4 | OTP : Overtemperature fault propagation 1 = enabled 0 = disabled | | | | | | | |
| Bit 3 | OCP : Overcurrent fault propagation 1 = enabled 0 = disabled | | | | | | | |
| Bit 2 | UVP : Undervoltage fault propagation 1 = enabled 0 = disabled | | | | | | | |
| Bit 1 | OVP : Overvoltage error propagation 1 = enabled 0 = disabled | | | | | | | |
| Bit 0 | PVP : Phase voltage error propagation (Not Active) 1 = enabled 0 = disabled | | | | | | | |

R = Readable bit
W = Writable bit
U = Unimplemented bit, read as '0'
- n = Value at POR reset

Figure 34. Protection Configuration Register PC3

In addition, the OK lines can be connected to the DPM to facilitate propagation of faults and errors between groups. One DPM can control up to 4 independent groups. To enable fault propagation between groups, the respective bit needs to be checked in the GUI Fault and Error Propagation window shown in Figure 35.

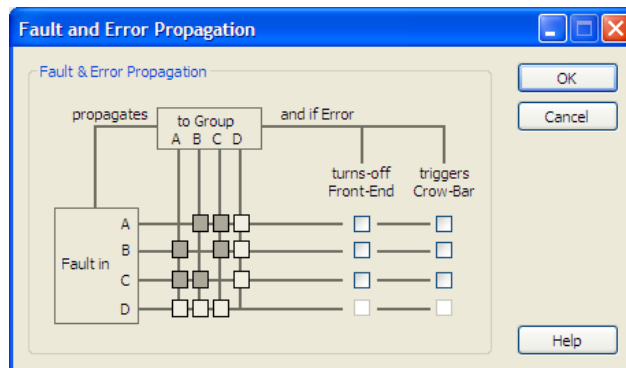


Figure 35. Fault and Error Propagation Window

In this case low OK line will signal DPM to pull other OK lines low to initiate shutdown of other POLs as programmed in the GUI Fault and Error Propagation window. If an error is propagated, the DPM can also generate commands to turn off a front end (a DC-DC converter generating the intermediate bus voltage) and trigger an optional crowbar protection to accelerate removal of the IBV voltage.

8.3.4.2 Propagation Process

Propagation of a fault (OCP, UVP, OTP, and TRP) initiates regular turn-off of other POLs. The faulty POL in this case performs either the regular or the fast turn-off depending on a specific fault as described in section 8.3.2.

Propagation of an error initiates fast turn-off of other POLs. The faulty POL performs the fast turn-off and turns on its low side switch.

Example of the fault propagation is shown in Figure 36 - Figure 37. In this three-output system (refer to the block diagram in Figure 17), the POL powering the output V3 (Ch 1 in the picture) encounters the undervoltage fault after the turn-on. When the fault propagation is not enabled, the POL turns off and generates the UV fault signal. Because the UV fault triggers the regular turn off, the POL meets its turn-off delay and falling slew rate settings during the turn-off process as shown in Figure 36. Since the UV fault is programmed to be non-latching, the POL will attempt to restart every 130ms, repeating the process described above until the condition causing the undervoltage is removed.

If the fault propagation between groups is enabled, the POL powering the output V3 pulls its OK line low and the DPM propagates the signal to the POL powering the output V1 that belongs to other group.

The POL powering the output V1 (Ch3 in the picture) executes the regular turn-off. Since both V1 and V3 have the same delay and slew rate settings they will continue to turn off and on synchronously every 130ms as shown in Figure 37 until the condition causing the undervoltage is removed. The POL powering the output V2 continues to ramp up until it reaches its steady state level.

130ms is the interval from the instant of time when the output voltage ramps down to zero until the output voltage starts to ramp up again. Therefore, the 130ms hiccup interval is guaranteed regardless of the turn-off delay setting.

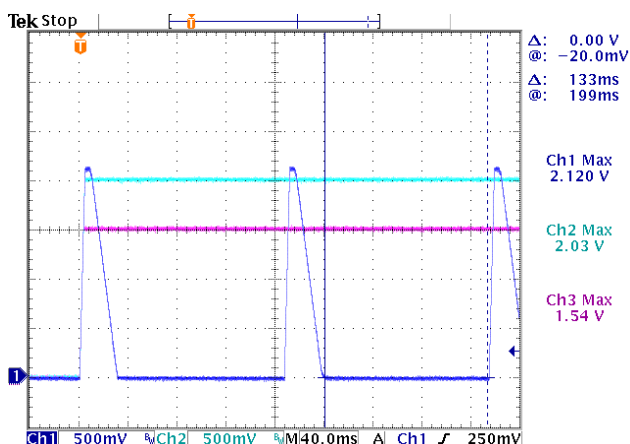


Figure 36. Turn-On into UVP on V3. The UV Fault Is Programmed To Be Non-Latching. Ch1 – V3 (Group C), Ch2 – V2, Ch3 – V1 (Group A)

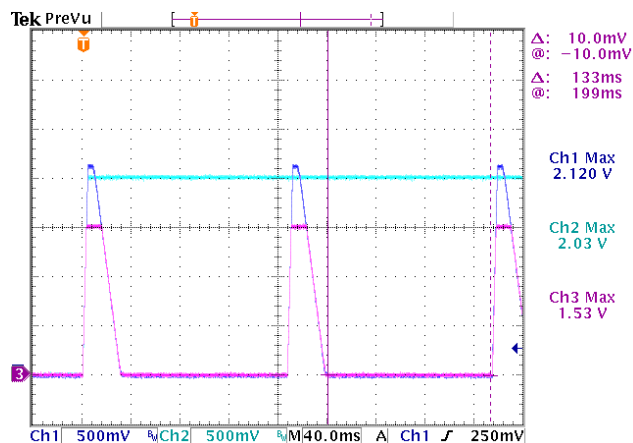


Figure 37. Turn-On into UVP on V3. The UV Fault Is Programmed To Be Non-Latching and Propagate From Group C to Group A. Ch1 – V3 (Group C), Ch2 – V2, Ch3 – V1 (Group A)

Summary of protections, their parameters and features are shown in Table 3

Table 3. Summary of Protections Parameters and Features

| Code | Name | Type | When Active | Turn Off | Low Side Switch | Propagation | Disable |
|------|---------------------|---------|--------------------------------|----------|-----------------|---------------------|---------|
| PT | Temperature Warning | Warning | Whenever V_{IN} is applied | No | N/A | Sends signal to DPM | No |
| PG | Power Good | Warning | During steady state | No | N/A | Sends signal to DPM | No |
| TR | Tracking | Fault | During ramp up | Fast | Off | Regular turn off | Yes |
| OT | Overtemperature | Fault | Whenever V_{IN} is applied | Regular | Off | Regular turn off | No |
| OC | Overcurrent | Fault | When V_{OUT} exceeds prebias | Fast | Off | Regular turn off | No |
| UV | Undervoltage | Fault | During steady state | Regular | Off | Regular turn off | No |
| OV | Overvoltage | Error | When V_{OUT} exceeds prebias | Fast | On | Fast turn off | No |

8.4 PWM Parameters

Z-Series POLs utilize the digital PWM controller. The controller enables users to program most of the PWM performance parameters, such as switching frequency, interleave, duty cycle, and feedback loop compensation.

8.4.1 Switching Frequency

The switching frequency can be programmed in the GUI PWM Controller window shown in Figure 38 or directly via the I²C bus by writing into the INT register shown in Figure 39. Note that the content of the register can be changed only when the POL is turned off.

Switching actions of all POLs connected to the SD line are synchronized to the master clock generated by the DPM. Each POL is equipped with a PLL and a frequency divider so they can operate at multiples (including fractional) of the master clock frequency as programmed by a user. The POL converters can operate at 500kHz, 750kHz, and 1MHz. Although synchronized, switching frequencies of different POLs are independent of each other. It is permissible to mix POLs operating at different frequencies in one system. It allows optimizing efficiency and transient response of each POL in the system individually.

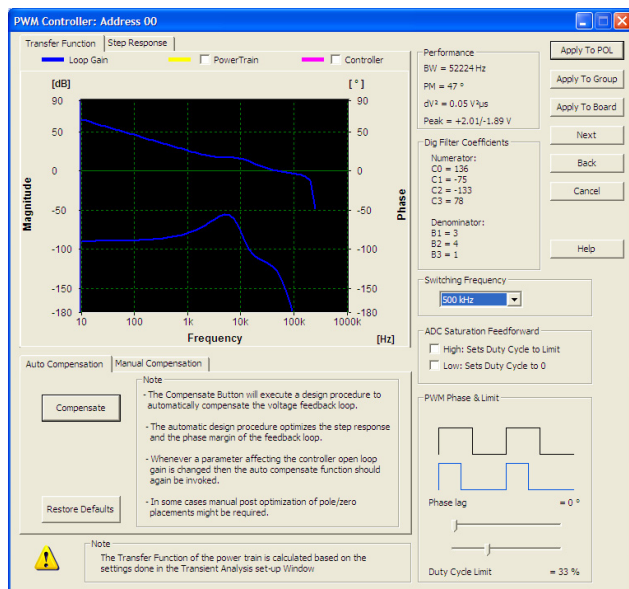


Figure 38. PWM Controller Window

| | | | | | | | |
|-------|-------|-------|---------------------|---------------------|---------------------|---------------------|---------------------|
| R/W-0 | R/W-0 | R/W-0 | R/W-0 ¹⁾ | R/W-0 ¹⁾ | R/W-0 ¹⁾ | R/W-0 ¹⁾ | R/W-0 ¹⁾ |
| FRQ2 | FRQ1 | FRQ0 | INT4 | INT3 | INT2 | INT1 | INT0 |
| Bit 7 | | | Bit 0 | | | | |

Bit 7:5 **FRQ[2:0]**: PWM Frequency Selection

000: 500kHz
001: 750kHz
010: 1000kHz

R = Readable bit
W = Writable bit
U = Unimplemented bit, read as '0'
- n = Value at POR reset

Bit 4:0 **INT[4:0]**: Interleave position

00h: Ton starts with 0.0° Phase lag to SD Line
01h: Ton starts with 11.25° Phase lag to SD Line
02h: Ton starts with 22.50° Phase lag to SD Line
...
1Fh: Ton starts with 348.75° Phase lag to SD Line

¹⁾ Initial value depends on the state of the Interleave Mode (**IM**) Input:
IM=Open: At POR reset the 5 corresponding ADDRESS bits are loaded
IM=Low: At POR reset a 0 is loaded

Figure 39. Interleave Configuration Register INT

8.4.2 Interleave

Interleave is defined as a phase delay between the synchronizing slope of the master clock on the SD pin and PWM signal of a POL. The interleave can be programmed in the GUI PWM Controller window or directly via the I²C bus by writing into the INT register.

Every POL generates switching noise. If no interleave is programmed, all POLs in the system switch simultaneously and noise reflected to the input source from all POLs is added together as shown in Figure 40.

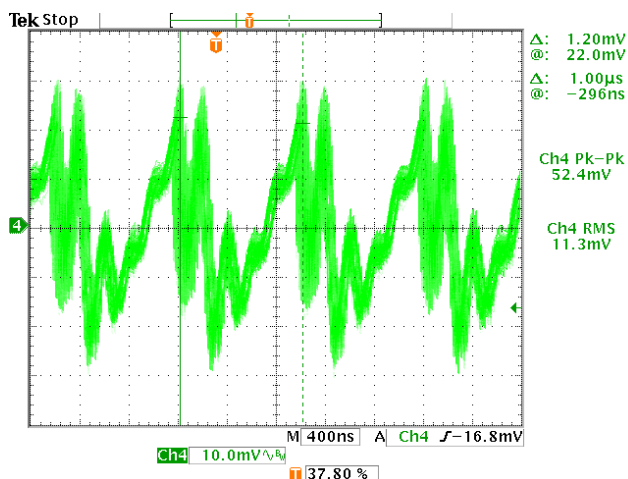


Figure 40. Input Voltage Noise, No Interleave

Figure 41 shows the input voltage noise of the three-output system with programmed interleave. Instead of all three POLs switching at the same time as in the previous example, the POLs V1, V2, and V3 switch at 67.5°, 180°, and 303.75°, respectively. Noise is spread evenly across the switching cycle resulting in more than 1.5 times reduction. To achieve similar noise reduction without the interleave will require the addition of an external LC filter.

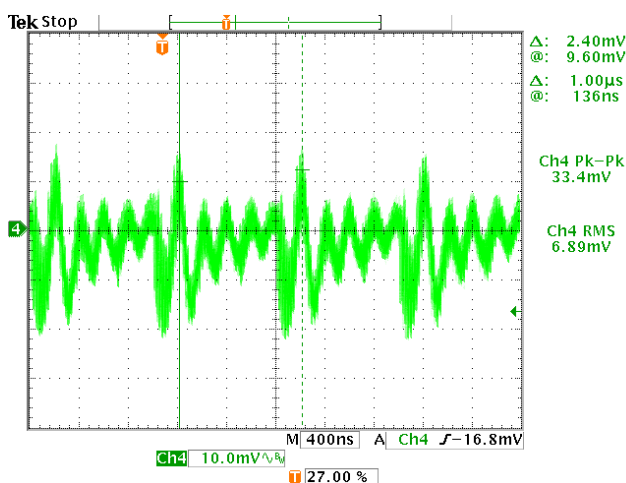


Figure 41. Input Voltage Noise with Interleave

ZY8110 interleave is independent of the number of POLs in a system and is fully programmable in 11.25° steps. It allows maximum output noise reduction by intelligently spreading switching energy.

Note: Due to noise sensitivity issues that may occur in limited cases, it is recommended to avoid phase lag settings of 112.5 and 123.75 degrees, otherwise false PG and/or OV indications may occur.

8.4.3 Duty Cycle Limit

The ZY8110 is a step-down converter therefore V_{OUT} is always less than V_{IN} . The relationship between the two parameters is characterized by the duty cycle and can be estimated from the following equation:

$$DC = \frac{V_{OUT}}{V_{IN,MIN}}$$

Where, DC is the duty cycle, V_{OUT} is the required maximum output voltage (including margining), $V_{IN,MIN}$ is the minimum input voltage.

It is good practice to limit the maximum duty cycle of the PWM controller to a somewhat higher value

compared to the steady-state duty cycle as expressed by the above equation. This will further protect the output from excessive voltages. The duty cycle limit can be programmed in the GUI PWM Controller window or directly via the I²C bus by writing into the DCL register shown in Figure 42.

| R/W-1 | R/W-1 | R/W-1 | R/W-0 | R/W-1 | R/W-0 | R/W-0 | R/W-0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| DCL5 | DCL4 | DCL3 | DCL2 | DCL1 | DCL0 | HI | LO |
| Bit 7 | | | | | | Bit 0 | |

Bit 7:2 **DCL[5:0]**, Duty Cycle Limitation

00h: 0

01h: 1/192

...

3Fh: 63/192

Bit 1: **HI**, ADC high saturation feed -forward

0: disabled

1: enabled

Bit 0: **LO**, ADC low saturation feed -forward

0: disabled

1: enabled

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

- n = Value at POR reset

Figure 42. Duty Cycle Limit Register

8.4.4 ADC Saturation Feedforward

To speed up the PWM response in case of heavy dynamic loads, the duty cycle can be forced either to 0 or the duty cycle limit depending on the polarity of the transient. This function is equivalent to having two comparators defining a window around the output voltage setpoint. When an error signal is inside the window, it will produce gradual duty cycle change proportional to the error signal. If the error signal goes outside the window (usually due to large output current steps), the duty cycle will change to its limit in one switching cycle. In most cases this will significantly improve transient response of the controller, reducing amount of required external capacitance.

Under certain circumstances, usually when the maximum duty cycle limit significantly exceeds its nominal value, the ADC saturation can lead to the overcompensation of the output error. The phenomenon manifests itself as low frequency oscillations on the output of the POL. It can usually be reduced or eliminated by disabling the ADC saturation or limiting the maximum duty cycle to 120-140% of the calculated value. It is not recommended to use ADC saturation for output voltages higher than 2.0V.

The ADC saturation feedforward can be programmed in the GUI PWM Controller window or

directly via the I²C bus by writing into the DCL register.

8.4.5 Feedback Loop Compensation

Feedback loop compensation can be programmed in the GUI PWM Controller window by setting frequency of poles and zeros of the transfer function.

The transfer function of the POL converter is shown in Figure 43. It is a third order function with two zeros and three poles. Pole 1 is the integrator pole, Pole 2 is used in conjunction with Zero 1 and Zero 2 to adjust the phase lead and limit the gain increase in mid band. Pole 3 is used as a high frequency low-pass filter to limit PWM noise.

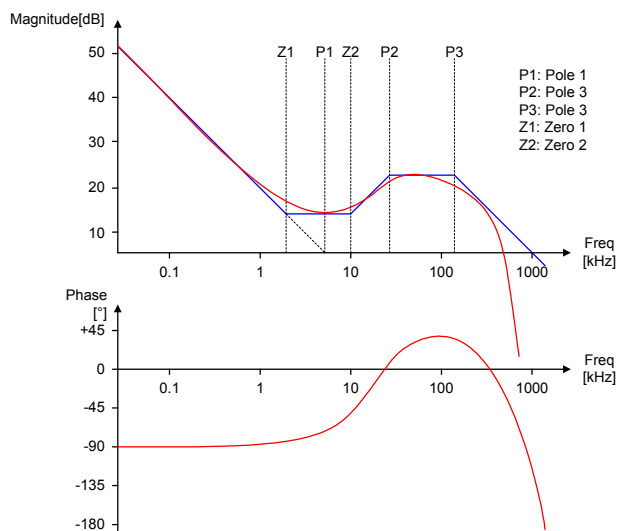


Figure 43. Transfer Function of PWM

Positions of poles and zeroes are determined by coefficients of the digital filter. The filter is characterized by four numerator coefficients (C_0 , C_1 , C_2 , C_3) and three denominator coefficients (B_1 , B_2 , B_3). The coefficients are automatically calculated when desired frequency of poles and zeros is entered in the GUI PWM Controller window. The

coefficients are stored in the C0H, C0L, C1H, C1L, C2H, C2L, C3H, C3L, B1, B2, and B3 registers.

Note: The GUI automatically transforms zero and pole frequencies into the digital filter coefficients. It is strongly recommended to use the GUI to determine the filter coefficients.

Programming feedback loop compensation allows optimizing POL performance for various application conditions. For example, increase in bandwidth can significantly improve dynamic response.

8.5 Performance Parameters Monitoring

The POL converters can monitor their own performance parameters such as output voltage, output current, and temperature.

The output voltage is measured at the output sense pins, output current is measured using the ESR of the output inductor and temperature is measured by the thermal sensor built into the controller IC. Output current readings are adjusted based on temperature readings to compensate for the change of ESR of the inductor with temperature.

An 8-Bit Analog to Digital Converter (ADC) converts the output voltage, output current, and temperature into a digital signal to be transmitted via the serial interface. The ADC allows a minimum sampling frequency of 700 Hz for all three values.

Monitored parameters are stored in registers (VOM, IOM, and TMON) that are continuously updated. If the Retrieve Monitoring bits in the GUI Group Configuration window shown in Figure 45 are checked, those registers are being copied into the ring buffer located in the DPM. Contents of the ring buffer can be displayed in the GUI IBS Monitoring Window shown in Figure 46 or it can be read directly via the I²C bus using high and low level commands as described in the "DPM Programming Manual".

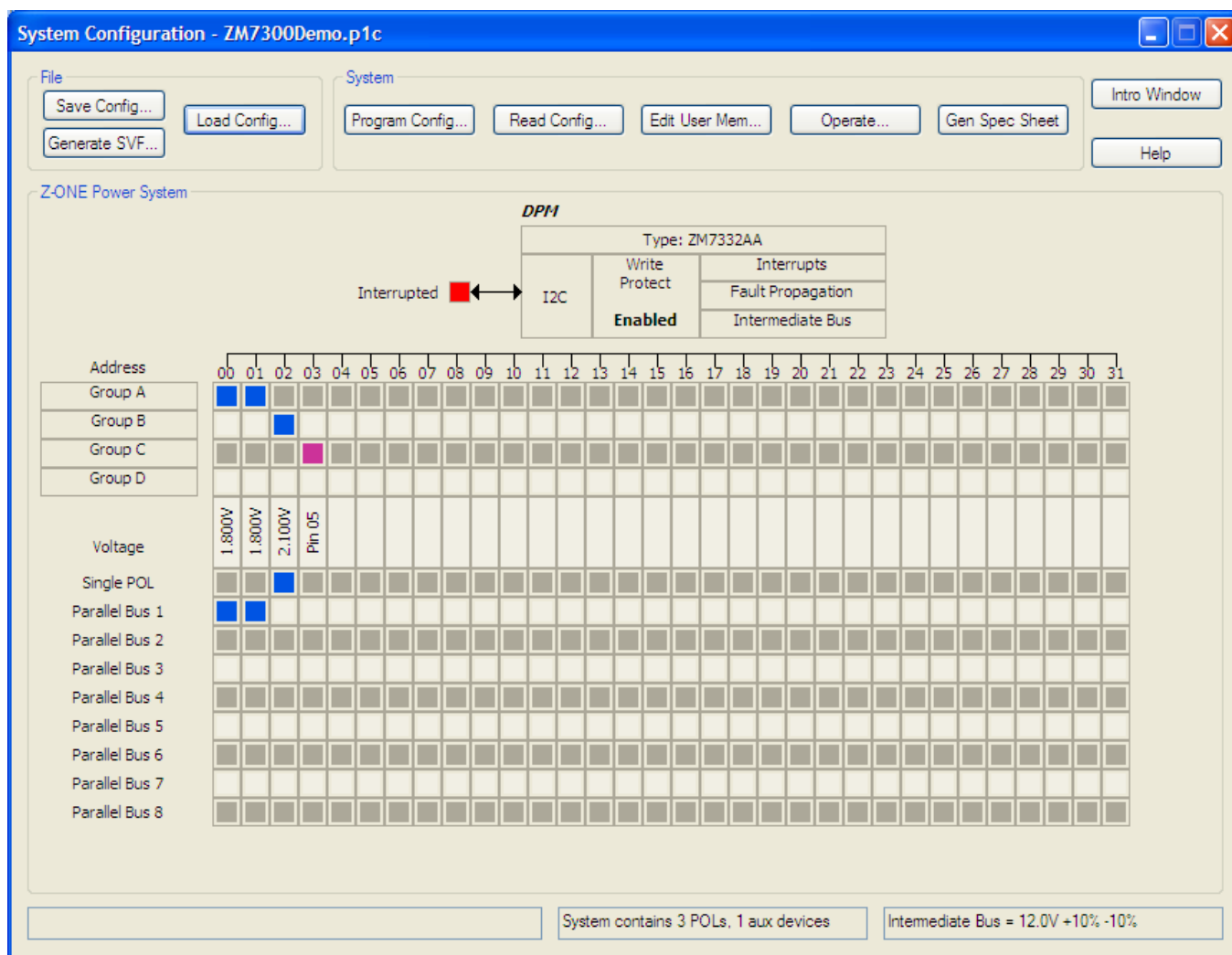


Figure 44. GUI System Configuration Window

POL Configuration: Address 0

| | | |
|------------------------------------|--------------------------|------------------------|
| Device Type | ZY8110 | |
| Fault Management | Tracking Fault | Disabled |
| | Temperature Fault | Auto Restart/Propagate |
| | Over-Current Fault | Auto Restart/Propagate |
| | Under-Voltage Error | Auto Restart/Propagate |
| | Over-Voltage Fault | Auto Restart/Propagate |
| | Phase Voltage Error | Latching/Propagate |
| Output Configuration | Output Voltage | 2.00V |
| | Load Regulation | 0.0 mV/A |
| | Current Limitation | 13.0 A |
| | Over-Voltage Threshold | 2.6 V |
| | Power Good Low Threshold | 1.8 V |
| | Under-Voltage Threshold | 1.5 V |
| Sequencing | Turn-On Delay | 0 ms |
| | Turn-On Slew Rate | 1.0 V/ms |
| | Turn-Off Delay | 10 ms |
| | Turn-Off Slew Rate | -1.0 V/ms |
| PWM Controller | Switching Frequency | 500 kHz |
| | Zero 1 | 9872 Hz |
| | Zero 2 | 49314 Hz |
| | Pole 1 | 1335 Hz |
| | Pole 2 | 177772 Hz |
| | Pole 3 | 442223 Hz |
| | PWM Phase Lag | 0 ° |
| | PWM Duty Cycle Limit | 33% |
| Transient Simulation Set-Up Window | | |
| Edit Device Output Configuration | | |

Return

Program

Help

Address Select: < 0 >

Figure 45. POL Group Configuration Window

9. Safety

The ZY8110 POL converters **do not provide isolation** from input to output. The input devices powering ZY8110 must provide relevant isolation requirements according to all IEC60950 based standards. Nevertheless, if the system using the converter needs to receive safety agency approval, certain rules must be followed in the design of the system. In particular, all of the creepage and clearance requirements of the end-use safety requirements must be observed. These requirements are included in UL60950 - CSA60950-00 and EN60950, although specific applications may have other or additional requirements.

The ZY8110 POL converters have no internal fuse. If required, the external fuse needs to be provided to protect the converter from catastrophic failure. Refer to the "Input Fuse Selection for DC/DC converters" application note on www.power-one.com for proper selection of the input fuse. Both input traces and the chassis ground trace (if applicable) must be capable of conducting a current of 1.5 times the value of the fuse without opening. The fuse must not be placed in the grounded input line.

Abnormal and component failure tests were conducted with the POL converter's input protected by a fast-acting 125V, 10A, fuse. If a fuse rated

greater than 10A is used, additional testing may be required.

In order for the output of the ZY8110 POL converter to be considered as SELV (Safety Extra Low

Voltage), according to all IEC60950 based standards, the input to the POL needs to be supplied by an isolated secondary source providing a SELV also.

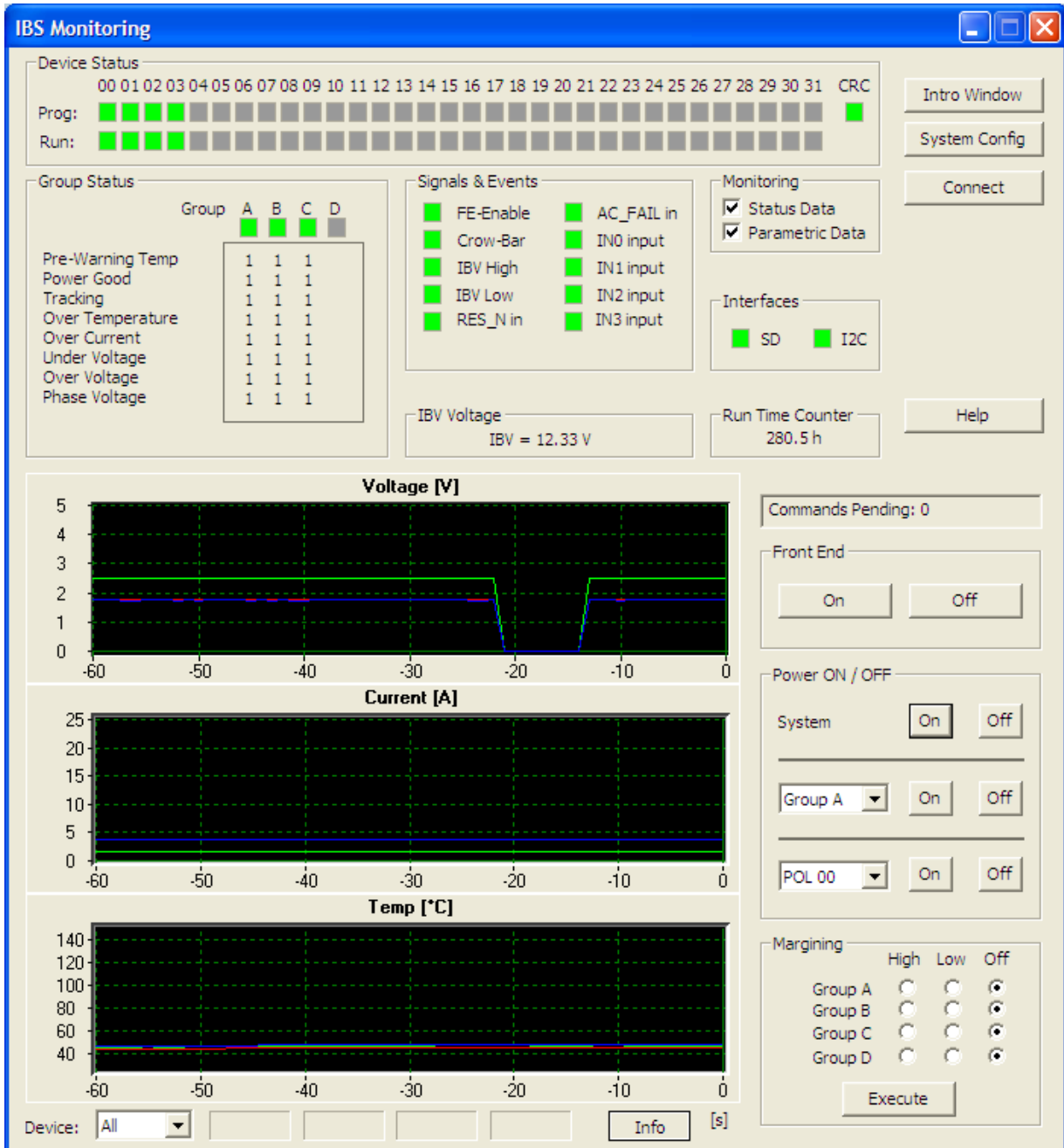


Figure 46. IBS Monitoring Window

10. Mechanical Drawings

All Dimensions are in mm

Tolerances: XX.X: ± 0.1 XX.XX: ± 0.05

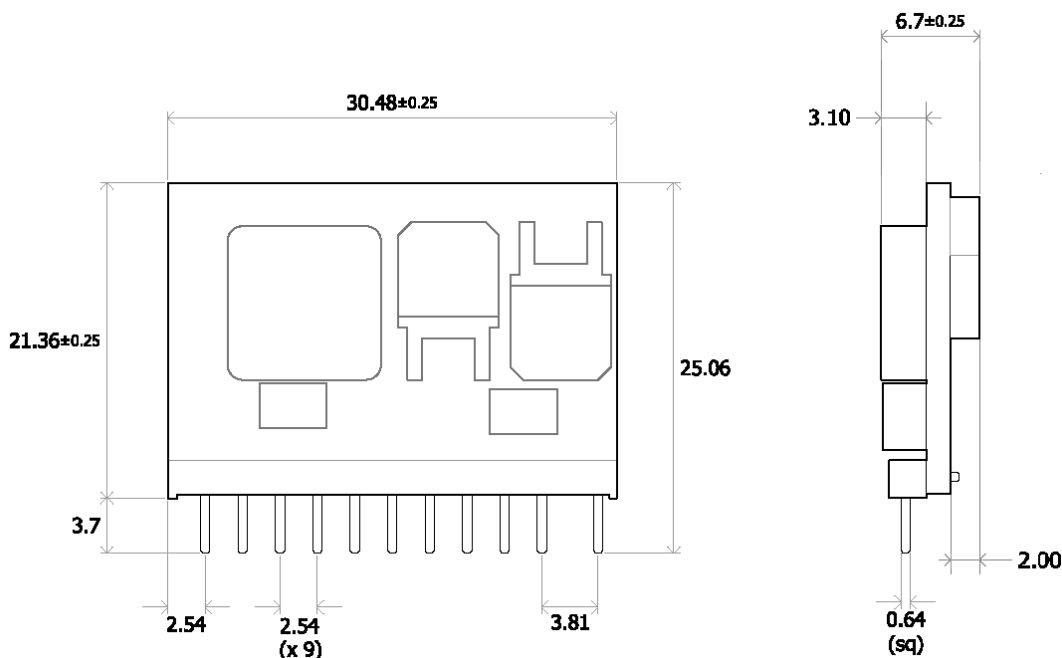


Figure 47. Mechanical Drawing

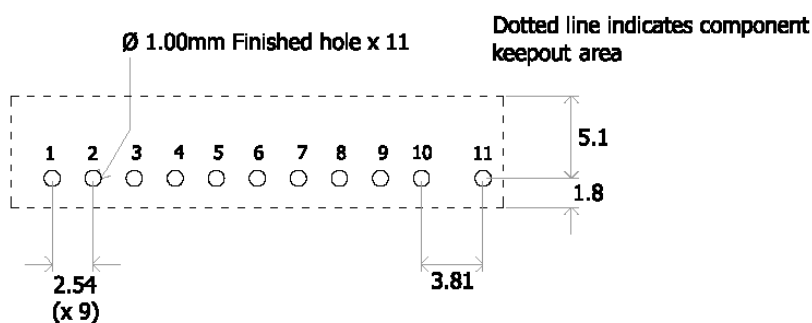


Figure 48. Recommended Footprint – Top View

Notes:

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