

Description

The DFC15 Series of dc-dc converters is designed to provide a wide range of PCB power solutions. The converters feature dual-output filters for low noise. Trim and remote On/Off features give flexibility to designs. The output of the converter is electrically isolated, thereby allowing the output to be configured as a positive or negative output voltage. The ultra-wide input range, from 20 to 60 volts, allows use in many industrial and communication applications.

Features

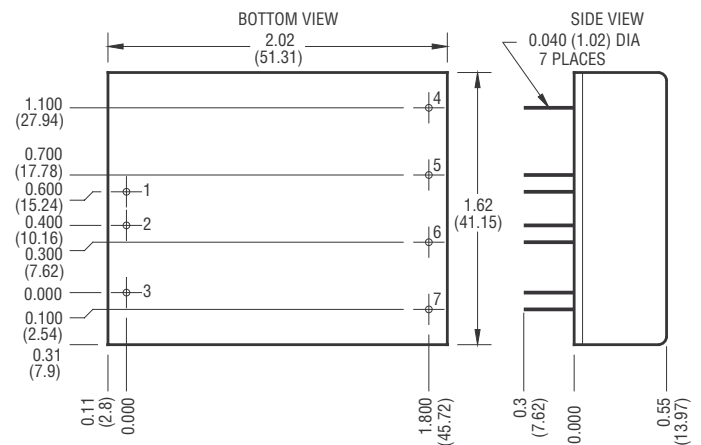
- RoHS lead solder exemption compliant
- Up to 15 watts output power
- Efficiencies to 83%
- Very low Off current
- 700 V isolation
- Dual-stage output filter
- -40 °C to +90 °C operation
- Ultra-wide range input (3:1)
- Remote On/Off and Trim



Model Selection				
Model	Input Range VDC		Output VDC	Output mA
	Min	Max		
DFC15U48S5	20	60	5	3000
DFC15U48S12	20	60	12	1250
DFC15U48S15	20	60	15	1000

Model numbers highlighted in yellow or shaded are not recommended for new designs.

General Specifications (1)				
All Models				Units
ON/OFF Function (2)				
OFF Logic Level or Pin Open	MIN	8.0	VDC	
OFF Logic Level	MAX	2.0	VDC	
Input Resistance	TYP	100	Kohms	
Converter Idle Current ON/OFF Pin Low	TYP	<1	mA	
Isolation (3)				
Isolation Voltage Input to Output 10 µA Leakage	MIN	700	VDC	
Input to Output Capacitance	TYP	300	pF	
Output Trim Function				
Input Resistance	TYP	20	Kohms	
Open Circuit Voltage	MIN	±5	%	
Environmental				
Case Operating Range, Tc No Derating	MIN	-40	i C	
	MAX	90		
Storage Range	MIN	-55	i C	
	MAX	105		
Thermal Impedance (5)	TYP	10	i C/Watt	
General				
MTBF (Calculated)	TYP	800,000	HRS	
Unit Weight	TYP	2/57	oz/gm	
Chassis Mounting Kit	CM2A1			



Mechanical tolerances unless otherwise noted:
X.XX dimensions: ±0.020 inches
X.XXX dimensions: ±0.005 inches

Pin	Function
1	+INPUT
2	-INPUT
3	ON/OFF
4	NO PIN
5	+OUT
6	-OUT
7	TRIM

Notes

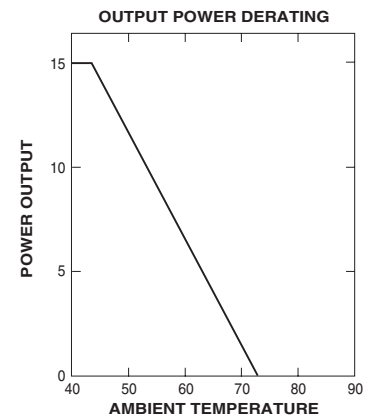
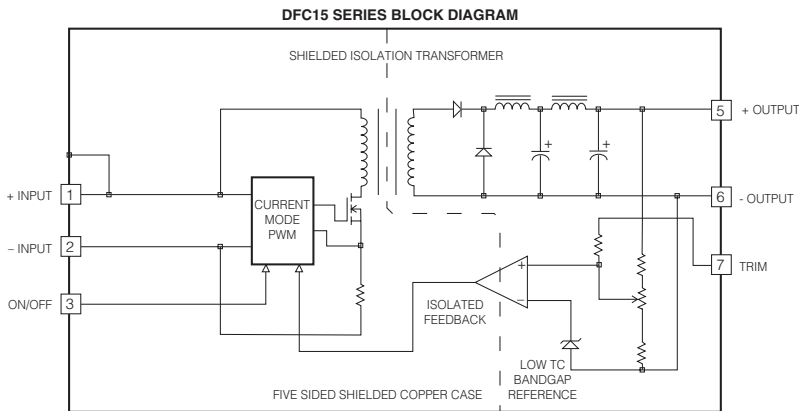
- (1) All parameters measured at Tc = 25°C, nominal input voltage and full rated load unless otherwise noted.
- (2) The ON/OFF pin is the Open Collector TTL, CMOS, and relay compatible. The input to this pin is referenced to Pin 2 (-Input) and is protected to +75VDC.
- (3) The Case is tied to Pin 3, +Input pin.
- (4) The case thermal impedance is specified as the case temperature rise over ambient per package watt dissipated.

Input Parameters (1)						
Model		DFC15U48S5	DFC15U48S12	DFC15U48S15	Units	
Voltage Range	MIN	20.0			VDC	
	TYP	48.0				
	MAX	60.0				
Input Current	Full Load	TYP	950	915	905	mA
	No Load	TYP	2	4	4	
Efficiency	TYP	79	82	83	%	
Switching Frequency	TYP	120			kHz	
Maximum Input Overvoltage, 100ms No Damage	MAX	75			VDC	
Turn-on Time, 1% Output Error	TYP	5	10		ms	

Output Parameters (1)					
Model		DFC15U48S5	DFC15U48S12	DFC15U48S15	Units
Output Voltage		5	12	15	VDC
Rated Load (3)	MIN	0	0	0	mA
	MAX	3000	1250	1000	
Voltage Range 100% Load	MIN	4.95	11.90	14.90	VDC
	TYP	5.00	12.00	15.00	
	MAX	5.05	12.10	15.10	
Load Regulation 25-100% Full Load	TYP	0.5	0.1	0.1	%
	MAX	0.75	0.2	0.2	
Line Regulation Vin = Min-Max VDC	TYP	0.1	0.01	0.01	%
	MAX	0.15	0.1	0.1	
Short Term Stability (4)	TYP	< 0.02			%/24Hrs
Long Term Stability	TYP	< 0.05			%/kHrs
Input Ripple Rejection (5)	TYP	> 60			dB
Noise, 0-20MHz bw (2)	TYP	75	60	60	mV _{pp}
RMS Noise	TYP	3	2	2	mV _{rms}
Temperature Coefficient	TYP	50			ppm/°C
	MAX	150			
Short Circuit Protection +OUT to -OUT	Continuous Current Limit				

Notes

- (1) All Parameters measured at Tc=25°C, nominal input voltage and full rated load unless otherwise noted.
- (2) Noise measurement bandwidth is 0-20 MHz. RMS noise is measured over a 0.01-1 MHz bandwidth. To simulate standard PCB decoupling practices, output noise is measured with a 1µF/35V tantalum capacitor located 1 inch away from the converter.
- (3) Minimum load required for rated regulation only. Dynamic response may degrade if run at less than 25% full load.
- (4) Short term stability is specified after a 30-minute warmup at full load, and with constant line, load and ambient conditions.
- (5) The input ripple rejection is specified for DC to 120 Hz ripple with a modulation amplitude of 1% Vin.



DFC15 Series Application Notes:

External Capacitance Requirements

No external capacitance is required for operation of the DFC15 Series. However, for maximum performance, it is recommended that the DFC15 Series use a capacitor of sufficient ripple current capacity connected across the input pins if a capacitive input source is farther than 1" from the converter. To meet the reflected ripple requirements of the converter, an input impedance of less than 0.05 Ohms from DC to 200 kHz is required. External output capacitance is not required for operation, however it is recommended that 1 μ F to 10 μ F of tantalum and 0.001 to 0.1 μ F ceramic capacitance be selected for reduced system noise. Additional output capacitance may be added for increased filtering, but should not exceed 400 μ F.

Negative Outputs

A negative output voltage may be obtained by connecting the +OUT to circuit ground and connecting -OUT as the negative output.

Remote ON/OFF Operation

The remote ON/OFF pin may be left floating if this function is not used. It is recommended to drive this pin with an open collector arrangement or a relay contact. When the ON/OFF pin is pulled low with respect to the -INPUT, the converter is placed in a low power drain state. Do not drive this input from a logic gate directly; there is a 100 kV internal pull-up resistor to a 9 volt source.

Output Trim

The TRIM pin may be used to adjust the output \pm 5% from the nominal setting. This function allows adjustment for voltage drops in the system wiring, as well 5.2 volt outputs for ECL applications. Figure 1 shows the proper connections to use this function. A trimpot value of 10 kV should be used for 5 volt outputs. A trimpot value of 20 kV should be used for 12 and 15 volt outputs. If the TRIM function is not required, the pin may be left floating.

Typical Performance: (Tc=25°C, Vin=Nom VDC, Rated Load)

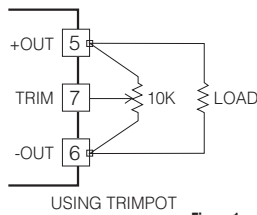
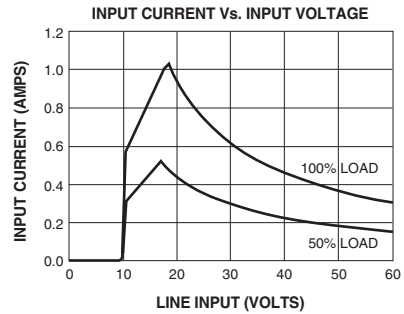
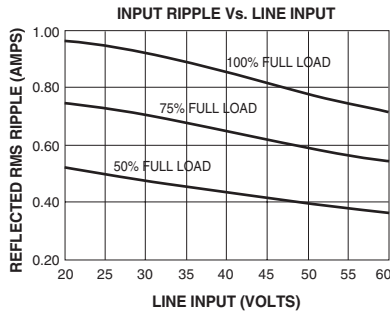
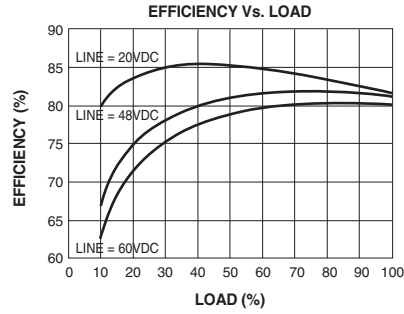
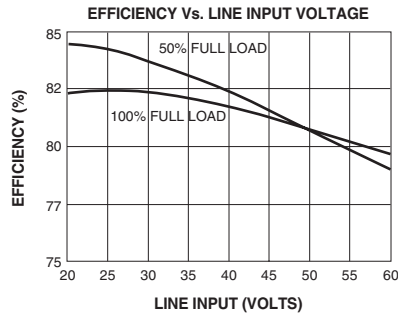
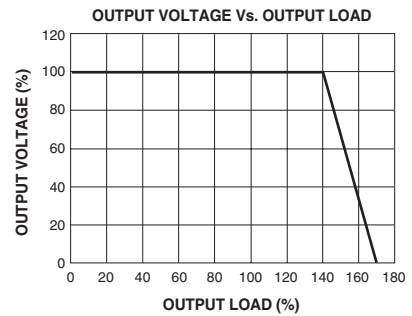
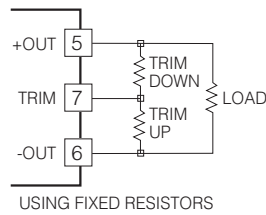


Figure 1.



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