Product Technical Specification and Customer Design Guidelines

AirPrime WMP50/100/150, WMP100/150 Embedded SIM with Open AT Framework

SIERRA WIRELESS®

4111967
15.0
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Document History

Version	Date	Updates
001	April 15, 2008	Creation
002	May 29, 2008	Update
003	June 27, 2008	Update
004	July 3, 2008	Update
005	November 17, 2008	Update (memory shielded content)
006	August 6, 2010	Updated exception as “Except for resistor R,”. Added new cautionary note regarding the Load signal on GPIO31.Added features of EDGE-Rx capable and optional embedded SIM (ESIM). Added subsection 2.1.6 to illustrate the WMP family.
007	September 8, 2010	Changed instances of SM3 to ESIM throughout the document.
		Updated section 3.22.4.1 Super Capacitor.
008	September 21, 2010	Changed instances of ESIM to Embedded SIM throughout the document.
		Updated Table 104 Applicable Standards and Requirements for the WMP Series Embedded Module.
009	September 30, 2010	Added CE mark in section 8.2 Standards and Recommendations.
010	August 02, 2011	Updated Table 83 Power Consumption without Open AT Framework (Typical Values).
		Added additional external interrupt pins in: • Section 3.19 External Interrupt • Table 15 SPI1 Pin Description and Table 16 SPI2 Pin Description • Table 20 UART1 Pin Description • Table 21 UART2 Pin Description • Table 22 SIM Interface Pin Description • Table 27 GPIO Pin Description • Table 78 Pin Description of Data and Address Signal • Table 88 Pin-out Labeling of Module
		Added ATEX compliance information: • Updated sections 8.3.2.7 and 8.3.2.8 for ATEX compliant modules. • Added section 8 ATEX Specifications
	August 19, 2011	Updated the crystal reference from MS2V-T1S to MS3V-T1R in section 3.21 Real Time Clock
011	February 8, 2012	Updated document reference number. Updates the Safety and Hazards, Limitations of Liability, Patents, Copyright, and Trademarks sections of the manual’s legal boilerplate. Updated Table 104: Applicable Standards and Requirements for the WMP Series Embedded Module.

Version	Date	Updates
12.0	September 24, 2012	Updated legal boilerplate content. Updated reset values for CTS2 and RXD2 from “Z” to “0”. Corrected the PTS to clarify that the following features are not available on the AirPrime WMP50 module: • Digital Audio PCM • I^2C • SPI2 • DAC • CS2 and CS3 • ADC2 and ADC3 • inSIM test Corrected the following GPIO-related information regarding the AirPrime WMP50 module: • 11 GPIOs are available on the WMP50, from GPIO0 through GPIO10 • GPIOs 15, 26, 27, 32, 35, 37, and 41 are not multiplexed. • GPIOs 25 and 46 do not exist. • INTs 0 and 1 are not multiplexed. • Present Ground and Reserved pin-out lists for this and WMP100/150 modules in separate tables as they differ.
13.0	September 11, 2013	Added Figure 95 ATEX Certificate LCIE 11 ATEX 3025 U / 01
		Updated: • Section 2.1.2 Environment and Mechanics • Figure 96 ATEX Logo • 8.2 ATEX Directive and Related Norms
14.0	July 07, 2014	Updated section 8 ATEX Specifications
15.0	September 23, 2014	Removed ATEX certification; moved section 8.3 to section 5.7 Conformance with ATEX 94/9/CE Directive

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1. Reference

1.1. Reference Documents

For more details, several documents are referenced in this specification. The Sierra Wireless documents references herein are provided in the Sierra Wireless documentation package; the general reference documents which are not owned by Sierra Wireless are not provided in the documentation package.

1.1.1. Sierra Wireless Reference Documentation

Note that the following software manual references are for Open AT Framework 2.0, though any version of Open AT Framework from 2.0 on is applicable. Refer to your software package to determine the current version being used and for the applicable manuals. Download documentation from Developer Zone (www.developer.sierrawireless.com) if needed.

[1] AirPrime WMP Series Product Technical Specification and Customer Design Guidelines

Reference: 4111967

[2] AirPrime WMP Series Development Kit User Guide

Reference: WM_DEV_WMP150_UGD_001

[3] Open AT Framework AT Commands Interface Guide for Firmware 7.0 or later

Reference: 4111703; 4111843

[4] Manufacturing Guidelines

Reference: WM_PGM_WUP_UGD_001

[5] DWLWin Download Application User Guide

Reference: WM_DEV_TOO_UGD_010

[6] ADL User Guide for Open AT Framework OS 6.00 or later

Reference: 4111704; 4111844

Please refer to the latest documentations on the Sierra Wireless Developer Zone at http://developer.sierrawireless.com.

1.1.2. General Reference Documentation

[7] "I^2C Bus Specification", Version 2.0, Philips Semiconductor 1998

[8] ISO 7816-3 Standard

1.2. List of Abbreviations

Table 1. Abbreviation Definitions

Abbreviation	Definition
AC	Alternative Current
ADC	Analog to Digital Converter
A/D	Analog to Digital conversion
AF	Audio-Frequency
AT	ATtention (prefix for modem commands)
AUX	AUXiliary
CAN	Controller Area Network
CB	Cell Broadcast
CEP	Circular Error Probable
CLK	CLocK
CMOS	Complementary Metal Oxide Semiconductor
CS	Coding Scheme
CTS	Clear To Send
DAC	Digital to Analogue Converter
dB	Decibel
DC	Direct Current
DCD	Data Carrier Detect
DCE	Data Communication Equipment
DCS	Digital Cellular System
DR	Dynamic Range
DSR	Data Set Ready
DTE	Data Terminal Equipment
DTR	Data Terminal Ready
EFR	Enhanced Full Rate
E-GSM	Extended GSM
EMC	ElectroMagnetic Compatibility
EMI	ElectroMagnetic Interference
EMS	Enhanced Message Service
EN	ENable
ESD	ElectroStatic Discharges
FIFO	First In First Out
FR	Full Rate
FTA	Full Type Approval
GND	GrouND
GPI	General Purpose Input
GPC	General Purpose Connector
GPIO	General Purpose Input Output
GPO	General Purpose Output
GPRS	General Packet Radio Service
GPS	Global Positioning System

Abbreviation	Definition
GSM	Global System for Mobile communications
HR	Half Rate
I/O	Input / Output
JTAG	Joint Test Action Group
LED	Light Emitting Diode
LNA	Low Noise Amplifier
MAX	MAXimum
MIC	MICrophone
MIN	MINimum
MMS	Multimedia Message Service
MO	Mobile Originated
MT	Mobile Terminated
na	Not Applicable
NF	Noise Factor
NMEA	National Marine Electronics Association
NOM	NOMinal
NTC	Négative Temperature Coefficient
PA	Power Amplifier
Pa	Pascal (for speaker sound pressure measurements)
PBCCH	Packet Broadcast Control CHannel
PC	Personal Computer
PCB	Printed Circuit Board
PDA	Personal Digital Assistant
PFM	Power Frequency Modulation
PSM	Phase Shift Modulation
PWM	Pulse Width Modulation
RAM	Random Access Memory
RF	Radio Frequency
RFI	Radio Frequency Interference
RHCP	Right Hand Circular Polarization
RI	Ring Indicator
RST	ReSeT
RTC	Real Time Clock
RTCM	Radio Technical Commission for Maritime services
RTS	Request To Send
RX	Receive
SCL	Serial CLock
SDA	Serial DAta
SIM	Subscriber Identification Module
SMS	Short Message Service
SPI	Serial Peripheral Interface
SPL	Sound Pressure Level
SPK	SPeaKer

Abbreviation	Definition
SW	SoftWare
PSRAM	Pseudo Static RAM
TBC	To Be Confirmed
TDMA	Time Division Multiple Access
TP	Test Point
TVS	Transient Voltage Suppressor
TX	Transmit
TYP	TYPical
UART	Universal Asynchronous Receiver-Transmitter
USB	Universal Serial Bus
USSD	Unstructured Supplementary Services Data
VSWR	Voltage Standing Wave Ratio
WMP	Wireless MicroProcessor

2. General Description

2.1. General Information

The AirPrime WMP50/100/150 and WMP100/150 Embedded SIM Intelligent Embedded Modules are self-contained E-GSM/GPRS 900/1800 and 850/1900 quad-band embedded modules, including the characteristics listed in the subsection below. In addition, they are EDGE-Rx capable except for the WMP50.

WMP100 Embedded SIM and WMP150 Embedded SIM are the Embedded SIM versions of WMP100 and WMP150 respectively. It allows usage of two different SIMs, an external SIM and an embedded SIM. The embedded SIM application has to be personalized by a card-maker.

The module is a hybrid integrated circuit, combination of some passive elements (resistors, capacitors, inductances, etc.) obtained by thin- or thick-film technology, some active elements (diodes, transistors, monolithic integrated circuits with multiple processing CPU cores, etc.) obtained by semiconductor technology, and discrete components, combined to all intents and purposes indivisibly by interconnections or interconnecting cables, on a single insulating substrate in epoxy.

2.1.1. Physical Dimension and Weight

- Length: 25 mm
- Width: 25 mm
- Thickness: 3.65 mm for WMP50, WMP100, and WMP100 Embedded SIM
  3.78 mm for WMP150 and WMP150 Embedded SIM
- Weight: 4.25 g
- Package: WMBGA576 / ball Ø 0,6 mm @ pitch 1mm

Caution: *The thickness of WMP100 module is, at current size, 3.65mm. Sierra Wireless recommends that customers consider the fact that in future releases, the WMP100 module could increase up to 3.78 mm.*

2.1.2. Environment and Mechanics

- Green policy: Restriction of Hazardous Substances in Electrical and Electronic Equipment (RoHS) compliant
- Complete shielding

The modules are compliant with RoHS Directive 2011/65/EU which sets limits for the use of certain restricted hazardous substances. This directive states that “from 1st July 2006, new electrical and electronic equipment put on the market does not contain lead, mercury, cadmium, hexavalent chromium, polybrominated biphenyls (PBB) or polybrominated diphenyl ethers (PBDE)”.

2.1.3. GSM/GPRS/EDGE-RX Features

- 2 Watts EGSM 900/GSM 850 radio section running under 3.6 Volts
- 1 Watt GSM1800/1900 radio section running under 3.6 Volts
- Hardware GPRS class 10 capable
- Hardware EDGE-Rx class 10 capable

2.1.4. Interface

- Digital section running under 2.8 Volts and 1.8Volts
- 3V/1V8 SIM interface
- 1.8V Parallel interface for devices (memories, LCD, etc.)
- Power supplies
- Watchdog
- Serial links (UART)
- Analogue audio
- ADC / DAC
- PCM digital audio
- Keyboard
- USB 2.0 slave
- Serial buses (I^2C,SPI)
- PWM (BUZZER)
- GPIOs
- SIM (external SIM and optional embedded SIM)

2.1.5. Operating System

- Real Time Clock with calendar
- Echo Cancellation + noise reduction (quadri codec)
- Full GSM or GSM/GPRS/EDGE-Rx Operating System stack

2.1.6. AirPrime WMP Series

Table 2. RF Band Supported by the AirPrime WMP Series Modules

Product Reference (MKT Name)	Part Number	RF Band
WMP50	WMP50	EGSM / GPRS CL 10 850 / 900 / 1800 /1900 MHz
WMP100	WMP100	EGSM / GPRS CL 10 / EDGE-Rx CL 10 850 / 900 / 1800 /1900 MHz
WMP100 Embedded SIM	WMP100 Embedded SIM	EGSM / GPRS CL 10 / EDGE-Rx CL 10 850 / 900 / 1800 /1900 MHz
WMP150	WMP150	EGSM / GPRS CL 10 / EDGE-Rx CL 10 850 / 900 / 1800 /1900
WMP150 Embedded SIM	WMP150 Embedded SIM	EGSM / GPRS CL 10 / EDGE-Rx CL 10 850 / 900 / 1800 /1900

Note: WMP50 is not Edge-Rx capable.

2.2. Functional Description

The global architecture of module is described below:

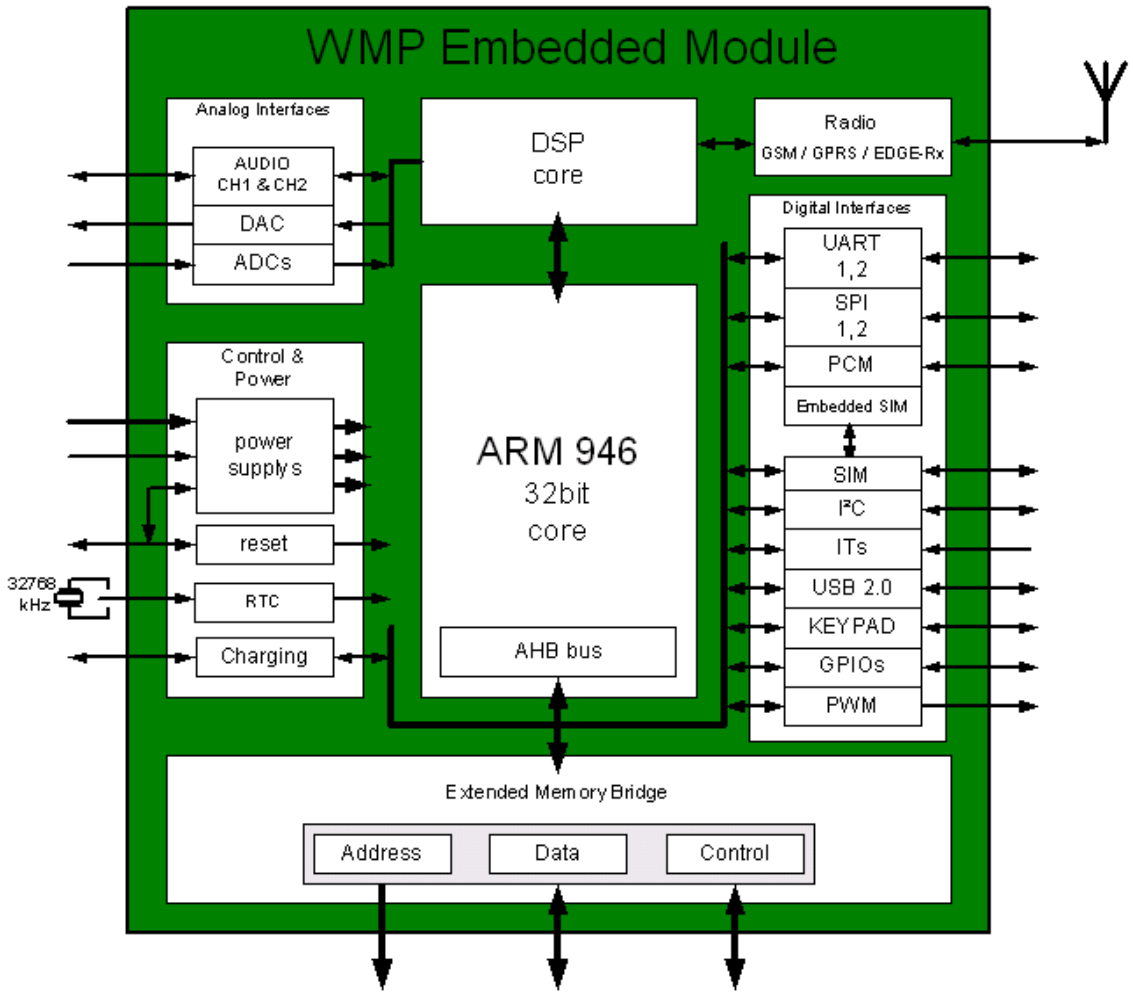


Figure 1. Functional Architecture of WMP Embedded Module

Note: WMP50 is not Edge-Rx capable.

2.2.1. RF Functionalities

The Radio Frequency (RF) range complies with the Phase II EGSM 900/DCS 1800 and GSM 850/PCS 1900 recommendation. The frequencies are listed in the table below.

Table 3. RF Functionalities

	Transmit band (Tx)	Receive band (Rx)
GSM 850	824 to 849 MHz	869 to 894 MHz
E-GSM 900	880 to 915 MHz	925 to 960 MHz
DCS 1800	1710 to 1785 MHz	1805 to 1880 MHz
PCS 1900	1850 to 1910 MHz	1930 to 1990 MHz

The RF part is based on a specific quad band chip including:

- a Digital low-IF receiver
- a Quad-band LNAs (Low Noise Amplifier)
- an Offset PLL (Phase Locked Loop) transmitter
- a Frequency synthesizer
- a Digitally controlled crystal oscillator (DCXO)
- a Tx/Rx FEM (Front-End Module) for quad-band GSM/GPRS/EDGE-Rx

2.2.2. Baseband Functionalities

The Baseband is composed of an ARM9, a DSP and an analog element (with audio signals, I/Q signals, ADC, DAC).

The ARM clock is programmable up to 104MHz. The DSP clock is at 78MHz. The External Bus Interface clock is set-up to 26MHz.

The core power supply is to 1.8 volts. The digital power supply is to 2.8v.

2.3. Software Description

The Open AT Framework 2.0 is the software package that supports the modules of WMP50, WMP100, WMP150, WMP100 Embedded SIM, and WMP150 Embedded SIM. It consists of:

- A Firmware which drives the module thanks to an AT command interface over a serial port or USB
- An Operating System (OS) which runs various types of applications (telematics, multimedia, metering, alarm, automotive, etc.)
- An Integrated Development Environment (IDE) which builds and debugs applications over the Operating System
- Several Libraries which are software provided by Sierra Wireless that are able to run over the Operating System

3. Interfaces

3.1. General Interfaces

The modules are provided with a “Wireless Microprocessor Development Kit” containing access to all the interfaces.

The available interfaces are listed in the table below.

Table 4. Available Interfaces

Name	Driven by AT Commands	Open AT Framework 2.0
Serial Interface		✓
Parallel Interface (on Memory interface)		✓
Keyboard Interface	✓	✓
Main Serial Link	✓	✓
Auxiliary Serial Link	✓	✓
SIM Interface	✓	✓
General Purpose IO	✓	✓
Analog to Digital Converter	✓	✓
Digital to Analog Converter	✓	✓
Analog audio Interface	✓	✓
Buzzer Output	✓	✓
Battery Charging Interface	✓	✓
External Interruption	✓	✓
BAT-RTC (Backup Battery)	✓	✓
LED0 signal	✓	✓
Digital Audio Interface (PCM)	✓	✓
USB 2.0 Interface	✓	✓
External Bus Interface (Memory Interface)	✓	✓

3.2. Power Supply

3.2.1. Power Supply Description

The power supply is one of the key elements in the design of a GSM terminal.

The module is powered by a single power supply VBATT. This power supply feeds two inputs to the supply, VBATT-BB and VBATT-RF.

VBATT-RF powers all the radio components of the module. It has to be carefully designed because most of the current is transmitted through this input. The VBATT-RF current is bursted due to the GSM/GPRS transmission protocol.

VBATT-BB supplies the digital part of the module. VBATT-BB is directly connected to the internal power management unit of the module. This unit controls the VBATT-BB voltage and provides the power supplies like VCC_1V8 and VCC_2V8.

Note: The VBATT-BB input generates noise, so the VBATT can be filtered by a band reject filter.

3.2.2. Power Supply Constraints on VBATT-RF

Due to the bursted emission in GSM/GPRS, the power supply must be able to deliver high current peaks in a short time. During the peaks the ripple (U_{ripp}) on the supply voltage must not exceed a certain limit (see Table 5 Operating Voltage for details).

- In communication mode, a GSM/GPRS class 2 terminal emits 577µs radio bursts every 4.615ms. (See Figure 2 below.)
- In communication mode, a GPRS class 10 terminal emits 1154µs radio bursts every 4.615ms.

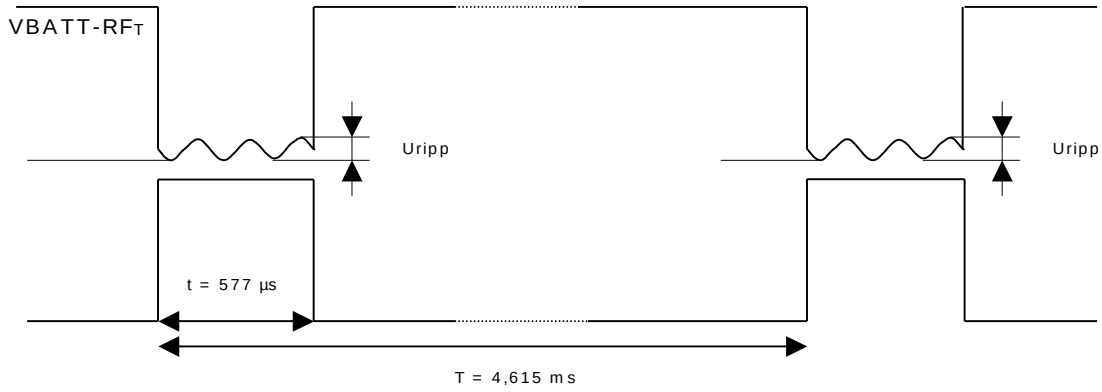


Figure 2. Power Supply During Burst Emission

VBATT-RF:

- Supplies the RF components with 3.6 V directly. It is essential to keep a minimum voltage ripple at this connection in order to avoid any phase error.

  The RF Power Amplifier current (1.5 A peak in GSM /GPRS mode) flows with a ratio of:
  - 1/8 of the time (around 577µs every 4.615ms for GSM /GPRS cl. 2) and
  - 2/8 of the time (around 1154µs every 4.615ms for GSM /GPRS cl. 10) with the rising time is around 10µs.
- It is recommended to add an external decoupling capacitor of 33 pF close to the VBATT-RF input.

3.2.3. Power Supply Constraints on VBATT

The VBATT-BB input is used as well as to supply the module core as well as to monitor the level voltage of VBATT.

VBATT-BB is internally connected to several regulators and to a switching regulator which provides the VCC_1V8 voltage internally. Because the switching regulator generates perturbation on the VBATT signal, it is recommended to add an external reject filter between VBATT and VBATT-BB.

3.2.4. Electrical Characteristics

Table 5. Operating Voltage

	V_{MIN}[4]	V_{NOM}	V_{MAX}	$I_{TYP.}$	I_{MAX}	Ripple max (U_{ripp})
VBATT-BB[1]	3.2	3.6	4.8	0.1 A	0.3 A	100mV[3]
VBATT-RF[1,2]	3.2	3.6	4.8	1.4 A	1.5 A	See following table

(1): This value has to be guaranteed during the burst (with 1.5A Peak in GSM or GPRS mode)

(2): Maximum operating Voltage Stationary Wave Ratio (VSWR) 2:1

(3): Take the VBATT-RF ripple max in consideration only if you use the same power supply for VBATT-RF and VBATT-BB.

(4): The minimum start-up voltage must be 3.3V for WMP100 Embedded SIM and WMP150 Embedded SIM.

Note: The Embedded SIM versions of WMP modules require at least 3.3V start-up voltage.

When powering the module with a battery, the total impedance (battery + protections + PCB) should be < 150 mΩ.

As the radio power amplifier is directly connected to the VBATT, the module is sensitive to any voltage variation. When a DC/DC converter is used, Sierra Wireless recommends setting the converter frequency so that the resulting voltage does not exceed the values given in the following table "Maximum voltage ripple (U_{ripp}) versus Frequency".

Table 6. Maximal Voltage Ripple (U_{ripp}) Versus Frequency

Freq. (kHz)	U_{ripp} Max (mVpp)	Freq. (kHz)	U_{ripp} Max (mVpp)	Freq. (kHz)	U_{ripp} Max (mVpp)
<100	96	800	27	1500	>60
200	51	900	67	1600	>60
300	37	1000	67	1700	>60
400	15	1100	>60	1800	>60
500	54	1200	>60	>1900	>60
600	21	1300	>60		
700	55	1400	>60		

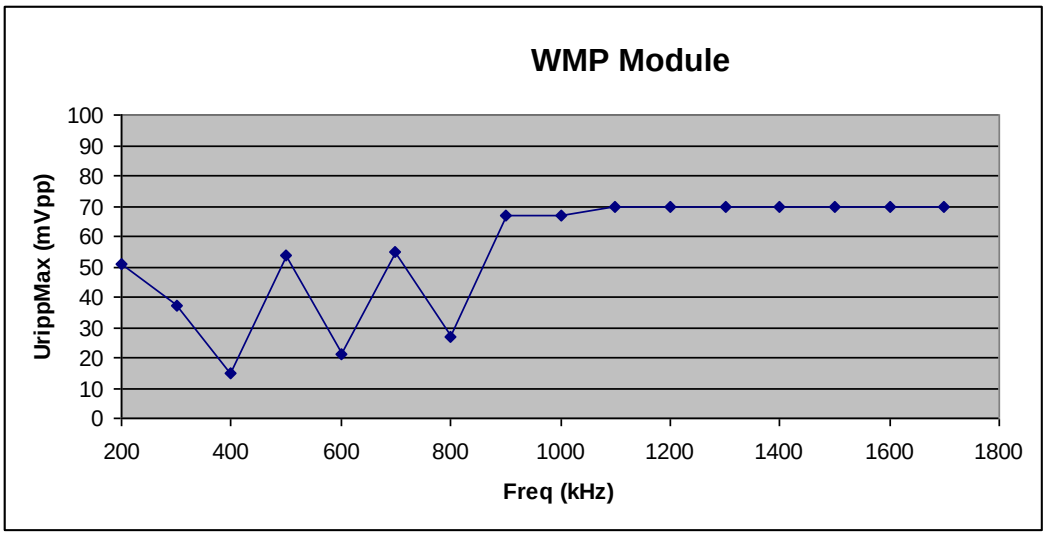


Figure 3. Maximum Voltage Ripple (U_{ripp}) Versus Frequencies in GSM & DCS

3.2.5. Pin Description

Table 7. VBATT Pin Description

Signal	Pin Number
VBATT-BB	AC1,AC2,AD1,AD2
VBATT-RF	A12,A13,A14,B12,B13,B14

3.2.6. Application

The reject filter can be connected between VBATT and VBATT-BB. A decoupling capacitor C3 on VBATT-RF input is recommended.

Caution: *If the reject filter (C1+L1+C2) is an option, a capacitor (i.e.C2) is mandatory close to the VBATT-BB balls.*

The reject filter (C1+L1+C2) is mandatory for application with power supply cable longer than 3m.

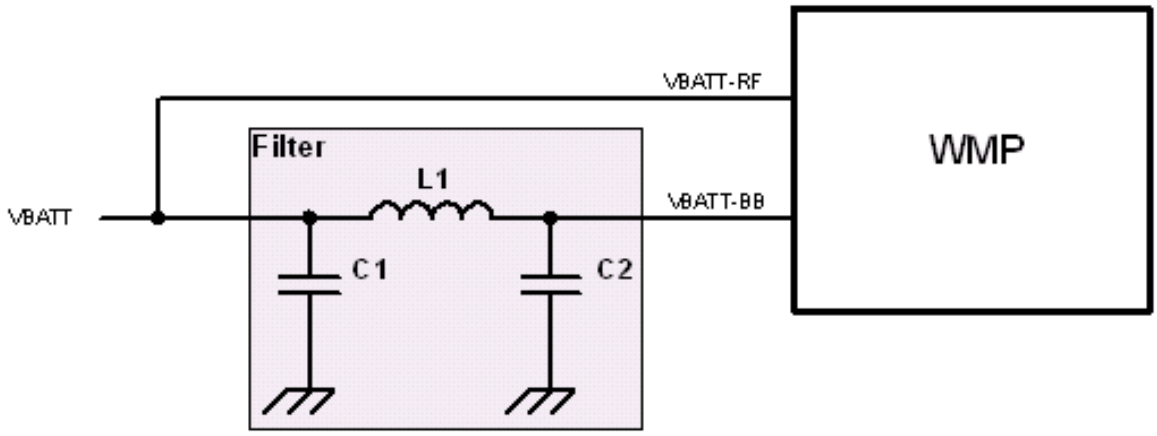


Figure 4. Reject Filter Diagram

Recommended Components

C1, C2: 10µF +/-20%

- GRM21BR60J106KE19L from MURATA
- CM21X5R106M06AT from KYOCERA
- JMK212BJ106MG-T from TAYO YUDEN
- C2012X5R0J106MT from TDK

C3: 33pF +/-5% (COG)

- GRM1555C1H330JZ01J from MURATA
- CM05CG330J50AH from KYOCERA
- CC0402JPNPO9BN330 from YAGEO
- MCH155A330JK from ROHM

L1: 220nH +/-5%

- 0805CS-221XJLC from COILCRAFT
- 0805G221J E from STETCO

3.3. Electrical Information for Digital I/O

There are three types of digital I/O on the WMP module:

- 2.8Volt CMOS
- 1.8Volt CMOS
- Open drain

I/Os concerned are all interfaces like GPIOs, SPIs, Keypad, etc.

Refer to the tables below for the electrical characteristics of these three digital I/Os.

Table 8. Electrical Characteristic of a 2.8V Digital I/O

Parameter		I/O Type	Minimum	Typical	Maximum	Condition
Internal 2.8V power supply		VCC_2V8	2.74V	2.8V	2.86V	
Input / Output pin	V_{IL}	CMOS	-0.5V*		0.84V	
	V_{IH}	CMOS	1.96V		3.2V*	
	V_{OL}	CMOS			0.4V	I_{OL} = - 4 mA
	V_{OH}	CMOS	2.4V			I_{OH} = 4 mA
	I_{OH}				4mA	
	I_{OL}				- 4mA	

(*): Absolute maximum ratings

All 2.8V I/O pins do not accept input signal voltages above the maximum voltage specified above; except for the UART1 interface, which is 3.3V tolerant.

Table 9. Electrical Characteristic of a 1.8V Digital I/O

Parameter		I/O Type	Minimum	Typical	Maximum	Condition
Internal 1V8 power supply		VCC_1V8	1.76V	1.8V	1.94V	
Input / Output pin	V_{IL}	CMOS	-0.5V*		0.54V	
	V_{IH}	CMOS	1.33V		2.2V*	
	V_{OL}	CMOS			0.4V	I_{OL} = - 4 mA
	V_{OH}	CMOS	1.4V			I_{OH} = 4 mA
	I_{OH}				4mA	
	I_{OL}				- 4mA	

(*): Absolute maximum ratings

Table 10. Electrical Characteristic of Open Drain Output Type Digital I/O

Signal name	Parameter	I/O Type	Minimum	Typical	Maximum	Condition
LED0	V_{OL}	Open Drain			0.4V	
	I_{OL}	Open Drain			8mA	

Signal name	Parameter	I/O Type	Minimum	Typical	Maximum	Condition
BUZZER0	V_{OL}	Open Drain			0.4V	
	I_{OL}	Open Drain			100mA	
SDA1 and SCL1	V_{TOL}	Open Drain			3.3V	Tolerated voltage
	V_{IH}	Open Drain	2V			
	V_{IL}	Open Drain			0.8V	
	V_{OL}	Open Drain			0.4V	
	I_{OL}	Open Drain			3mA	

The reset states of each I/O are given in their corresponding interface's section descriptions. The state definitions are defined below:

Table 11. Reset State Definition

Parameter	Definition
0	Set to GND
1	Set to supply 1V8 or 2V8 depending of I/O type
Pull down	Internal pull down with ~60K resistor.
Pull up	Internal pull up with ~60K resistor to supply 1V8 or 2V8 depending of I/O type.
Z	High impedance
Undefined	Undefined must not be used in an application if a special state is required at reset. These pins may be toggling a signal(s) during reset.

3.4. SPI Bus

The AirPrime WMP100 and WMP150 modules provide two SPI buses (i.e. for LCD, memories, etc.). The WMP50 provides only one, SPI1 (and not SPI2).

Note: The AirPrime WMP50 does not offer SPI2 and only has one SPI bus as a result.

3.4.1. Features

- a CLK signal
- an I/O signal
- an I signal
- a CS signal complying with standard SPI bus (any GPIO)
- an optional LOAD signal (only the SPIx-LOAD signal)

3.4.1.1. Characteristics

- Master mode operation
- The CS signal must be any GPIO
- The LOAD signal (optional) is used for the word handling mode (only the SPIx-LOAD signal)
- The SPI speed is from 102 Kbit/s up to 13 Mbit/s in master mode operation

- 3 or 4-wire interface (5-wire possible with the optional SPIx-LOAD signal)
- SPI-mode configuration: 0 to 3
- 1 to 16 bits data length

3.4.1.2. SPI Configuration

Table 12. SPI Bus Configuration

Operation	Maximum Speed	SPI-Mode	Duplex	3-wire Type	4-wire Type	5-wire Type
Master	13 Mb/s	0,1,2,3	Half	SPIx-CLK; SPIx-IO; GPIOx as CS	SPIx-CLK; SPIx-IO; SPIx-I; GPIOx as CS	SPIx-CLK; SPIx-IO; SPIx-I; GPIOx as CS; SPIx-LOAD (not muxed in GPIO);

For the 3-wire configuration, SPIx-I/O is used as input and output.

For the 4-wire configuration, SPIx-I/O is used as output only, SPIx-I is used as input only.

For the 5-wire configuration, SPIx-I/O is used as output only, SPIx-I is used as input only. And the dedicated SPIx-LOAD signal is used. It is an additional signal in more than a Chip Select (any other GPIOx)

3.4.1.3. SPI Waveforms

The figure below shows the waveforms for SPI transfers with a 4-wire configuration in master mode 0.

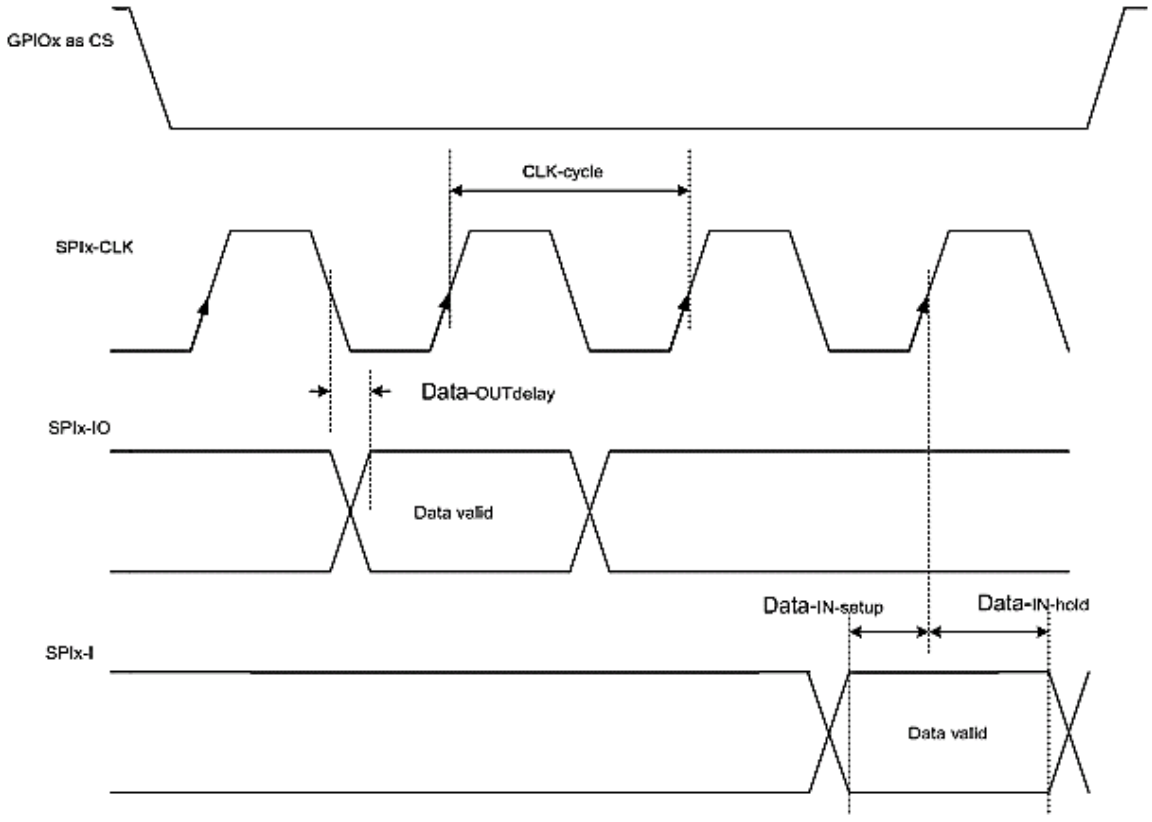


Figure 5. SPI Timing Diagram (Mode 0, Master, 4 wires)

Table 13. SPI Bus AC Characteristics

Signal	Description	Minimum	Typical	Maximum	Unit
CLK-cycle	SPI clock frequency	0.102		13	MHz
Data-OUT delay	Data out ready delay time			10	ns
Data-IN-setup	Data in setup time	2			ns
Data-OUT-hold	Data out hold time	2			ns

The following figure shows the waveform for SPI transfer with the LOAD signal configuration in master mode 0 (chip select is not represented).

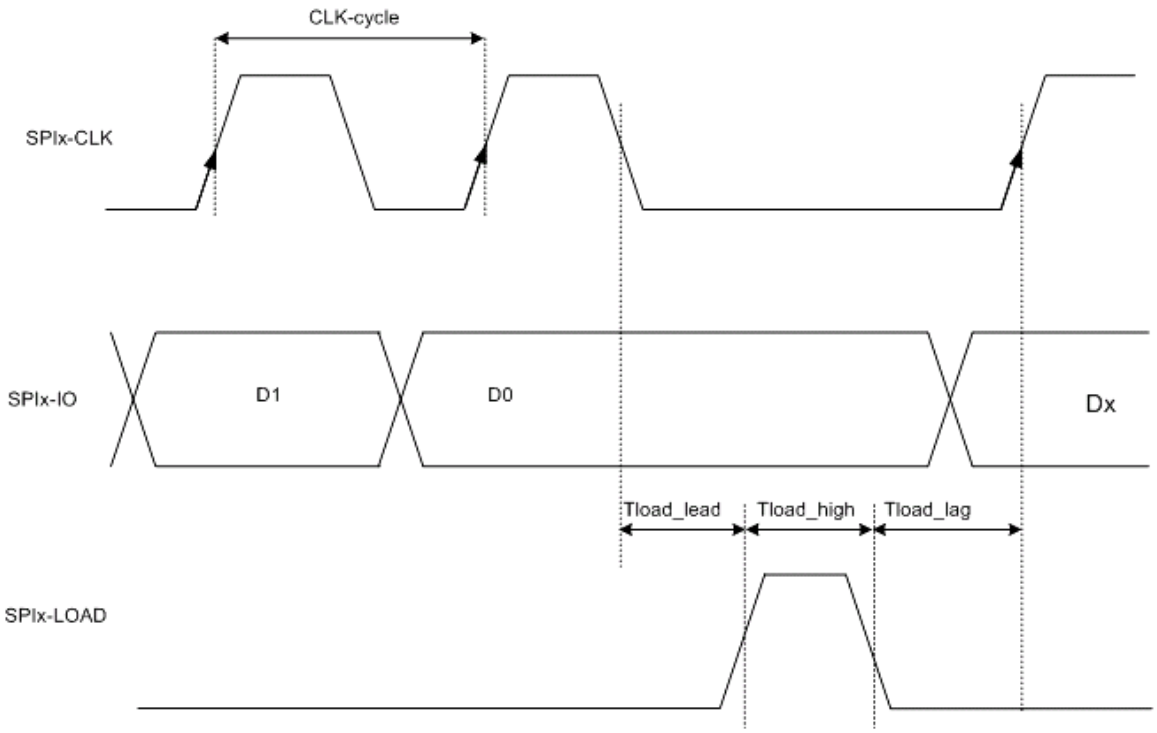


Figure 6. SPI Timing Diagram with LOAD Signal (Mode 0, Master, 4 wires)

Table 14. SPI Bus AC Characteristics With Load

Signal	Description	Minimum	Typical	Maximum	Unit
CLK-cycle	SPI clock frequency	0.102		13	MHz
Tload_lead	SPI-LOAD lead time after SPI-CLK falling edge		TCLK-cycle/2		ns
Tload_high	SPI-LOAD high time		TCLK-cycle/2		ns
Tload_lag	SPI-LOAD lag time before SPI-CLK rising edge		TCLK-cycle/2		ns

3.4.2. Pin Description

Table 15. SPI1 Pin Description

Signal	Pin Number	I/O	I/O Type	Reset State	Description	Multiplexed with
SPI1-CLK	U15	O	2V8	Z	SPI Serial Clock	GPIO28
SPI1-IO	V12	I/O	2V8	Z	SPI Serial input/output	GPIO29
SPI1-I	R13	I	2V8	Z	SPI Serial input	GPIO30
SPI1-LOAD	M14	O	2V8	Z	SPI load	GPIO31* / INT5**

Refer to section 3.3, "Electrical Information for Digital I/O" for Open drain, 2V8 and 1V8 voltage characteristics and for Reset state definition.

** The multiplexed interrupt pin is only applicable to the WMP100 and WMP150 embedded module variant. Refer to section 3.19, External Interrupt for more information about interrupt pins and their multiplexes.

Caution: *(*): If the Load signal is configured for use, then GPIO31 is not available for use as Chip Select and will result in a bus subscription error by the ADL.*

Table 16. SPI2 Pin Description (for WMP100 and WMP150 only)

Signal	Pin Number	I/O	I/O Type	Reset State	Description	Multiplexed with
SPI2-CLK	R15	O	2V8	Z	SPI Serial Clock	GPIO32
SPI2-IO	M13	I/O	2V8	Z	SPI Serial input/output	GPIO33
SP2-I	U16	I	2V8	Z	SPI Serial input	GPIO34
SPI2-LOAD	T18	O	2V8	Z	SPI load	GPIO35 / INT4**

Refer to section 3.3, "Electrical Information for Digital I/O" for Open drain, 2V8 and 1V8 voltage characteristics and for Reset state definition.

** The multiplexed interrupt pin is only applicable to the WMP100 and WMP150 embedded module variant. Refer to section 3.19, External Interrupt for more information about interrupt pins and their multiplexes.

3.4.3. Application

3.4.3.1. 3-wire Interface

When used in 3-wire interface (SPI bus), only the line SPIx-IO is used for output and input data.

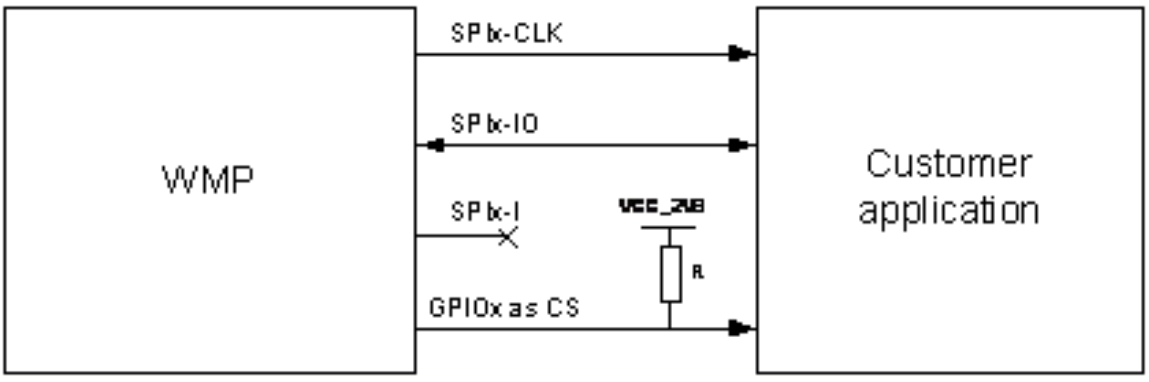


Figure 7. Example of a 3-wire SPI Bus Application

The SPIx-I line is not used in 3-wire configuration. This line can be left opened or used as GPIO for different application functionality.

One pull up resistor R is needed to set the CS level during the reset state. Except for R, no external component is needed if the electrical specification of the customer application complies with the module SPIx interface electrical specification.

The SPIx interface voltage range is 2.8V. It can be powered by the VCC_2V8 (ball R1) of the module or by another power supply.

Note that R value depends on the peripheral plugged on the SPIx interface.

3.4.3.2. 4-wire Interface

The particularity of the 4-wire serial interface (SPI bus) is that the input and the output data lines are dissociated. The SPIx-IO signal is used only for data output and the SPIx-I signal is used only for data input.

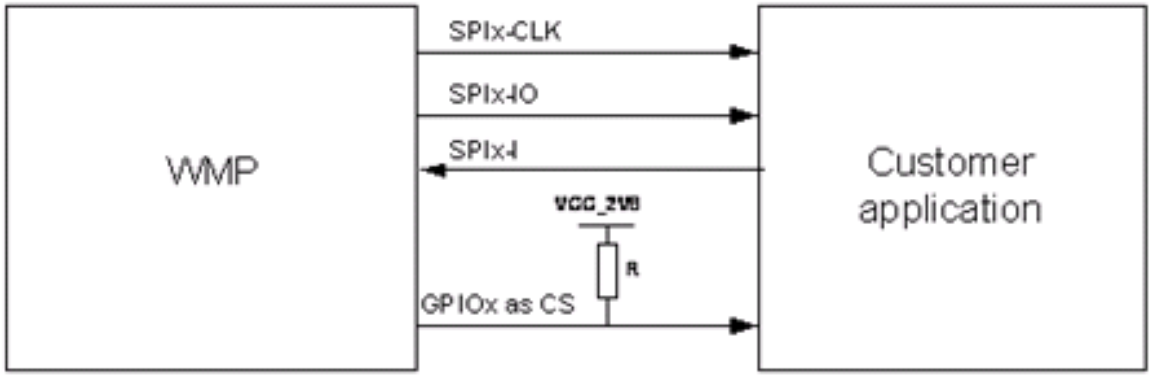


Figure 8. Example of a 4-wire SPI Bus Application

One pull up resistor R is needed to set the CS level during the reset state.

Except for R, no external component is needed if the electrical specification of the customer application complies with the module SPIx interface electrical specification.

3.4.3.3. 5-wire Interface

The particularity of the 5-wire serial interface (SPI bus) is the same configuration than the 4-wire interface but the dedicated signal (SPIx-LOAD) is added.

This dedicated signal may be necessary for some slave devices to validate or load data. It may be generated after each word including the last word of a transmission.

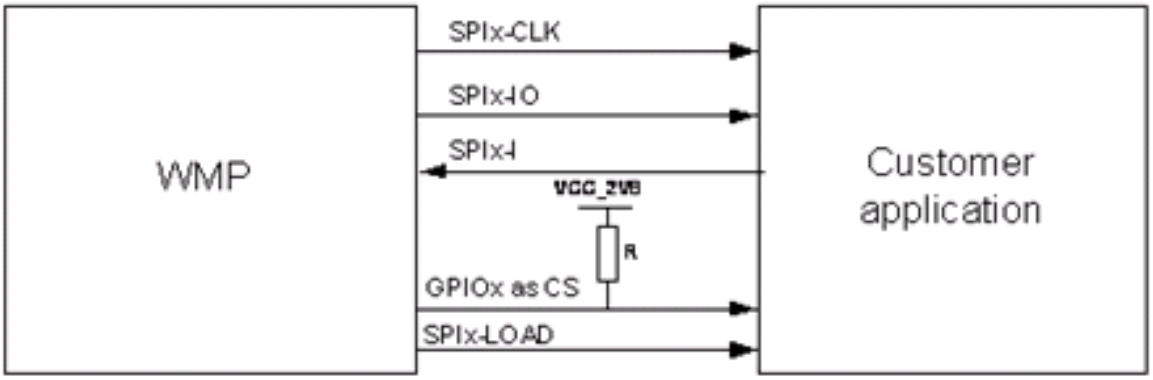


Figure 9. Example of 5-wire SPI Bus Application (with SPIx-LOAD Signal)

One pull up resistor R is needed to set the CS level during the reset state.

Except for resistor R, no external component is needed if the electrical specification of the customer application complies with the module SPIx interface electrical specification.

3.5. I²C Bus

3.5.1. Features

The I²C interface includes a clock signal (SCL) and a data signal (SDA) complying with a 100Kbit/s-standard interface (standard mode: s-mode).

Note: The AirPrime WMP50 does not offer I²C functionality. I²C (including the SCL and SDA signals) applies only to the WMP100 and WMP150 modules.

3.5.1.1. Characteristics

The I²C bus is always master.

The maximum speed transfer range is 400Kbit/s (Fast mode: f-mode).

For more information on the bus, refer to document [7] "I2C Bus Specification", Version 2.0, Philips Semiconductor 1998.

3.5.1.2. I²C Waveforms

The figure below shows I²C bus waveform in master mode configuration.

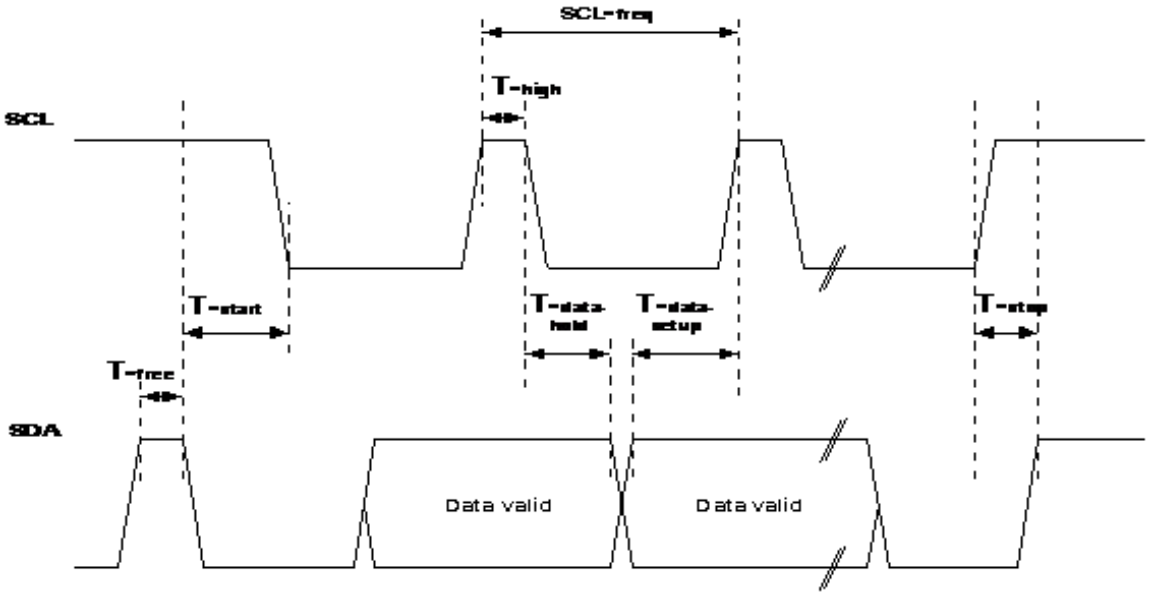


Figure 10. I²C Timing Diagram (Master)

Table 17. I²C AC Characteristics

Signal	Description	Minimum	Typical	Maximum	Unit
SCL-freq	I²C clock frequency	100		400	KHz

Signal	Description	Minimum	Typical	Maximum	Unit
T-start	Hold time START condition	0.6			µs
T-stop	Setup time STOP condition	0.6			µs
T-free	Bus free time, STOP to START	1.3			µs
T-high	High period for clock	0.6			µs
T-data-hold	Data hold time	0		0.9	µs
T-data-setup	Data setup time	100			ns

3.5.2. Pin Description

Table 18. I²C Pin Description for WMP100 and WMP150

Signal	Pin Number	I/O	I/O Type	Reset State	Description	Multiplexed with
SCL	AA15	O	Open drain	Z	Serial Clock	GPIO26
SDA	AA16	I/O	Open drain	Z	Serial Data	GPIO27

Refer to section 3.3, "Electrical Information for Digital I/O" for Open drain, 2V8 and 1V8 voltage characteristics and for Reset state definition.

Note: The AirPrime WMP50 does not offer I²C functionality. I²C (including the SCL and SDA signals) applies only to the WMP100 and WMP150 modules.

3.5.3. Application

The two lines need to be pull up to the V_{I^2C} voltage. The V_{I^2C} voltage is dependent on the customer application component connected on the I²C bus. Nevertheless, the V_{I^2C} must complying with the module electrical specification (3.3V Max).

The VCC_2V8 (ball R1) of the module can be used to connect the pull up resistors, if the I²C bus voltage is 2.8 V.

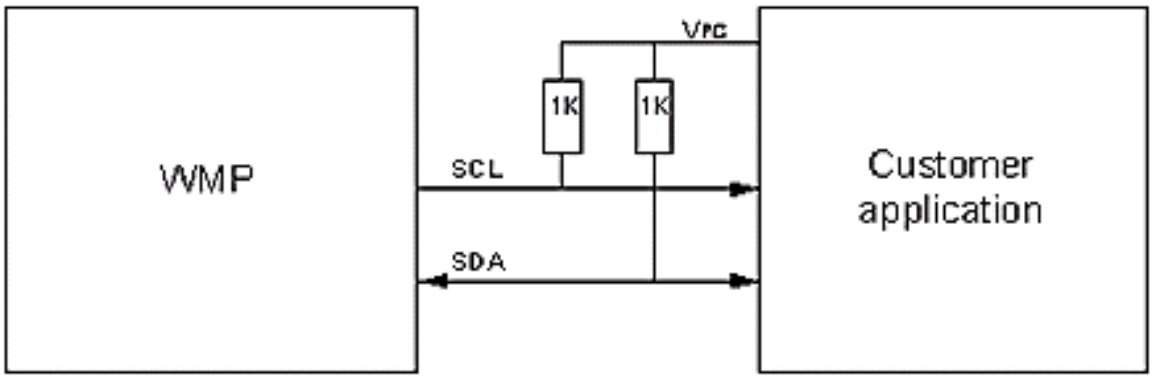


Figure 11. First Example of an I²C Bus Application

The I²C bus is complying with the Standard mode (baud rate 100Kbit/s) and the Fast mode (baud rate 400Kbit/s). The pull up resistor value choice depends on the mode used. For the Fast mode, it is recommended to use 1K ohm resistor to ensure the compliance with the I²C specification. For the Standard mode, higher values of resistors can be used to save power consumption.

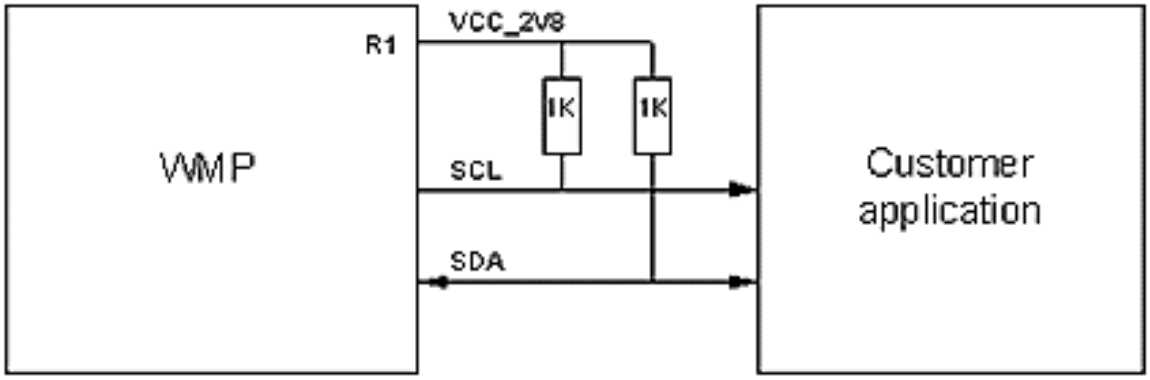


Figure 12. Second Example of an I^2C Bus Application

3.6. Keyboard Interface

3.6.1. Features

This interface provides 10 connections:

- 5 rows (ROW0 to ROW4)
- 5 columns (COL0 to COL4)

The scanning is digital, and the debouncing is performed in the module.

The keyboard scanner is equipped with the following:

- Internal pull-down resistors for the rows
- Pull-up resistors for the columns

Current only flows from the column pins to the row pins. This allows a transistor to be used in place of the switch for power-on functions.

3.6.2. Pin Description

Table 19. Keyboard Interface Pin Description

Signal	Pin Number	I/O	I/O Type	Reset State	Description	Multiplexed with
ROW0	AC23	I/O	1V8	0	Row scan	GPIO9
ROW1	AD22	I/O	1V8	0	Row scan	GPIO10
ROW2	AD21	I/O	1V8	0	Row scan	GPIO11
ROW3	AC22	I/O	1V8	0	Row scan	GPIO12
ROW4	AD23	I/O	1V8	0	Row scan	GPIO13
COL0	AD19	I/O	1V8	Pull up	Column scan	GPIO4
COL1	AD20	I/O	1V8	Pull up	Column scan	GPIO5
COL2	AC20	I/O	1V8	Pull up	Column scan	GPIO6
COL3	AC19	I/O	1V8	Pull up	Column scan	GPIO7

Signal	Pin Number	I/O	I/O Type	Reset State	Description	Multiplexed with
COL4	AC21	I/O	1V8	Pull up	Column scan	GPIO8

Refer to section 3.3, "Electrical Information for Digital I/O" for Open drain, 2V8 and 1V8 voltage characteristics and for Reset state definition.

With the Open AT Framework 2.0, the set of multiplexed signals become unavailable for other purposes when the keyboard service is used. In the same way, if one or more GPIOs (of this table) are allocated, the keyboard service is unavailable.

3.6.3. Application

Keypad matrix application allows for up to 25 keys.

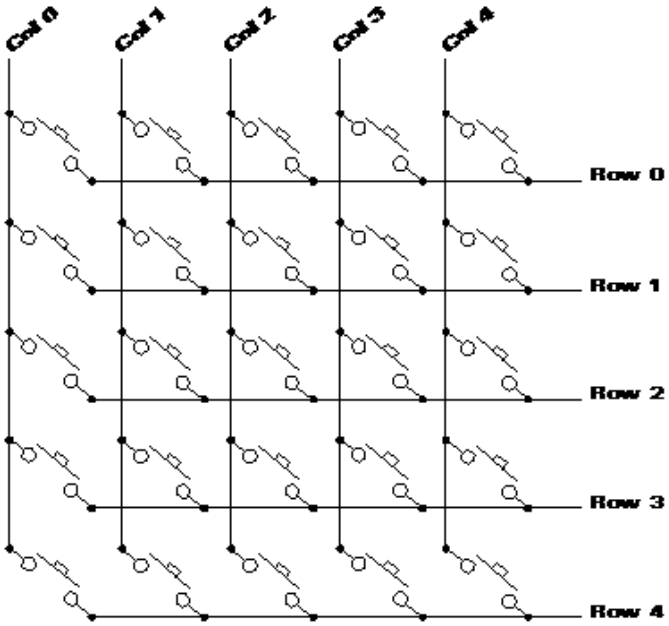


Figure 13. Example of a 25-key keyboard Implementation

3.7. Main Serial Link (UART1)

A flexible 8-wire serial interface is available complying with V24 protocol signaling but not with V28 (electrical interface) due to a 2.8 Volts interface.

3.7.1. Features

The maximum baud rate of the UART1 is 921 Kbit/s.

The signals used by UART1 are as follows:

- TX data (CT103/TX)
- RX data (CT104/RX)
- Request To Send (~CT105/RTS)
- Clear To Send (~CT106/CTS)

- Data Terminal Ready (~CT108-2/DTR)
- Data Set Ready (~CT107/DSR)
- Data Carrier Detect (~CT109/DCD)
- Ring Indicator (~CT125/RI)

3.7.2. Pin Description

Table 20. UART1 Pin Description

Signal	Pin Number	I/O	I/O Type	Reset State	Description	Multiplexed with
CT103/TXD1*	R17	I	2V8	Z	Transmit serial data	GPIO36
CT104/RXD1*	T13	O	2V8	1	Receive serial data	GPIO37 / INT2/INT9**
~CT105/RTS1*	Y18	I	2V8	Z	Request To Send	GPIO38
~CT106/CTS1*	N15	O	2V8	Z	Clear To Send	GPIO39
~CT107/DSR1*	T12	O	2V8	Z	Data Set Ready	GPIO40
~CT108-2/DTR1*	M16	I	2V8	Z	Data Terminal Ready	GPIO41 / INT3/INT10**
~CT109/DCD1 *	AB16	O	2V8	Undefined	Data Carrier Detect	GPIO43
~CT125/RI1 *	AA18	O	2V8	Undefined	Ring Indicator	GPIO42
CT102/GND*	AA19		GND		Ground	

Refer to section 3.3, "Electrical Information for Digital I/O" for Open drain, 2V8 and 1V8 voltage characteristics and for Reset state definition.

(*): According to PC view

** The multiplexed interrupt pin varies depending on the WMP embedded module variant. Refer to section 3.19, External Interrupt for more information about interrupt pins and their multiplexes.

With the Open AT Framework 2.0 when the UART1 service is used the whole multiplexed signals become unavailable for other purposes. In the same way if one or more GPIOs (of this table) are allocated the UART1 service is unavailable.

The rising time and falling time of the reception signals (mainly CT103) have to be less than 300 ns.

The UART1 interface is 2.8V type, but it is 3V tolerant.

Tip: *The WMP series module is designed to operate using all the serial interface signals and it is recommended to use ~CT105/RTS1 and ~CT106/CTS1 for hardware flow control in order to avoid data corruption or loss during transmissions.*

3.7.3. 5-wire Serial Interface Hardware Design

The signals used in this interface are as follows:

- CT103/TXD1
- CT104/RXD1
- ~CT105/RTS1
- ~CT106/CTS1
- ~CT108-2/DTR1

The signal ~CT108-2/DTR1 must be managed following the V24 protocol signaling if slow (or fast) idle mode is to be used.

For more information, refer to document [3] Open AT Framework AT Commands Interface Guide for Firmware 7.0 or later.

3.7.4. 4-wire Serial Interface Hardware Design

The signals used in this interface are as follows:

- CT103/TXD1
- CT104/RXD1
- ~CT105/RTS1
- ~CT106/CTS1

The signal ~CT108-2/DTR1 must be configured at the low level.

For more information, refer to document [3] Open AT Framework AT Commands Interface Guide for Firmware 7.0 or later.

3.7.5. 2-wire Serial Interface Hardware Design

Caution: *Although this case is possible for a connected external chip, it is not recommended (and forbidden for AT command or modem use).*

The flow control mechanism has to be managed from the customer side. The signals used in this interface are as follows:

- CT103/TXD1
- CT104/RXD1

The signal ~CT108-2/DTR1and ~CT105/RTS1 must be configured at the low level

The signals ~CT105/RTS1 and ~CT106/CTS1 are not used; default hardware flow control on UART1 should be de-activated using AT command (**AT+IFC=0, 0)**.

The other signals and their multiplexed GPIOs are not available.

For more information, refer to document [3] Open AT Framework AT Commands Interface Guide for Firmware 7.0 or later.

3.7.6. First Download

A blank flash connected on the module can **only** be downloaded with a specific PC software tool provided by Sierra Wireless “DWLWIN” (using the dongle) for the first download. DWLWIN is pairing the WMP module with its flash. The downloaded firmware is then encrypted to only work with this flash.

For Open AT Framework application download, the pairing is not required anymore. DWLWIN (without dongle) or AT command can be used.

Customer should use the DWLWIN software tool on a PC connected to the UART1 of the module to download the software (firmware + customer application) on a blank flash. A dongle is needed for the first download. Dongle is a secured key (look like USB key) to connect on a PC when using the DWLWIN downloading tool. It is mandatory for customer when they first load the firmware onto the “blank” flash of their WMP system (to pair the flash ID with the module ID).

For production DWLWIN tool can be configured to download multiple modules at the same time Customer bench to be set-up to allow 10 by 10 unit downloading capability at the same time. This implies 10 UARTs access on a PC but single software.

Refer to document [5] DWLWin Download Application User Guide for more information.

That's mandatory that the UART1 is available for the first download, so it's necessary to be careful about the connectivity of the UART1 with others devices used in the application.

If no device is connected and there are no conflicts, the computer can be directly connected on the module through a RS232 level shifter.

When a device is used on UART1, allowing for the ability to unselect the device during the download is recommended (via the enable signal).

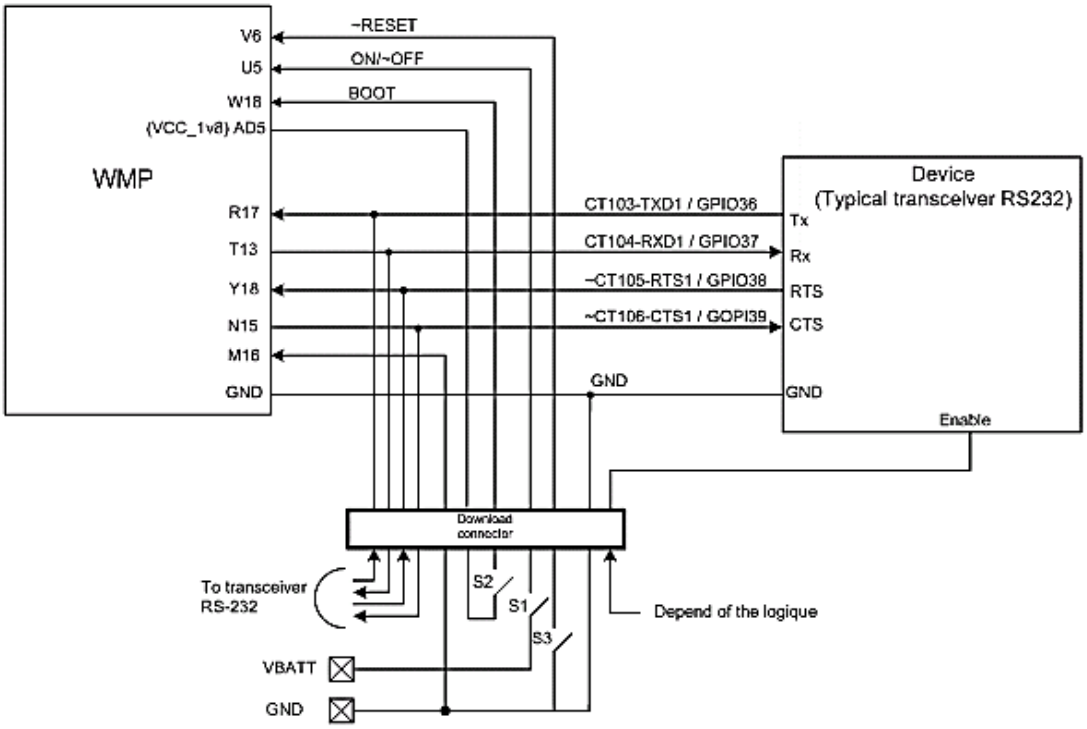


Figure 14. Example of UART1 Connection For Download With Another Device On The Link

The Download connector is directly connected on the four UART1 signals, which may create conflicts with the Device lines. For this reason an enable must be available on the device to set the device output signals at High impedance.

Note: In this configuration (4-wire), the signal ~CT108-2/DTR1 (ball M16) must be configured at the low level.

At the same time, to run the first download, the BOOT signal of the module must be driven. The switch **S2 must be closed** after the download started S2 can be open. Refer to section 3.17, BOOT Signal, for more information.

If the module is powered ON (VBATT present), **S1 must be closed** for enable the module.

Start the specific PC software tool provided by Sierra Wireless.

S3 must be closed* (a pulse to 0L during at least 200µs) for start the download. Refer to section 3.18, Reset Signals for more information.

(*): S3 can be not use if the condition on S1 and S2 are respected before than the power supply is applied. (There is in this case an automatic internal reset).

If a computer is used for the first download, a RS232 level shifter must be used (refer to the application with the ADM3307EACP in this chapter).

Note: XMODEM download can be launched only through the UART1, and the first download has to be launched with a specific PC software tool provided by Sierra Wireless "DWLWIN".

3.7.7. Application

The level shifter must be a 2.8V with V28 electrical signal compliance.

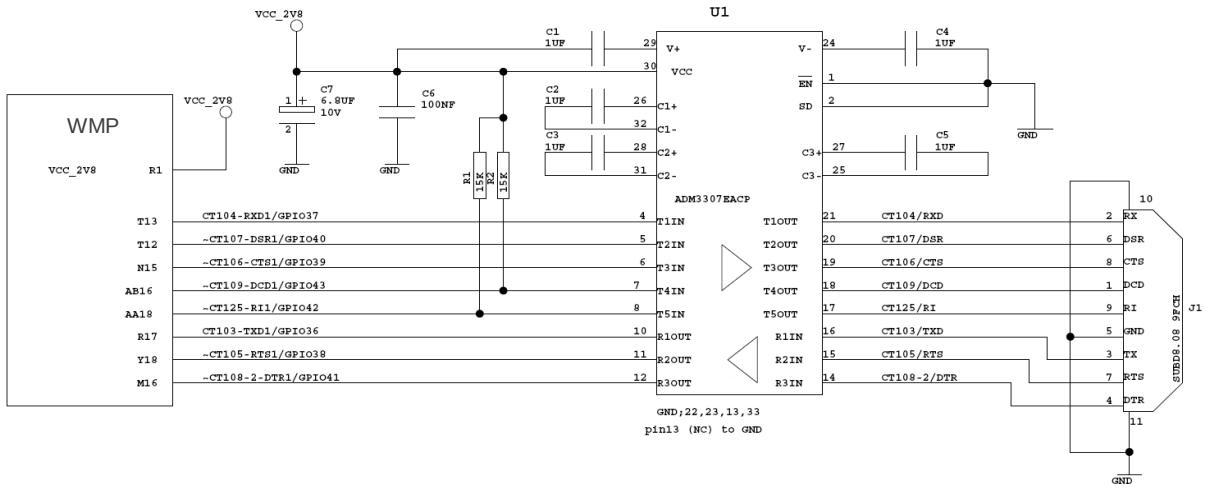


Figure 15. Example of RS-232 Level Shifter Implementation for UART1

Note: U1 chip also protects the WMP module against ESD at 15KV (air discharge).

Recommended Components

- R1, R2: 15kΩ
- C1, C2, C3, C4, C5: 1uF
- C6: 100nF
- C7: 6.8uF TANTAL 10V CP32136 from AVX
- U1: ADM3307EACP from ANALOG DEVICES
- J1: SUB-D9 female

R1 and R2 are necessary only during Reset state to forced ~CT1125-RI1 and ~CT109-DCD1 signal to high level.

The ADM3307EACP chip is able to speed up to **921Kb/s***. If others level shifters are used, ensured that their speed are compliant with the UART1 speed useful.

(*): For this baud rate the power supply must be provided by an **external regulator at 3.0 V**.

The ADM3307EACP can be powered by the VCC_2V8 (ball R1) of the module or by an external regulator at 2.8 V (the baud rate will be limited up to 720kbps).

If the UART1 interface is connected directly to a host processor, it is not necessary to used level shifters. The interface can be connected as shown below:

V24/CMOS Possible Design

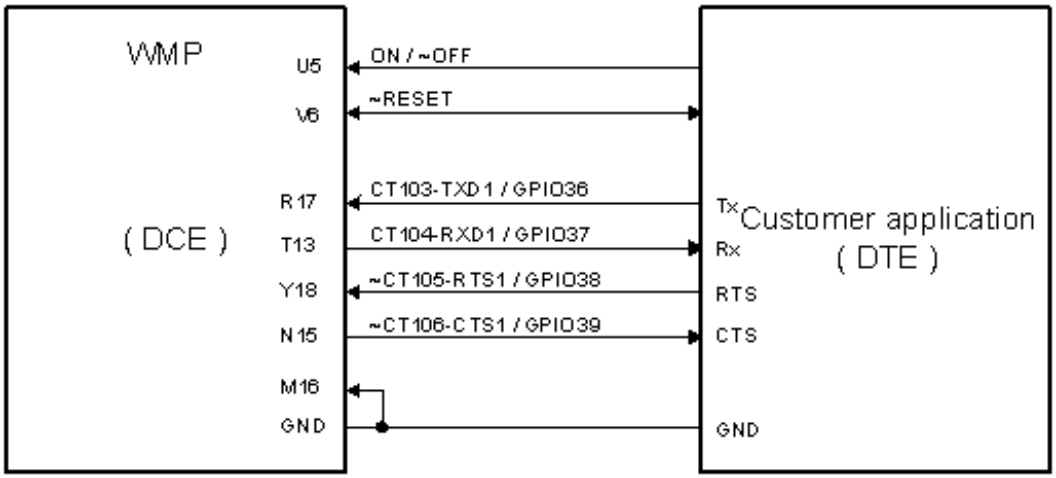


Figure 16. Example of V24/CMOS Serial Link Implementation for UART1

Note that the design shown in the above figure is a basic design and a more flexible design to access this serial link with all modem signals is shown below.

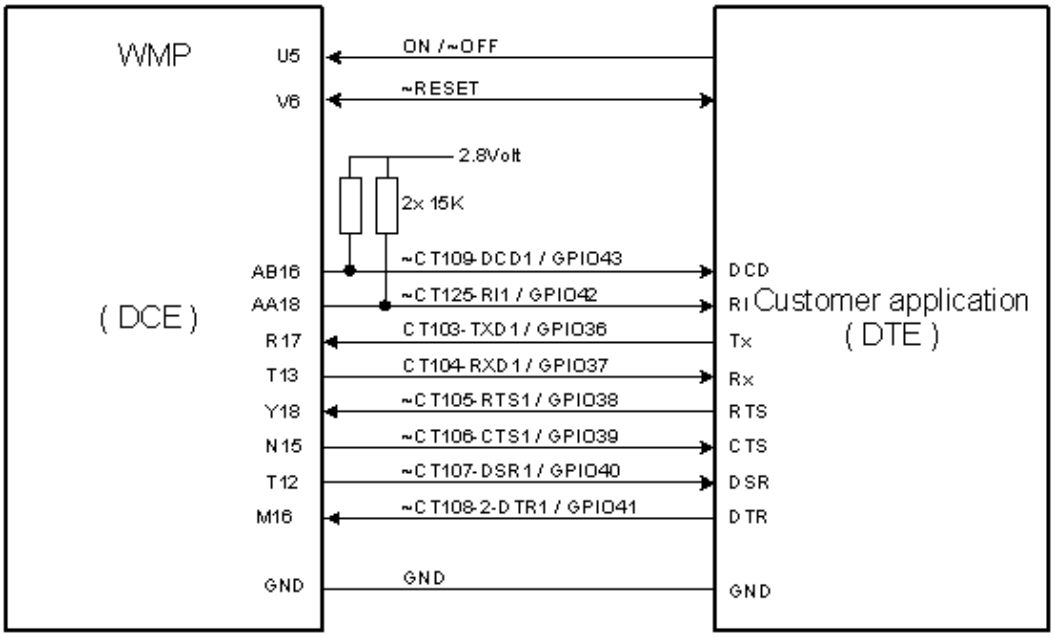


Figure 17. Example of Full Modem V24/CMOS Serial Link Implementation for UART1

It is recommended to add a 15kΩ pull-up resistor on ~CT125-RI1 and ~CT109-DCD1 to set high level during reset state.

The UART1 interface is 2.8 Volt type, but is 3 Volt tolerant.

Tip:	*WMP UART1 is designed to operate using all the serial interface signals. In particular, it is recommended to use RTS and CTS for hardware flow control in order to avoid data corruption during transmission.*

Caution:	*In case the Power Down mode (Sierra Wireless 32K mode) is to be activated using the Open AT Framework, the DTR pin must be wired to a GPIO. Refer to document [3] Open AT Framework AT Commands Interface Guide for Firmware 7.0 or later, for more information on Sierra Wireless 32K mode activation using the Open AT Framework.*

3.8. Auxiliary Serial Link (UART2)

An auxiliary serial interface (UART2) is available on the module. This interface may be used to connect a Bluetooth or a GPS chip controlled by an Open AT Framework Library.

3.8.1. Features

Maximum baud rate of the UART2 is 921 Kbit/s.

The signals used by UART2 are as follows:

- TX data (CT103/TX)
- RX data (CT104/RX)
- Request To Send (~CT105/RTS)
- Clear To Send (~CT106/CTS)

Tip: *WMP UART2 is designed to operate using all the serial interface signals. In particular, it is recommended to use RTS and CTS for hardware flow control in order to avoid data corruption during transmission.*

3.8.2. 2-Wire Serial Interface Hardware Design

Caution: *Although this case is possible for a connected external chip, it is not recommended (and forbidden for AT command or modem use).*

The flow control mechanism has to be managed at the customer side. The signals used in this interface are as follows:

- CT103/TXD2
- CT104/RXD2

The signals ~CT105/RTS2, ~CT106/CTS2 are not used, default hardware flow control on UART2 should be de-activated using AT command (AT+IFC=0, 0).

The signal ~CT105/RTS2 must be configured at the low level.

The other signals and their multiplexed GPIOs are not available.

For more information, refer to document [3] Open AT Framework AT Commands Interface Guide for Firmware 7.0 or later.

3.8.3. Pin Description

Table 21. UART2 Pin Description

Signal	Pin Number	I/O	I/O Type	Reset State	Description	Multiplexed with
CT103 / TXD2*	T16	I	1V8	Z	Transmit serial data	GPIO14 / INT6**
CT104 / RXD2*	U17	O	1V8	0	Receive serial data	GPIO15 / INT4/INT11**
~CT106 / CTS2*	W17	O	1V8	0	Clear To Send	GPIO16
~CT105 / RTS2*	V13	I	1V8	Z	Request To Send	GPIO17 / INT7**

Signal	Pin Number	I/O	I/O Type	Reset State	Description	Multiplexed with
CT102/GND*	V15		GND		Ground	

Refer to section 3.3, "Electrical Information for Digital I/O" for Open drain, 2V8 and 1V8 voltage characteristics and for Reset state definition.

(*): According to PC view

** The multiplexed interrupt pin varies depending on the WMP embedded module variant. Refer to section 3.19, External Interrupt for more information about interrupt pins and their multiplexes.

With the Open AT Framework 1.0, the set of multiplexed signals become unavailable for other purposes when the UART2 service is used. In the same way, if one or more GPIOs (of this table) are allocated the UART2 service is unavailable.

3.8.4. Application

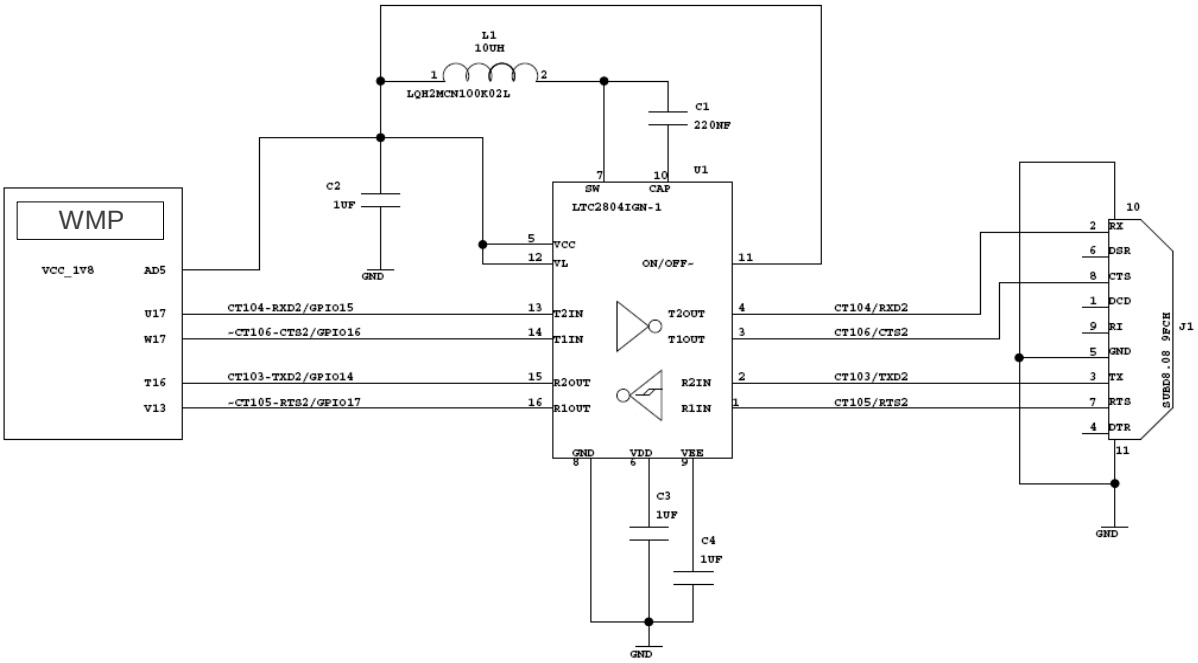


Figure 18. Example of RS-232 Level Shifter Implementation for UART2

Recommended Components

Capacitors

- C1 : 220nF
- C2, C3, C4 : 1µF

Inductor

- L1 : 10µH

RS-232 Transceiver

- U1 : LINEAR TECHNOLOGY LTC®2804IGN
- J1 : SUB-D9 female

The LTC2804 can be powered by the VCC_1V8 (ball AD5) of the module or by an external regulator at 1.8 V.

The UART2 interface can be connected directly to others components if the voltage interface is 1.8 V.

3.9. SIM Interface

WMP modules of Hardware Version 5.0 can provide two types of Subscriber Identification Module (SIM) application, the external SIM application and the optional embedded SIM application. For the external SIM application, it can be directly connected to the module through the SIM card interface. For the embedded SIM application, it is not necessary to connect a SIM card to the ball pins (Y1, Y2, Y3, W1, W2) so that it gives an advantage of BOM cost reduction. But it has to be personalized through these ball pins. An internal switch is managed by software to choose either internal or external SIM connection.

3.9.1. Features

The SIM interface controls a 3V / 1V8 SIM. This interface is fully compliant with GSM 11.11 recommendations concerning SIM functions.

The five signals used by this interface are as follows:

- SIM-VCC: SIM power supply
- ~SIM-RST: reset
- SIM-CLK: clock
- SIM-IO: I/O port
- SIMPRES: SIM card detect

3.9.2. Pin Description

Table 22. SIM Interface Pin Description

Signal	Pin Number	I/O	I/O Type	Reset State	Description	Multiplexed with
SIM-CLK	Y2	O	2V9 / 1V8	0	SIM Clock	Not mux
~SIM-RST	Y1	O	2V9 / 1V8	0	SIM Reset	Not mux
SIM-IO	W1	I/O	2V9 / 1V8	*Pull up	SIM Data	Not mux
SIM-VCC	W2	O	2V9 / 1V8		SIM Power Supply	Not mux
SIMPRES	Y3	I	1V8	Z	SIM Card Detect	GPIO18 / INT8**

(*): SIM-IO pull up is about 10K Ohm typically.

Refer to section 3.3, "Electrical Information for Digital I/O" for Open drain, 2V8 and 1V8 voltage characteristics and for Reset state definition.

** The multiplexed interrupt pin is only applicable to the WMP100 and WMP150 embedded module variant. Refer to section 3.19, External Interrupt for more information about interrupt pins and their multiplexes.

3.9.3. Electrical Characteristics

The following table refers to the electrical characteristics of the SIM interface.

Table 23. Electrical Characteristics of the SIM Interface

Parameter	Conditions	Minim.	Typ.	Maxim.	Unit
SIM-IO V_{IH}	I_{IH} = ± 20µA	0.7xSIMVCC			V
SIM-IO V_{IL}	I_{IL} = 1mA			0.4	V
~SIM-RST, SIM-CLK V_{OH}	Source current = 20µA	0.9xSIMVCC			V
SIM-IO V_{OH}	Source current = 20µA	0.8xSIMVCC			
~SIM-RST, SIM-IO, SIM-CLK V_{OL}	Sink current = -200µA			0.4	V
SIM-VCC Output Voltage	SIMVCC = 2.9V IVCC= 1mA	2.84	2.9	2.96	V
	SIMVCC = 1.8V IVCC= 1mA	1.74	1.8	1.86	V
SIM-VCC current	VBATT = 3.6V			10	mA
SIM-CLK Rise/Fall Time	Loaded with 30pF		20		ns
~SIM-RST, Rise/Fall Time	Loaded with 30pF		20		ns
SIM-IO Rise/Fall Time	Loaded with 30pF		0.7	1	µs
SIM-CLK Frequency	Loaded with 30pF			3.25	MHz

Note: When SIMPRES is used, a low to high transition means that a SIM card is inserted and a high to low transition means that the SIM card is removed.

3.9.4. Application

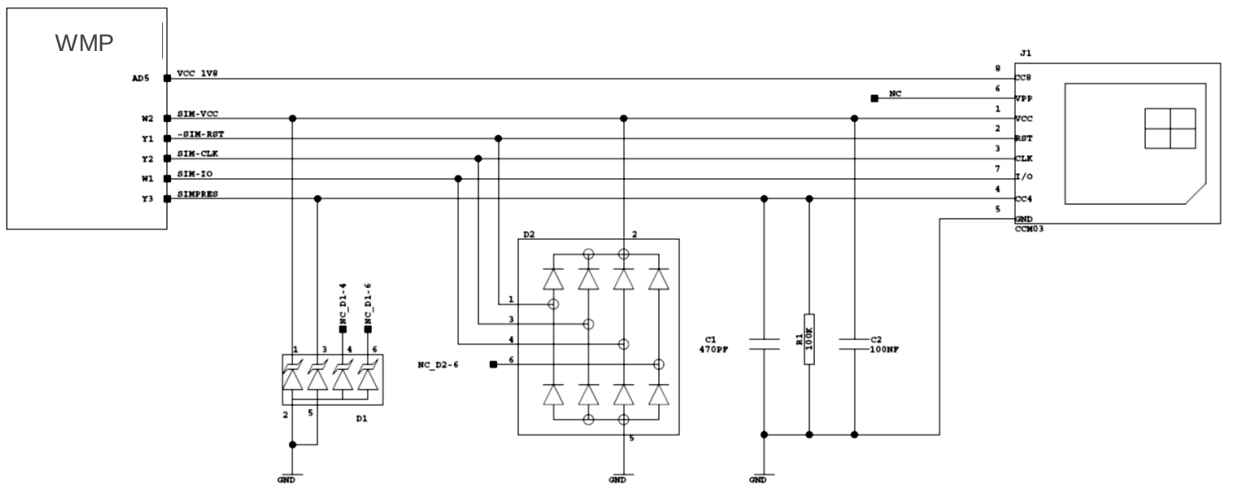


Figure 19. Example of a Typical SIM Socket Implementation

It is recommended to add Transient Voltage Suppressor diodes (TVS) on the signal connected to the SIM socket in order to prevent any Electrostatics Discharge.

TVS diodes with low capacitance (less than 10 pF) have to be connected on SIM-CLK signal and SIM-IO signal to avoid any disturbance of the rising and falling edge.

These types of diodes are mandatory for the Full Type Approval. They shall be placed as close as possible to the SIM socket.

Recommended Components

- R1 : 100K ohm
- C1 : 470pF
- C2 : 100nF

Note: C2 (100nF) should be as closed as possible to the SIM holder and must not exceed 330nF when placing on the SIM-VCC line.

- D1 : ESDA6V1SC6 from ST
- D2 : DALC208SC6 from SGS-THOMSON / ST Microelectronics
- J1 : ITT CANNON CCM03 series (Refer to section 6.2, Microphone for more information)

SIM Socket Connection

Table 24. SIM Socket Pin Description

Signal	Pin Number	Description
VCC	1	SIM-VCC
RST	2	~SIM-RST
CLK	3	SIM-CLK
CC4	4	SIMPRES with 100 kΩ pull down resistor and 470 pF capacitor
GND	5	GROUND
VPP	6	Not connected
I/O	7	SIM-IO
CC8	8	VCC_1V8 of WMP module (ball AD5)

3.9.5. Embedded SIM

WMP100 Embedded SIM and WMP150 Embedded SIM modules allow the selection of an external or embedded SIM by the software-controlled embedded switch. Open AT Framework 2.30 or later can drive the embedded switch automatically. The default configuration of the firmware is the external SIM. With the absence of the external SIM, it will be automatically switched to the embedded SIM. For each change of SIM selection by AT command, the module MUST be reset.

The embedded SIM personalization can be personalized by a card-maker through the external SIM interface of the module.

3.9.5.1. AT Commands for SIM Selection

To select internal or external SIM, AT+WHCNF command can be used.

Table 25. Useful AT Commands for SIM Selection

AT Command	Description
AT+WHCNF =4,0	External SIM preferred, default configuration

AT Command	Description
AT+WHCNF=4,1	External SIM
AT+WHCNF=4,2	Embedded SIM
AT+WHCNF=4,3	Get the embedded switch selected mode
AT+CFUN=1	Reset the mode

Note: After changing the mode, the module must be reset.

For more information, refer to document [3] Open AT Framework AT Commands Interface Guide for Firmware 7.0 or later.

3.10. General Purpose Input/Output

The WMP50 module provides up to 11, and the WMP100/150 modules provides up to 47 General Purpose I/Os. They are used to control any external device such as an LCD or a Keyboard backlight.

These GPIOs offer the possibility to read the pin state whatever their direction.

3.10.1. Features

Reset State:

- 0 : Set to GND
- 1: Set to supply 1V8 or 2V8 depending of I/O type.
- Pull down: Internal pull down with ~60K resistor.
- Pull up: Internal pull up with ~60K resistor to supply 1V8 or 2V8 depending of I/O type.
- Z: High impedance.
- Undefined: Be careful, undefined must not be used in your application if a special state at reset is needed. Those pins can be toggling signals.

3.10.2. Pin Description for AirPrime WMP50

Table 26. GPIO Pin Description for AirPrime WMP50

Signal	Pin Number	I/O	I/O Type	Reset State	Multiplexed with
GPIO0	AA17	I/O	2V8	Z	Not mux
GPIO1	Y13	I/O	2V8	Undefined	Not mux
GPIO2	AA13	I/O	2V8	Undefined	Not mux
GPIO3	M15	I/O	2V8	Z	Not mux
GPIO4	V17	I/O	2V8	Z	Not mux
GPIO5	N16	I/O	2V8	Z	Not mux
GPIO6	AA15	I/O	Open drain	Z	Not mux
GPIO7	AA16	I/O	Open drain	Z	Not mux
GPIO8	R15	I/O	2V8	Z	Not mux
GPIO9	T18	I/O	2V8	Z	Not mux
GPIO10	AB13	I/O	2V8	Undefined	32kHz buffered output clock

3.10.3. Pin Description for AirPrime WMP100/150

Table 27. GPIO Pin Description for AirPrime WMP100/150

Signal	Pin Number	I/O	I/O Type	Reset State	Multiplexed with
GPIO0	W15	I/O	1V8	0	Not mux
GPIO1	R18	I/O	1V8	Z	CS2 / A25
GPIO2	U22	I/O	1V8	Z	A24
GPIO3	V16	I/O	1V8	Z	INT0* / A26
GPIO4	AD19	I/O	1V8	Pull up	COL0
GPIO5	AD20	I/O	1V8	Pull up	COL1
GPIO6	AC20	I/O	1V8	Pull up	COL2
GPIO7	AC19	I/O	1V8	Pull up	COL3
GPIO8	AC21	I/O	1V8	Pull up	COL4
GPIO9	AC23	I/O	1V8	0	ROW0
GPIO10	AD22	I/O	1V8	0	ROW1
GPIO11	AD21	I/O	1V8	0	ROW2
GPIO12	AC22	I/O	1V8	0	ROW3
GPIO13	AD23	I/O	1V8	0	ROW4
GPIO14	T16	I/O	1V8	Z	CT103-TXD2 / INT6*
GPIO15	U17	I/O	1V8	0	CT104-RXD2 / INT4/INT11*
GPIO16	W17	I/O	1V8	0	~CT106-CTS2
GPIO17	V13	I/O	1V8	Z	~CT105-RTS2 / INT7*
GPIO18	Y3	I/O	1V8	Z	SIMPRES / INT8*
GPIO19	AA17	I/O	2V8	Z	Not mux
GPIO20	Y13	I/O	2V8	Undefined	Not mux
GPIO21	AA13	I/O	2V8	Undefined	Not mux
GPIO22	M15	I/O	2V8	Z	Not mux
GPIO23	V17	I/O	2V8	Z	Not mux
GPIO24	N16	I/O	2V8	Z	Not mux
GPIO25	Y19	I/O	2V8	Z	INT0/INT1*
GPIO26	AA15	I/O	Open drain	Z	Not mux
GPIO27	AA16	I/O	Open drain	Z	Not mux
GPIO28	U15	I/O	2V8	Z	SPI1-CLK
GPIO29	V12	I/O	2V8	Z	SPI1-IO
GPIO30	R13	I/O	2V8	Z	SP1-I
GPIO31	M14	I/O	2V8	Z	SPI1-LOAD / INT5*
GPIO32	R15	I/O	2V8	Z	Not mux
GPIO33	M13	I/O	2V8	Z	SPI2-IO
GPIO34	U16	I/O	2V8	Z	Not mux
GPIO35	T18	I/O	2V8	Z	SPI2-LOAD / INT4*
GPIO36	R17	I/O	2V8	Z	CT103-TXD1
GPIO37	T13	I/O	2V8	1	CT104-RXD1 / INT2/INT9*
GPIO38	Y18	I/O	2V8	Z	~CT105-RTS1
GPIO39	N15	I/O	2V8	Z	~CT106-CTS1

Signal	Pin Number	I/O	I/O Type	Reset State	Multiplexed with
GPIO40	T12	I/O	2V8	Z	~CT107-DSR1
GPIO41	M16	I/O	2V8	Z	~CT108-2-DTR1 / INT3/INT10*
GPIO42	AA18	I/O	2V8	Undefined	~CT125-RI1
GPIO43	AB16	I/O	2V8	Undefined	~CT109-DCD1
GPIO44	AB13	I/O	2V8	Undefined	32kHz buffered output clock
GPIO45	Y17	I/O	1V8	Z	INT2*
GPIO47	Y15	I/O	1V8	0	Not mux
GPIO48	Y16	I/O	1V8	0	Not mux

Refer to section 3.3, "Electrical Information for Digital I/O" for Open drain, 2V8 and 1V8 voltage characteristics and for Reset state definition.

* The multiplexed interrupt pin varies depending on the WMP embedded module variant. Refer to section 3.19, External Interrupt for more information about interrupt pins and their multiplexes.

3.10.4. Pin Differences

The pin definitions differ between the AirPrime WMP50 and the WMP100/150 in the manner defined in the table below.

Table 28. GPIO Pin Differences between WMP50 and WMP100/150

	WMP50	WMP100, WMP150
GPIO Allocation table	0x2B, /* GPIO0 <-> GPIOB11 */ 0x5E, /* GPIO1 <-> GPIOC30 */ 0x5D, /* GPIO2 <-> GPIOC29 */ 0x19, /* GPIO3 <-> GPIOA25 */ 0x1A, /* GPIO4 <-> GPIOA26 */ 0x18, /* GPIO5 <-> GPIOA24 */ 0x4A, /* GPIO6 <-> GPIOC10 */ 0x4B, /* GPIO7 <-> GPIOC11 */ 0x29, /* GPIO8 <-> GPIOB09 */ 0x0E, /* GPIO9 <-> GPIOA14 */ 0x27, /* GPIO10 <-> GPIOB07 */ 0x05, /* GPIO11 <-> GPIOA05 */	0x2B, /* GPIO19 <-> GPIOB11 */ 0x5E, /* GPIO20 <-> GPIOC30 */ 0x5D, /* GPIO21 <-> GPIOC29 */ 0x19, /* GPIO22 <-> GPIOA25 */ 0x1A, /* GPIO23 <-> GPIOA26 */ 0x18, /* GPIO24 <-> GPIOA24 */ 0x4A, /* GPIO26 <-> GPIOC10 */ 0x4B, /* GPIO27 <-> GPIOC11 */ 0x29, /* GPIO32 <-> GPIOB09 */ 0x0E, /* GPIO35 <-> GPIOA14 */ 0x27, /* GPIO44 <-> GPIOB07 */ 0x05, /* GPIO45 <-> GPIOA05 */

3.11. Analog-to-Digital Converter

Three Analog-to-Digital Converter inputs are provided by the module. These converters are 10 bits resolution, ranging from 0 to 2V.

3.11.1. Features

ADC1/BAT-TEMP input is used to monitor external temperature. This is very useful for monitoring the application temperature and can be used as an indicator to safely power OFF the application in case of overheating (for Li-Ion batteries).

For more information on battery charging, refer to section 3.15, Battery Charging Interface for more information.

ADC2 and ADC3 input can be used for customer specific applications.

Note: The AirPrime WMP50 does not offer ADC2 and ADC3. ADC2 and ADC3 apply only to the WMP100 and WMP150 modules.

3.11.2. Pin Description

Table 29. ADC Pin Description

Signal	Pin Number	I/O	I/O Type	Description
ADC1 / BAT-TEMP*	N18	I	Analog	A/D converter
ADC2 (unavailable in WMP50)	N17	I	Analog	A/D converter
ADC3 (unavailable in WMP50)	M17	I	Analog	A/D converter

(*): This input is reserved for battery charging temperature sensor. For more information, refer to section 3.15, Battery Charging Interface.

3.11.3. Electrical Characteristics

Table 30. Electrical Characteristics of ADC

Parameter		Min.	Typ.	Max.	Unit
Resolution			10		bits
Sampling rate			216		S/s
Input signal range		0		2	V
Gain error (Vin=2v)		- 0.5		+0.5	dB
Offset error (Vin=0v)		-3		+3	LSB
Vref (DC reference level)		1.15	1.20	1.25	V
Integral Accuracy			15		mV
Differential Accuracy			2.5		mV
Input impedance to Vref.	ADC1 / BAT-TEMP		1M		Ω
	ADC2 (unavailable in WMP50)		1M		Ω
	ADC3 (unavailable in WMP50)		1M		Ω

3.12. Digital-to-Analog Converter

One Digital to Analog Converter (DAC) output is provided by the module.

Note: The AirPrime WMP50 does not have this capability. This section applies only to the WMP100 and WMP150 modules.

3.12.1. Features

The converter is 8-bit resolution, guaranteed monotonic with a range from 0V to 2.3V.

This output assumes a typical external load of 2kΩ and 50pF in parallel to GND.

3.12.2. Pin Description

Table 31. DAC Pin Description

Signal	Pin number	I/O	I/O type	Reset state	Description
DAC0	V14	O	Analog	Pull down	D/A converter

3.12.3. Electrical Characteristics

Table 32. Electrical Characteristics of DAC

Parameter	Min.	Typ.	Max.	Unit
Resolution	-	8	-	bits
Maximum Output voltage	2.1	2.2	2.3	V
Minimum Output voltage	0	-	40	mV
Output voltage after reset	-	1.147	-	V
Integral Accuracy	-5	-	+5	LSB
Differential Accuracy	-1	-	+1	LSB
Full scale settling time (load: 50pF // 2kΩ to GND)	-	40	-	µs
One LSB settling time (load: 50pF // 2kΩ to GND)	-	8	-	µs

3.13. Analog Audio Interface

The WMP module supports two microphone inputs and two speaker outputs. It also includes an echo cancellation and a noise reduction feature which allows for an improved quality of hands-free functionality.

In some cases, ESD protection must be added on the audio interface lines.

3.13.1. Pin Description

The following table lists the pin description of the analog audio interface.

Table 33. Analog Audio Pin Description

Signal	Pin Number	I/O	I/O Type	Description
MIC1P	AC10	I	Analog	Microphone 1 positive input
MIC1N	AB10	I	Analog	Microphone 1 negative input
MIC2P	AC9	I	Analog	Microphone 2 positive input
MIC2N	AB9	I	Analog	Microphone 2 negative input
SPK1P	AC8	O	Analog	Speaker 1 positive output
SPK1N	AB8	O	Analog	Speaker 1 negative output

Signal	Pin Number	I/O	I/O Type	Description
SPK2P	AC7	O	Analog	Speaker 2 positive output
SPK2N	AB7	O	Analog	Speaker 2 negative output

3.13.2. Microphone Features

The microphone can be connected in either differential or single-ended mode. However, it is strongly recommended to use a differential connection in order to reject common mode noise and TDMA noise. When using a single-ended connection, be sure to have a very good ground plane, very good filtering, as well as shielding in order to avoid any disturbance on the audio path. Also note that using a single-ended connection decreases the audio input signal by 6dB as compared to using a differential connection.

The gain of both MIC inputs are internally adjusted and can be tuned using AT commands. For more information on AT commands, refer to document [3] Open AT Framework AT Commands Interface Guide for Firmware 7.0 or later for more information.

Both can be configured in differential or single ended.

The MIC2 inputs already include the biasing for an electret microphone allowing an easy connection.

3.13.2.1. MIC1 Microphone Inputs

By default, MIC1 inputs are single-ended but can be configured in differential mode.

The MIC1 input does not include an internal bias making it the standard input for an external headset or a hands-free kit. If an electret microphone is used, there must be external biasing that corresponds with the characteristics of the electret microphone used.

AC coupling is already embedded in the module.

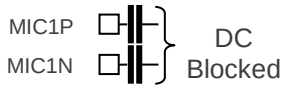
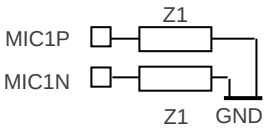
DC Equivalent Circuit	AC Equivalent Circuit
	

Figure 20. Equivalent Circuit of MIC1

Refer to the following table for the electrical characteristics of MIC1.

Table 34. Electrical Characteristics of MIC1

Parameters		Min.	Typ.	Max.	Unit
DC Characteristics			N/A		V
AC Characteristics 200 Hz<F<4 kHz	Z1	70	120	160	kΩ

Parameters		Min.	Typ.	Max.	Unit
Maximum working voltage (MIC1P-MIC1N)	AT+VGT*= 3500		13.8		mVrms
	AT+VGT* = 2000		77.5		
	AT+VGT* = 750		346		
Maximum rating voltage (MIC1P or MIC1N)	Positive			+7.35	V
	Negative	-0.9			

(*): The input voltage depends of the input micro gain set by AT command. Refer to document [3] Open AT Framework AT Commands Interface Guide for Firmware 7.0 or later.

Caution: *The voltage input value for MIC1 cannot exceed the maximum working voltage; otherwise, clipping will appear.*

3.13.2.2. MIC2 Microphone Inputs

By default, MIC2 inputs are differential ones, but it can be configured in single ended. The MIC2 input already includes biasing for an electret microphone and the electret microphone may be directly connected to this input.

AC coupling is already embedded in the module.

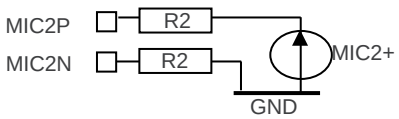
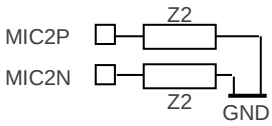
DC Equivalent Circuit	AC Equivalent Circuit
	

Figure 21. Equivalent Circuits of MIC2

Refer to the following table for the electrical characteristics of MIC2.

Table 35. Electrical Characteristics of MIC2

Parameters		Min.	Typ.	Max.	Unit
Internal biasing DC Characteristics	MIC2+	2	2.1	2.2	V
	Output current		0.5	1.5	mA
	R2	1650	1900	2150	Ω
AC Characteristics 200 Hz<F<4 kHz	Z2 MIC2P (MIC2N=Open)	1.1	1.3	1.6	kΩ
	Z2 MIC2N (MIC2P=Open)				
	Z2 MIC2P (MIC2N=GND)	0.9	1.1	1.4	
	Z2 MIC2N (MIC2P=GND)				
	Impedance between MIC2P and MIC2N	1.3	1.6	2	
Maximum working voltage (MIC2P-MIC2N)	AT+VGT* = 3500		14.2		mVrms
	AT+VGT* = 2000		80		
	AT+VGT* = 750		356		

Parameters		Min.	Typ.	Max.	Unit
Maximum rating voltage (MIC2P or MIC2N)	Positive			+7.35**	V
	Negative	-0.9			

(*): The input voltage depends of the input micro gain set by AT command. Refer to document [3] Open AT Framework AT Commands Interface Guide for Firmware 7.0 or later.

(**): Because MIC2P is internally biased, it is necessary to use a coupling capacitor to connect an audio signal provided by an active generator. Only a passive microphone can be directly connected to the MIC2P and MIC2N inputs.

Caution: *The voltage input value for MIC2 cannot exceed the maximum working voltage; otherwise, clipping will appear.*

3.13.3. Speaker Features

There are two different speaker channels, SPK1 and SPK2, available on the module. The connection on SPK1 is fixed as single-ended while SPK2 can be configured in either differential or single-ended mode.

However, as with the microphone connection, it is strongly recommended to use a differential connection in order to reject common mode noise and TDMA noise. Moreover, using a single-ended connection entails losing power (1/2 of the power lost) as compared to using a differential connection.

Note that when using a single-ended connection, a very good ground plane, very good filtering, as well as shielding is needed in order to avoid any disturbance on the audio path.

The gain of each speaker output channel is internally adjusted and can be tuned using AT commands. For more information on AT commands, refer to document [3] Open AT Framework AT Commands Interface Guide for Firmware 7.0 or later for more information.

The following table lists the typical values of both speaker outputs.

Table 36. Speaker Impedance Information

Parameter	Typ.	Unit	Connection
Z (SPK1P, SPK1N)	16 or 32	Ω	Single-ended mode
Z (SPK2P, SPK2N)	4	Ω	Single-ended mode
Z (SPK2P, SPK2N)	8	Ω	Differential mode

3.13.3.1. Speakers Outputs Power

The maximum power output of SPK1 and SPK2 are not similar because of the difference in their configuration. Because SPK2 can be connected in differential mode, it can provide more power compared to SPK1 which only allows single-ended connections. The maximal specifications given below are available with the maximum power output configuration values set by AT command, and the typical values are recommended.

Caution: *It is mandatory not to exceed the maximal speaker output power and the speaker load must be in accordance with the gain selection (gain is controlled by AT command). Exceeding beyond the specified maximal output power may damage the module.*

3.13.3.1.1. SPK1 Speaker Outputs

With the SPK1 interface, only single ended speaker connection is allowed.

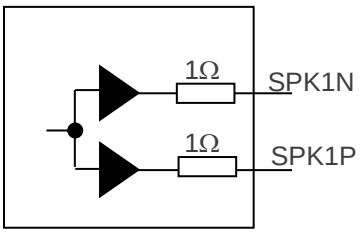


Figure 22. Equivalent Circuits of SPK1

Refer to the following table for the electrical characteristics of SPK1.

Table 37. Electrical Characteristics of SPK1

Parameters			Min.	Typ.	Max.	Unit
Biasing voltage	-			1.30		V
Output swing voltage	RL=16Ω: AT+VGR=600; single-ended		-	1.7	-	Vpp
	RL=32Ω; AT+VGR=600; single-ended		-	1.9	2.75	Vpp
RL	Load resistance		14.5	32	-	Ω
IOUT	Output current; single-ended; peak value	RL=16Ω	-	40	85	mA
		RL=32Ω	-	22	-	mA
POUT	RL=16Ω; AT+VGR*=600		-	25		mW
	RL=32Ω; AT+VGR*=600		-	16	27	mW
RPD	Output pull-down resistance at power-down		28	40	52	kΩ

(*): The output voltage depends of the output speaker gain set by AT command. Refer to document [3] Open AT Framework AT Commands Interface Guide for Firmware 7.0 or later.

3.13.3.1.2. SPK2 Speaker Outputs

The SPK2 interface allows differential or single ended speaker connection.

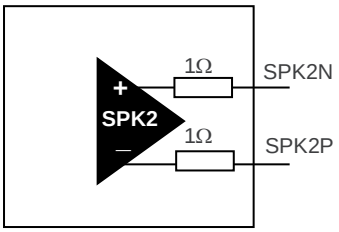


Figure 23. Equivalent Circuits of SPK2

Refer to the following table for the electrical characteristics of SPK2.

Table 38. Electrical Characteristics of SPK2

Parameters		Min.	Typ.	Max.	Unit
Biasing voltage	SPK2P and SPK2N		1.30		V

Parameters		Min.	Typ.	Max.	Unit
Output swing voltage	RL=8Ω: AT+VGR=600*; single ended	-	-	2	Vpp
	RL=8Ω: AT+VGR=600*; differential	-	-	4	Vpp
	RL=32Ω: AT+VGR=600*; single ended	-	-	2.5	Vpp
	RL=32Ω: AT+VGR=600*; differential	-	-	5	Vpp
RL	Load resistance	6	8	-	Ω
IOUT	Output current; peak value; RL=8Ω	-	-	180	mA
POUT	RL=8Ω; AT+VGR=600*;	-	-	250	mW
RPD	Output pull-down resistance at power-down	28	40	52	kΩ
VPD	Output DC voltage at power-down	-	-	100	mV

* The output voltage depends of the output speaker gain set by AT command. Please refer to document [3] Open AT Framework AT Commands Interface Guide for Firmware 7.0 or later. If a singled ended solution is used with the SPK2, only one of the both SPK2 has to be chosen. The result is a maximal output power divided by 2.

3.13.4. Application

3.13.4.1. Microphone MIC1

3.13.4.1.1. MIC1 Differential Connection Example

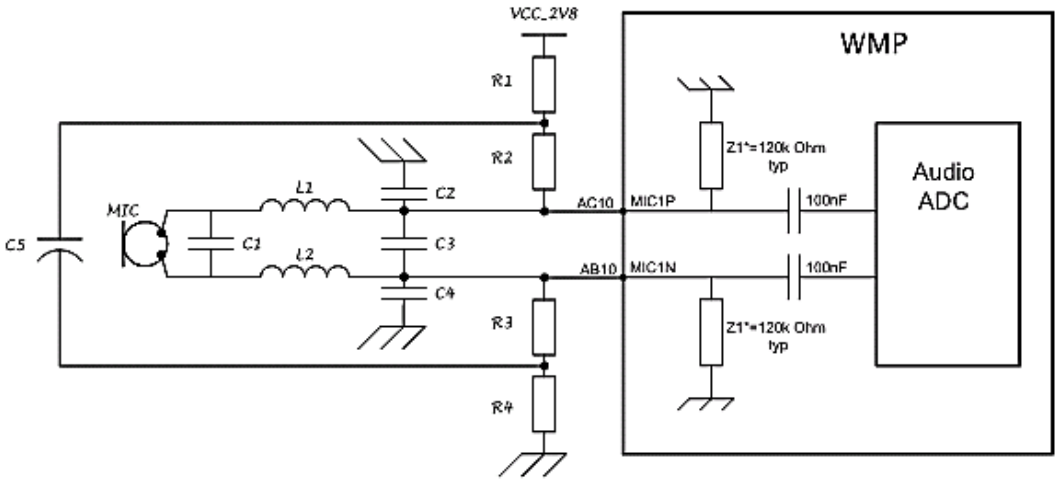


Figure 24. Example of a MIC1 Differential Connection with LC Filter

(*): Z1 is from 200 Hz to 4 kHz. For more characteristics, refer to section 3.13.2.1, MIC1 Microphone Inputs.

Note: Audio quality can be very good without L1, L2, C2, C3, and C4 depending on the design. But if there is EMI perturbation, this filter can reduce the TDMA noise. This filter (L1, L2, C2, C3, and C4) is not mandatory. If not used, the capacitor must be removed and coil replaced by 0 Ohm resistors as the shown in the following schematic.

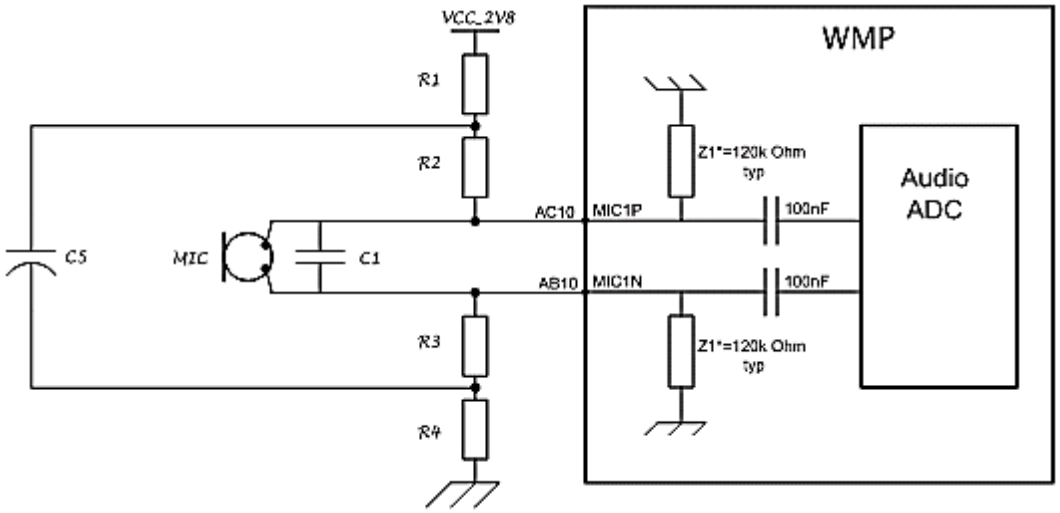


Figure 25. Example of a MIC1 Differential Connection without LC Filter

(*): Z1 is from 200 Hz to 4 kHz. For more characteristics refer to section 3.13.2.1, MIC1 Microphone Inputs.

Capacitor C1 is highly recommended to eliminate the TDMA noise and it must be connected close to the microphone.

Although Vbias can be VCC_2V8 (ball R1) of the module, it is recommended to use another 2V to 3V power supply voltage instead. This is because Vbias must be kept as “clean” as possible to avoid bad performance when a single-ended connection is used.

Caution: *TDMA noise may degrade quality when VCC_2V8 is used.*

The following table lists the recommended components to use in creating the LC filter.

Table 39. Recommended Components for a MIC1 Differential Connection

Component	Value	Notes
R1	4.7kΩ	For Vbias equal to 2.8V.
R2, R3	820Ω	
R4	1kΩ	
C1	12pF to 33pF	Must be tuned depending on the design.
C2, C3, C4	47pF	Must be tuned depending on the design.
C5	2.2uF +/- 10%	
L1, L2	100nH	Must be tuned depending on the design.

3.13.4.1.2. MIC1 Single-Ended Connection Example

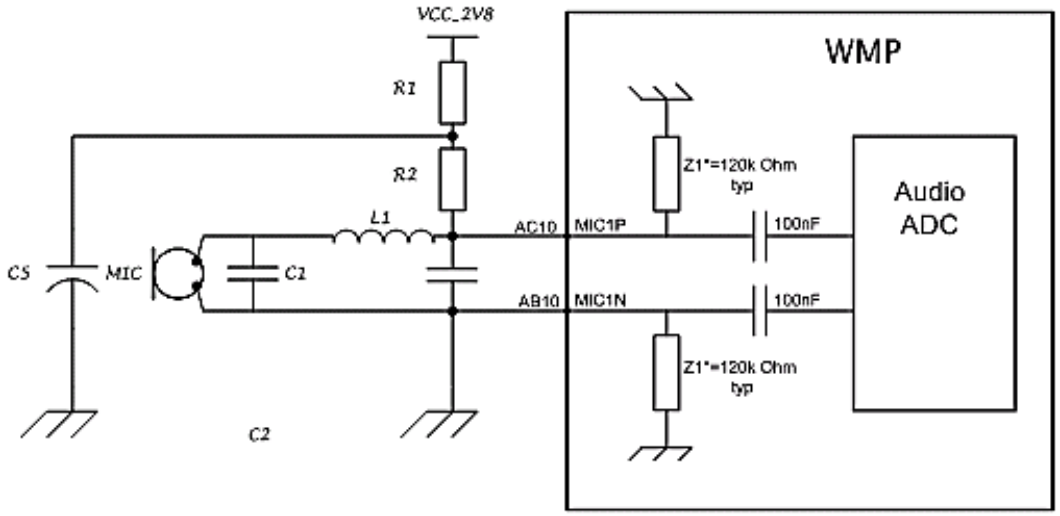


Figure 26. Example of a MIC1 Single-Ended Connection with LC Filter

(*): Z1 is from 200 Hz to 4 kHz. For more characteristics refer to section 3.13.2.1, MIC1 Microphone Inputs.

The single ended design is not recommended for improving TDMA rejection noise as it is usually difficult to eliminate TDMA noise from a single ended design.

It is recommended to add L1 and C2 footprint to add a LC EMI filter to try to eliminate the TDMA noise.

Note though that this filter is not mandatory. If the filter is not to be used, the capacitor C2 must be removed and the coil inductor (L1) must be replaced by 0Ω resistors as shown in the following diagram.

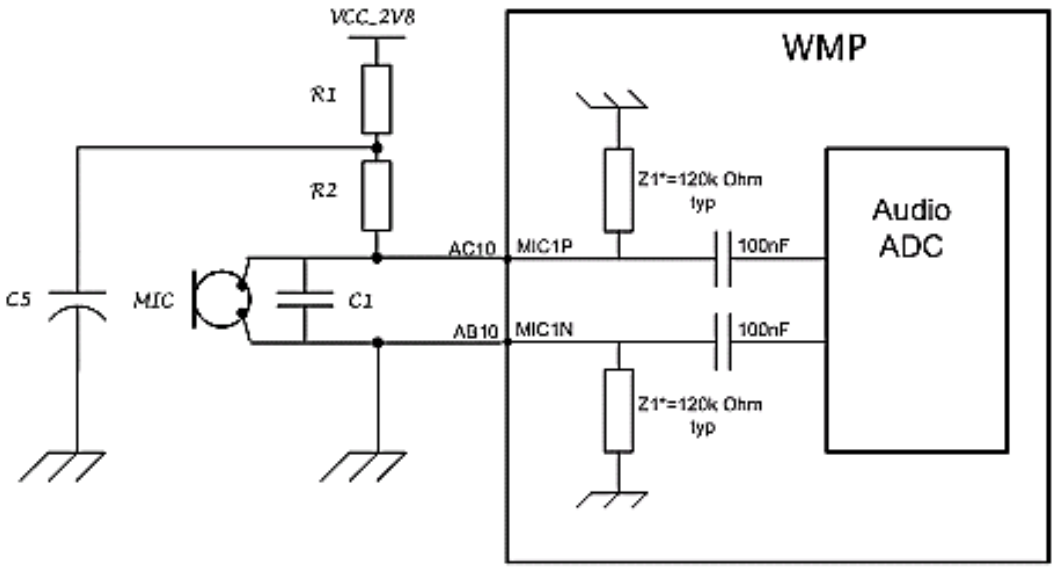


Figure 27. Example of a MIC1 Single-Ended Connection without LC Filter

(*): Z1 is from 200 Hz to 4 kHz. For more characteristics, refer to section 3.13.2.1, MIC1 Microphone Inputs.

The capacitor C1 is highly recommended to eliminate the TDMA noise. C1 must be close to the microphone.

Although Vbias can be VCC_2V8 (ball R1) of the module, it is recommended to use another 2V to 3V power supply voltage instead. This is because Vbias must be kept as “clean” as possible to avoid bad performance when a single-ended connection is used.

Caution: *TDMA noise may degrade quality when VCC_2V8 is used.*

Table 40. Recommended Components for a MIC1 Single-Ended Connection

Component	Value	Notes
R1	4.7kΩ	For Vbias equal to 2.8V.
R2	820Ω	
C1	12pF to 33pF	Must be tuned depending on the design.
C2	47pF	Must be tuned depending on the design.
C5	2.2uF +/- 10%	
L1	100nH	Must be tuned depending on the design.

3.13.4.2. Microphone MIC2

3.13.4.2.1. MIC2 Differential Connection Example

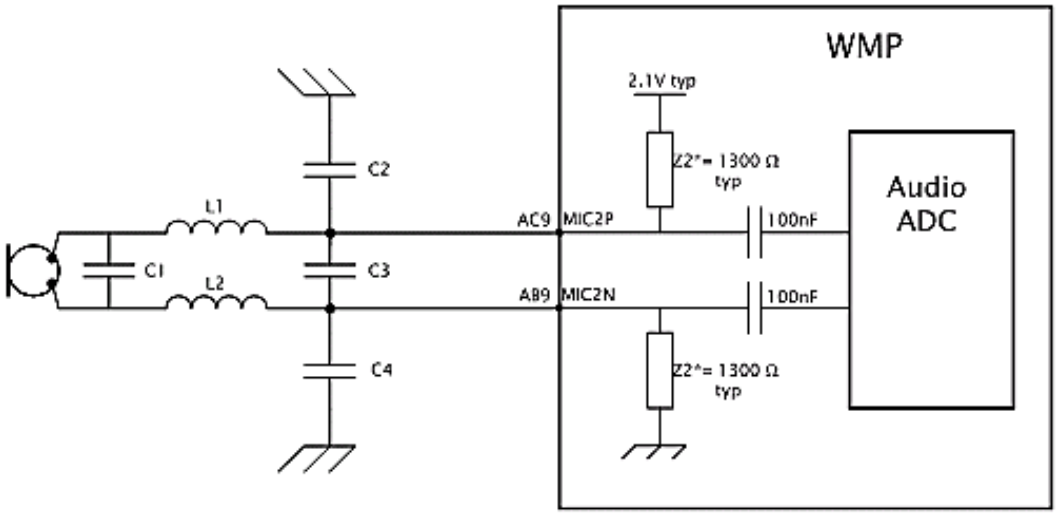


Figure 28. Example of a MIC2 Differential Connection with LC Filter

(*): Z2 is from 200Hz to 4 kHz. For more characteristics, refer to section 3.13.2.2, MIC2 Microphone Inputs.

Note: Audio quality can be very good without L1, L2, C2, C3, and C4 depending on the design. But if there is EMI perturbation, this filter can reduce the TDMA noise. This filter (L1, L2, C2, C3, and C4) is not mandatory. If not used, the capacitor must be removed and coil replaced by 0 Ohm resistors as the shown in the following schematic.

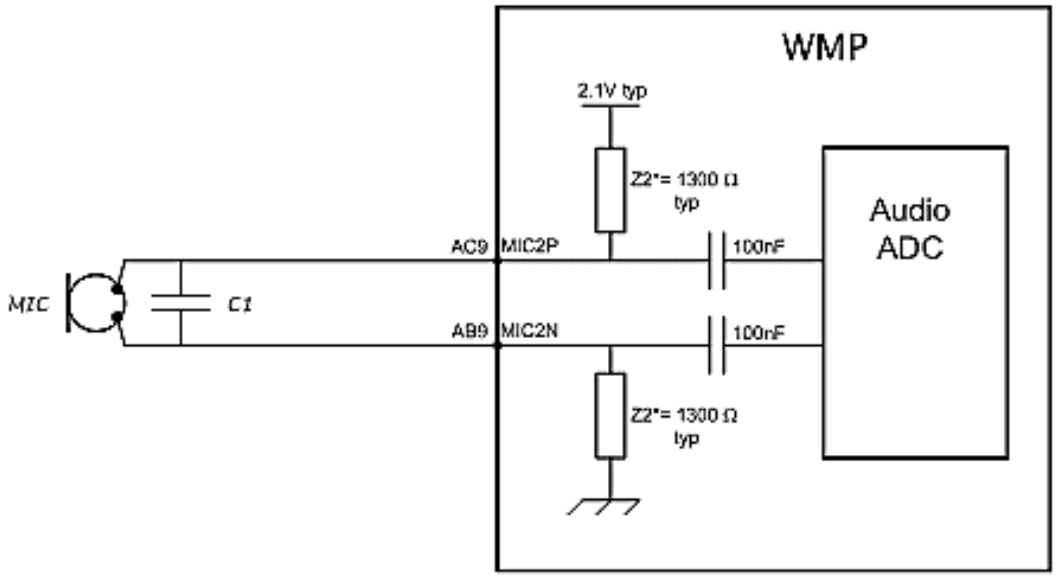


Figure 29. Example of a MIC2 Differential Connection without LC Filter

(*): Z2 is from 200 Hz to 4 kHz. For more characteristics, refer to section 3.13.2.2, MIC2 Microphone Inputs.

Capacitor, C1, is highly recommended to eliminate the TDMA noise and it must be close to the microphone.

The following table lists the recommended components to use in creating the LC filter.

Table 41. Recommended Components for a MIC2 Differential Connection

Component	Value	Notes
C1	12pF to 33pF	Must be tuned depending on the design.
C2, C3, C4	47pF	Must be tuned depending on the design.
L1, L2	100nH	Must be tuned depending on the design.

3.13.4.2.2. MIC2 Single-Ended Connection Example

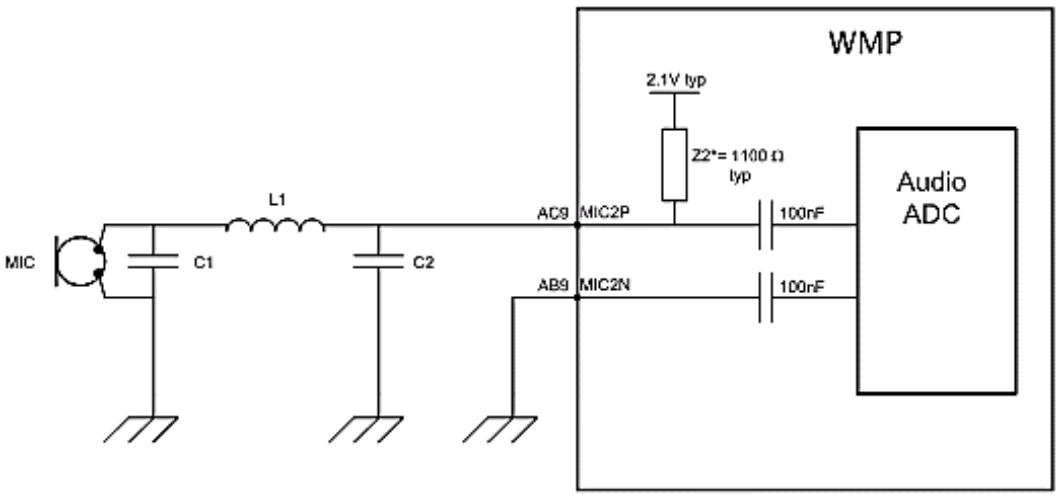


Figure 30. Example of a MIC2 Single-Ended Connection with LC Filter

(*): Z2 is from 200 Hz to 4 kHz. For more characteristics, refer to section 3.13.2.2, MIC2 Microphone Inputs.

Internal input impedance value becomes 1100 ohms, due to the connection of MIC2N to ground.

The single-ended design is not recommended for improving TDMA noise rejection as it is usually difficult to eliminate TDMA noise from a single-ended design.

It is recommended to add a LC filter (L1 and C2) to eliminate the TDMA noise. Note though that this filter is not mandatory. If the filter is not to be used, the capacitor C2 must be removed and the coil inductor must be replaced by 0 Ohm resistors as shown in the following diagram.

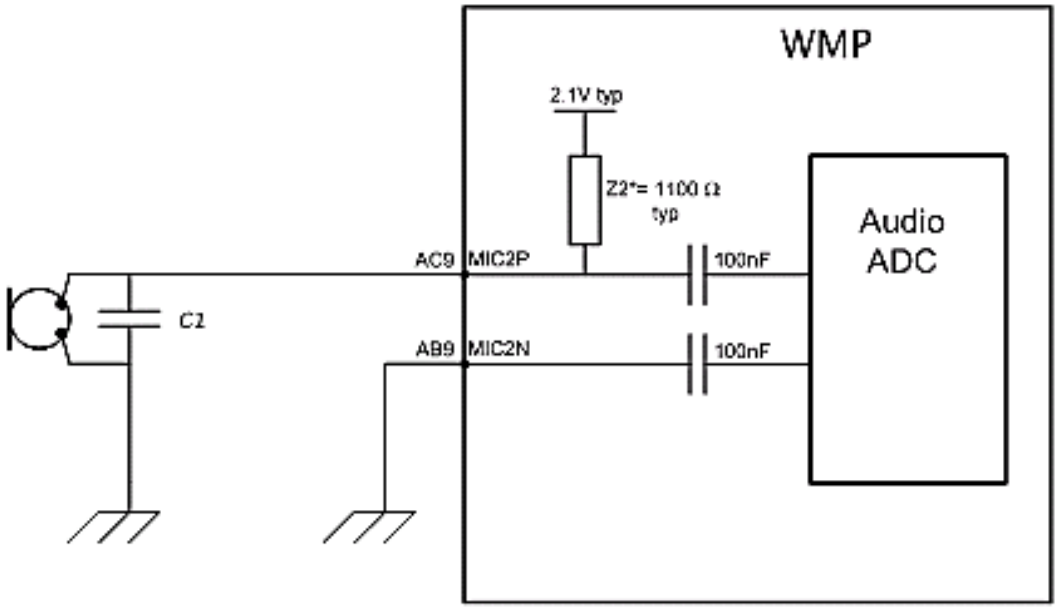


Figure 31. Example of a MIC2 Single-Ended Connection without LC Filter

(*): Z2 is from 200 Hz to 4 kHz. For more characteristics, refer to section 3.13.2.2, MIC2 Microphone Inputs.

Capacitor, C1, is highly recommended to eliminate the TDMA noise and it must be close to the microphone.

The following table lists the recommended components to use in creating the LC filter.

Table 42. Recommended Components for a MIC2 Single-Ended Connection

Component	Value	Notes
C1	12pF to 33pF	Must be tuned depending on the design.
C2		Must be tuned depending on the design.
L1		Must be tuned depending on the design.

3.13.4.3. Speaker

3.13.4.3.1. SPK2 Differential Connection

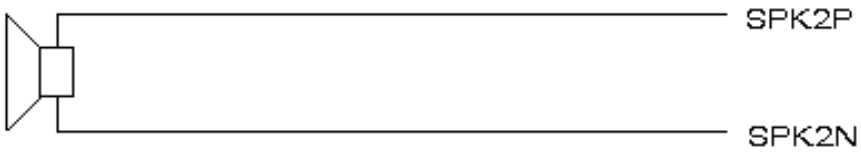


Figure 32. Example of Speaker Differential Connection

Impedance of the speaker amplifier output in differential mode is:

R ≤ 2Ω +/-10 %

Note that the connection between the speaker and the module pins must be designed to keep the serial impedance lower than 3Ω when it is connected in differential mode.

3.13.4.3.2. SPKx Single-Ended Connection Example

Typical implementation

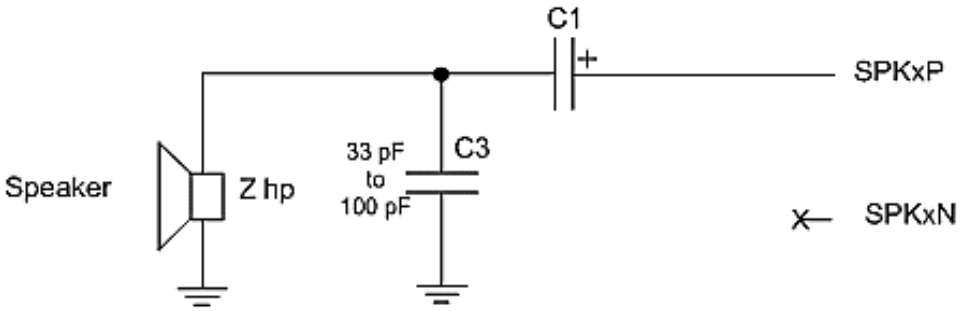


Figure 33. Example of Speaker Single-Ended Connection

Take note of the following when connecting the speaker in single-ended mode:

4.7 µF < C1 < 47 µF (depending on speaker characteristics and output power)

Note that using a single-ended connection includes losing of the output power (- 6dB) compared to a differential connection.

The connection between the module and the speaker must be designed to keep the serial impedance lower than 1.5 Ω in the single-ended mode.

If SPKxP channel is used, SPKxN can be left opened.

If SPKxN channel is used, SPKxP can be left opened.

3.13.5. Design Recommendations

3.13.5.1. General

When speakers and microphones are exposed to the external environment, it is recommended to add ESD protection as closed as possible to the speaker or microphone, connected between the audio lines and a good ground.

The microphone connections may be either differential or single-ended, but using a differential connection to reject common mode noise and TDMA noise is strongly recommended.

While using a single-ended connection, ensure to have a good ground plane, a good filtering as well as shielding, in order to avoid any disturbance on the audio path.

It is important to select an appropriate microphone, speaker and filtering components to avoid TDMA noise.

3.13.5.2. Recommended Microphone Characteristics

The impedance of the microphone has to be around 2 kΩ.

Sensitivity from -40dB to –50 dB

SNR > 50 dB

Frequency response compatible with the GSM specifications

To suppress TDMA noise, it is highly recommended to use microphones with two internal decoupling capacitors:

- CM1=56pF (0402 package) for the TDMA noise coming from the demodulation of the GSM 850 and GSM900 frequency signal.
- CM2=15pF (0402 package) for the TDMA noise coming from the demodulation of the DCS/PCS frequency signal.

The capacitors have to be soldered in parallel of the microphone.

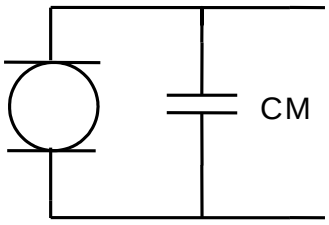


Figure 34. Microphone Circuit

3.13.5.3. Recommended Speaker Characteristics

Type of speakers: Electro-magnetic /10mW

Impedance: 8Ω for hands-free (SPK2)

Impedance: 32Ω for heads kit (SPK1)

Sensitivity: 110dB SPL min

Receiver frequency response is compatible with the GSM specifications.

3.13.5.4. Recommended Filtering Components

When designing a GSM application, it is important to select the right audio filtering components.

The strongest noise, called TDMA, is mainly due to the demodulation of the GSM850/GSM900/DCS1800 and PCS1900 signal: A burst being produced every 4.615ms; the frequency of the TDMA signal is equal to 216.7Hz plus harmonics.

The TDMA noise can be suppress by filtering the RF signal using the right decoupling components.

The types of filtering components are:

- RF decoupling inductors
- RF decoupling capacitors

A good “Chip S-Parameter” simulator is proposed by Murata, the following link help to find it:

http://www.murata.com/designlib/mcsil.html

Using different Murata components, we could see that the value, the package and the current rating can have different decoupling effects.

The table below shows some examples with different Murata components:

Table 43. Examples of Murata Components

Package	**0402**		
Filtered band	**GSM900**	**GSM 850/900**	**DCS/PCS**
Value	100nH	56pF	15pF
Types	Inductor	Capacitor	Capacitor
Position	Serial	Shunt	Shunt
Manufacturer	Murata	Murata	Murata
Rated	150mA	50V	50V
Reference	LQG15HSR10J02 or LQG15HNR10J02	GRM1555C1H560JZ01	GRM1555C1H150JZ01 or GRM1555C1H150JB01
Value	100nH	47pF	10pF
Types	Inductor	Capacitor	Capacitor
Position	Serial	Shunt	Shunt
Manufacturer	Murata	Murata	Murata
Rated	300mA	50V	50V
Reference	LQG18HNR10J00	GRM1885C1H470JA01 or GRM1885C1H470JB01	GRM1885C1H150JA01 or GQM1885C1H150JB01

3.13.5.5. Audio Track and PCB Layout Recommendations

To avoid TDMA noise, it is recommended to surround the audio tracks by ground as shown below.

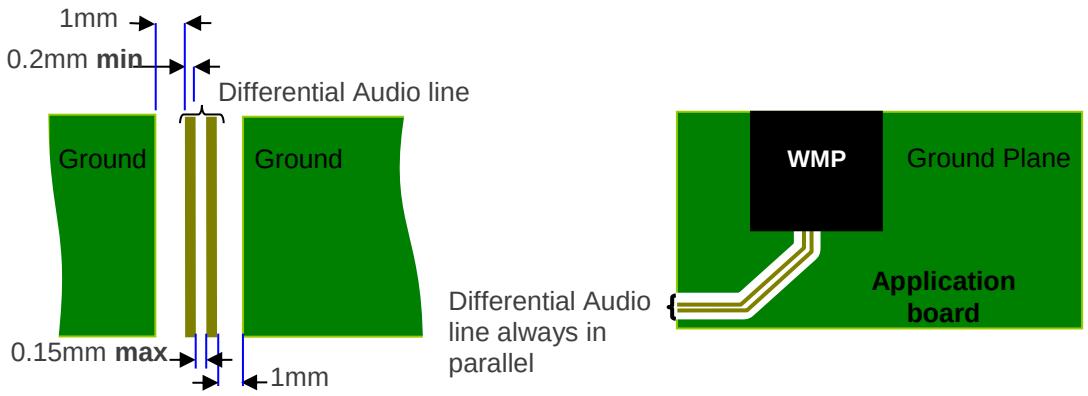


Figure 35. Audio Track Design

Tip: *Avoid digital tracks crossing under and over the audio tracks.*

3.14. Buzzer Output

This digital output is controlled by a pulse-width modulation (PWM) controller and is an open drain output. This signal may only be used in the implementation of a buzzer.

3.14.1. Features

The BUZZER0 is an open drain one. The buzzer can be directly connected between this output and VBATT. The maximum current is 100mA (PEAK).

3.14.2. Pin Description

Signal	Pin Number	I/O	I/O Type	Reset State	Description
BUZZER0	U4	O	Open drain	Z	Buzzer output

Refer to section 3.3, "Electrical Information for Digital I/O" for Open drain, 2V8 and 1V8 voltage characteristics and for Reset state definition.

3.14.3. Electrical Characteristics

Table 44. Electrical Characteristics of the Buzzer Output

Parameter	Condition	Minimum	Maximum	Unit
V_{OL}	I_{OL} = 100mA		0.4	V
I_{PEAK}	VBATT = VBATTmax		100	mA
Frequency		3	10000*	Hz

Parameter	Condition	Minimum	Maximum	Unit
Duty cycle		0*	100*	%

Note: (*) Be careful to the maximum frequency and the minimum/maximum duty cycle. There are limited due to the RC environment.

In fact, at the limits, the result is that the amplitude modulation is less fine.

3.14.4. Application

The maximum peak current is 100 mA and the maximum average current is 40 mA. A diode against transient peak voltage must be added as described below.

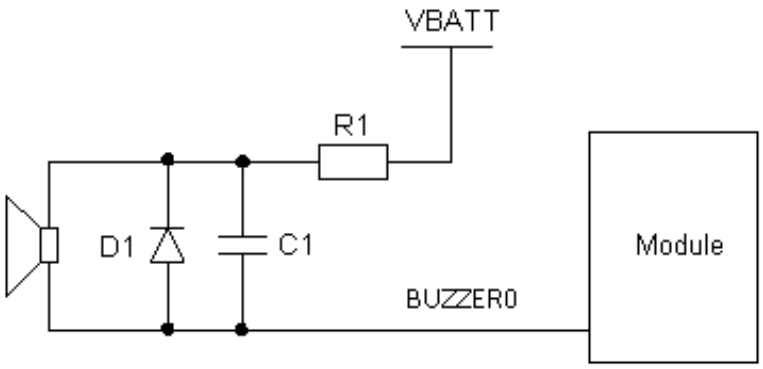


Figure 36. Example of a Buzzer Implementation

Where:

R1 must be chosen in order to limit the current at I_{PEAK} max and must be adjusted in function of the frequency and the duty cycle used.

C1 = 0 to 100 nF (depending on the buzzer type)

D1 = BAS16 (for example)

A low filter is recommended at low frequencies.

3.14.4.1. Calculations of the Low Filter

Req is the total resistor in line.

C is the capacitive charge on BUZZER0 signal and the ground.

The cut-off frequency (F_C) must be higher than $F_{BUZZER0}$.

Due to the conception of this signal, the frequency modulation of the BUZZER0 signal is 64* $F_{BUZZER0}$.

$F_C = 1/ (2. \Pi.Req.C)$

*Note: Fc must be at least 64 * FBUZZER0.*

3.14.4.2. Recommended Characteristics for the Buzzer

- Electro-magnetic type
- Impedance: 7 to 30 Ω
- Sensitivity: 90 dB SPL min @ 10 cm
- Current: 60 to 90 mA

The BUZZER0 output can also be used to drive an LED as shown in the figure below:

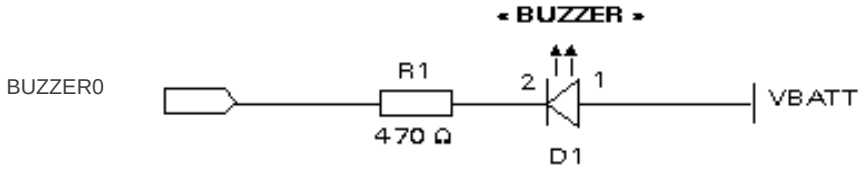


Figure 37. Example of a LED Driven by the Buzzer0 Output

The value of R1 should correspond with the characteristics of the LED (D1).

3.15. Battery Charging Interface

The charging interface of WMP modules is able to drive the charging of different battery technologies by combining hardware and software controls.

3.15.1. Features

The charging architecture of WMP modules supports 3 types of battery technology:

- Ni-Cd (Nickel-Cadmium)
- Ni-Mh (Nickel-Metal Hydride)
- Li-ion (Lithium-Ion) with the embedded PCM (Protection Circuit Module).

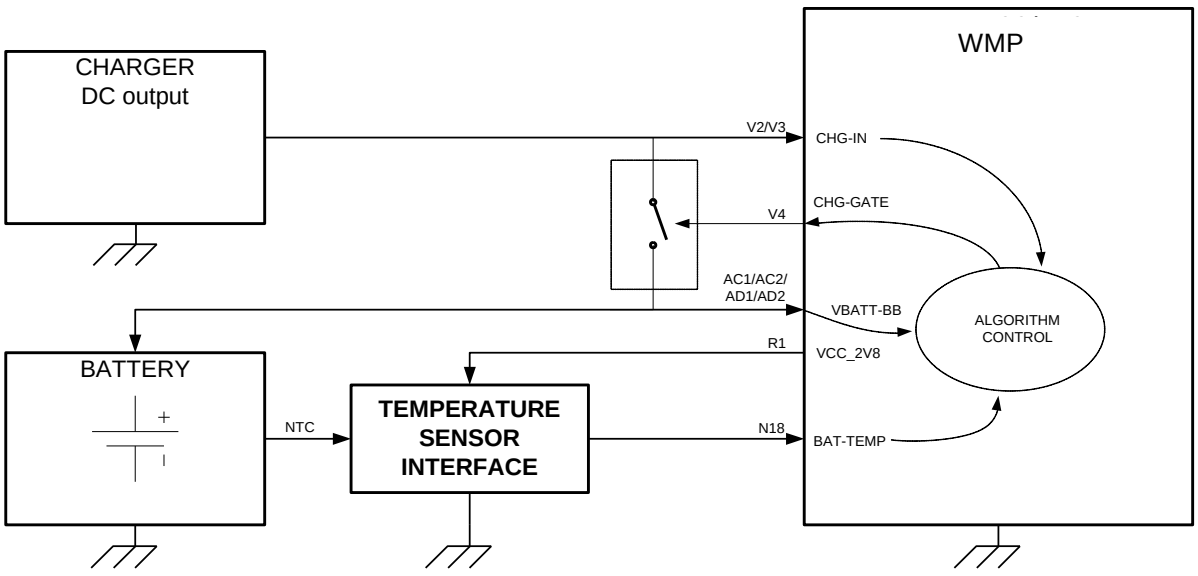


Figure 38. Battery Charging Block Diagram

The software algorithm controls a switch (by CHG-GATE signal), which connects the CHG-IN signal to the VBATT-BB signal. The algorithm controls the frequency and the connected time of the switching. During the charging procedure the battery charging level is controlled by the VBATT-BB measurement. When the battery is full, the algorithm stops the charging procedure.

When Li-Ion battery is used, the battery temperature is monitored through the BAT-TEMP ADC input.

One more charging mode is provided by the module called “Pre-charging” mode, but it’s a special charging mode because it is activated only when the module is OFF. So the control is only performed by the hardware. The goal of this charging mode is to prevent the battery from being damaged by preventing it from being discharged under the minimum battery level.

3.15.2. Pre-Charging

When a charger DC power supply is connected to the CHG-IN signal and if the voltage battery is between 2.8V* and 3.2V, a constant current of 50mA is provided to the battery.

When the battery is able to supply the module and Open AT Framework 2.0, the module is automatically powered on and the software algorithm is activated to finish the charge.

When pre-charging is launched, LED0 blinks automatically.

Caution: *It cannot release the PCM protection inside Lithium battery pack. Voltage forbidden on the CHG-IN signal if no battery connected on VBATT signals.*

Note: *(*) For the Lithium-ion battery, the minimum voltage must be higher than the PCM lock level. Take note that if the voltage goes below the PCM lock level (in this case, 2.8V), charging is not guaranteed.*

3.15.3. Pin Description

Table 45. Pin Description of Battery Charging Interface

Signal	Pin Number	I/O	I/O Type	Description
CHG-IN	V2 / V3	I	Analog	Current source input
CHG-GATE	V4	O	Analog	Current source to drive PNP transistor
ADC1 / BAT-TEMP	N18	I	Analog	A/D converter

3.15.4. Temperature Monitoring

The monitoring of the temperature is only available for the Li-Ion battery. The ADC1 / BAT-TEMP (N18) ADC input must be used to sample the temperature analog signal provided by a NTC temperature sensor which is placed close to the battery cellular. The minimum and maximum temperature range can be set by software command.

Table 46. Electrical Characteristics of Battery Charging Interface

Parameter	Minimum	Typical	Maximum	Unit
Charging Operating Temperature	0		50	°C

Parameter		Minimum	Typical	Maximum	Unit
ADC1 / BAT-TEMP	Resolution		10		bits
	Sampling Rate		216		S/s
	Input Impedance (R)		1M		Ω
	Input Signal Range	0		2	V
CHG-IN	Voltage (for I=Imax)	4.81			V
	Voltage (for I=0)			61	V
	DC Current Imax	Min.3		8004	mA
CHG-GATE (with R4) 2	Switch Control By Current			10	mA

(1): To be parameterized as per battery manufacturer.

(2): Refer to the application of section 3.15.5.

(3): With a charger limited to 100mA, without GSM communication and without R4=470 ohms, the module consumes around 60mA, so the battery is charged around 40mA. (70mA with R4=470ohm). If another power mode is used, refer to the power consumption tables at section 4.3, Power Consumption.

(4): In the case of section 3.15.5, it is recommended to use 800mA.

3.15.5. Application

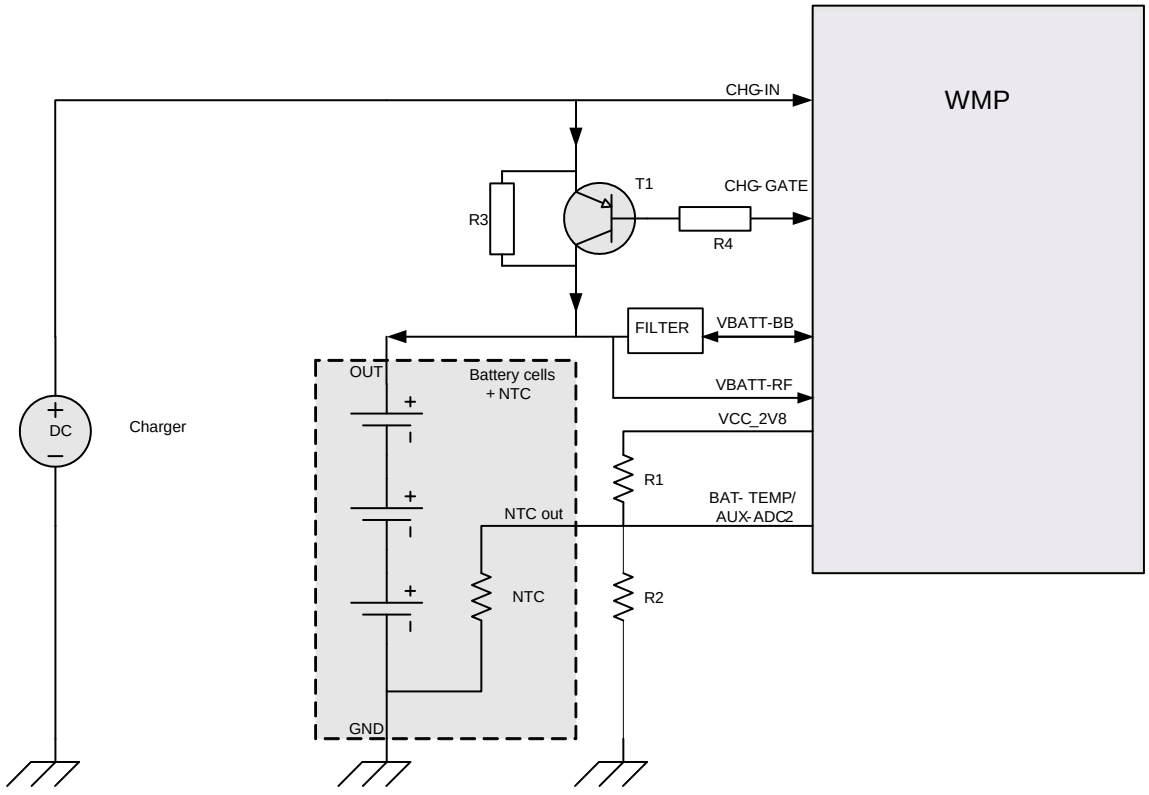


Figure 39. Charging Schematic for Li-ion

The charging schematic needs a transistor to switch the current from the Charger DC source power supply to the battery. The control of the transistor is performed through the CHG-GATE signal by the module.

It is important that the Charger DC power supply has a limited output current to not damage the transistor T1. T1 must be a PNP transistor due to the current source of the CHG-GATE input,

The R1 and R2 resistors are needed only when the temperature is monitored, typically for Li-Ion battery. The R1 is necessary to bias the NTC resistor of the battery. The VCC_2V8 output power voltage of the module can be used to power the bridge R1/ R2 / NTC. The R1 and R2 values have to be calculated to have a maximum of 2volt at the ADC1 / BAT-TEMP input on the module.

The R3 resistor must be ADDED to improve the performances of the charge.

Note: The R3 resistor MUST be removed for WMP100 Embedded SIM and WMP150 Embedded SIM.

Table 47. Design Configuration of R3 for Battery Charging Interface

	WMP50	WMP100	WMP150	WMP100 Embedded SIM	WMP150 Embedded SIM
R3	Added	Added	Added	Removed	Removed

The R4 resistor can be added to improve the charge efficiency. ($I_{CHG-GATE}$ is lower).

Pre-Charging mode doesn't use the T1 transistor, when Pre-charging is activated, the current provided by the Charger DC power supply crosses the module by the CHG-IN signal to the VBATT-BB to charge the battery. The current limitation is controlled inside the module.

3.15.5.1. Recommended components

- T1 : NSL12AW from On Semiconductor
- R1 = 100K
- R2 = 270K
- R3= 5.6K (package 0402, 1/16W, +-5% is sufficient)
- R4 = 470
- NTC = 100K @ 25°C NTH4G42B104F01 from MURATA

Warning: *The Charger DC power supply must have an output current limited to 800mA according to the DC current gain (β) and the base current (Ib) transistor characteristics.*

The maximum Charger output current, provided to the battery, must be accorded to the battery electrical characteristics.

With a charger limited to 100mA, without GSM communication and without R4=470 ohms, the module consumes around 60mA, so the battery is charged around 40mA. (70mA with R4=470ohm).

Li-Ion batteries must be used with the embedded PCM (Protection Circuit Module).

The maximum charging voltage is up to 4,3v (Software drive)

At the first plug, if the battery Li-ion is locked by its PCM the charger function doesn't work.

At the first plug, if the battery is under 2,8v the charger function doesn't work.

3.16. ON/~OFF Signal

This input is used to switch the module ON or OFF.

A high-level signal has to be provided on the pin ON/~OFF to switch ON the module. The voltage of this signal has to be maintained at 0.8 x VBATT for a minimum of 1500ms. This signal can be left at high level until switch off.

To switch OFF the module, the pin ON/OFF has to be released first. It can be switched off through the Operating System by the AT command, **AT+CPOF**.

Warning: *All external signals must be inactive when the module is OFF to avoid any damage when starting and allow the module to start and stop correctly.*

3.16.1. Pin Description

Table 48. ON/~OFF Signal Pin Description

Signal	Pin Number	I/O	I/O Type	Description
ON/~OFF	U5	I	CMOS	Power-ON

3.16.2. Electrical Characteristics

Table 49. Electrical Characteristics of the ON/~OFF Signal

Parameter	I/O Type	Minimum	Maximum	Unit
VIL	CMOS		VBATT x 0.2	V
VIH	CMOS	VBATT x 0.8	VBATT	V

3.16.3. Application

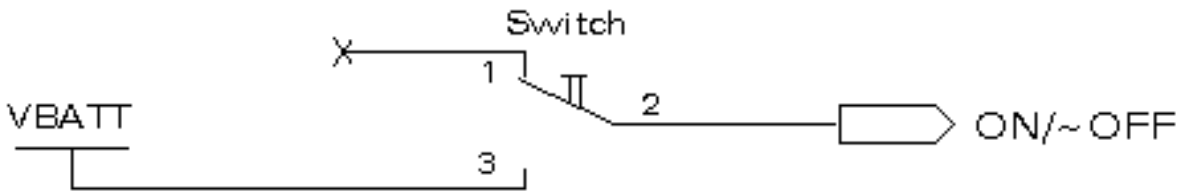


Figure 40. Example of ON/~OFF Pin Connection

3.16.3.1. Power-ON

Once the module and the Open AT Framework 2.0 are powered, the application must set the ON/OFF signal to high to start the module Power-ON sequence. The ON/OFF signal must be held high during a minimum delay of $\mathbf{T_{on/off\text{-}hold}}$ (Minimum hold delay on the ON/~OFF signal) to Power-ON. After this delay, an internal mechanism maintains the module and the firmware in power ON condition.

During the Power-ON sequence, an internal reset is automatically performed by the module and firmware for 40ms (typically). In this phase, any external reset should be avoided during this phase.

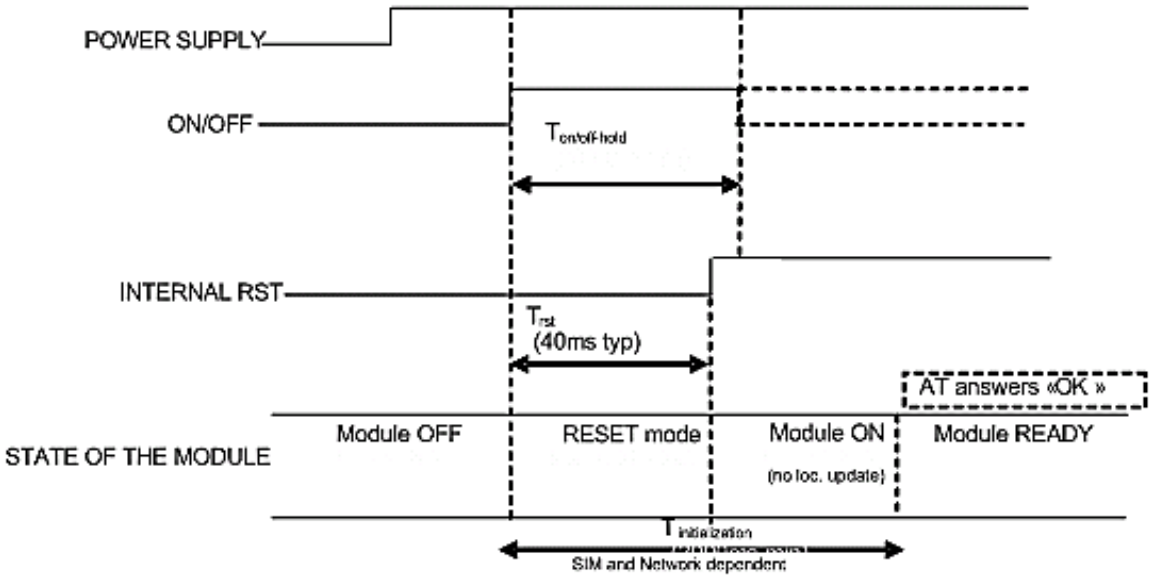


Figure 41. Power-ON Sequence (no PIN code activated)

The duration of the firmware power-up sequence depends on the need to perform a recovery sequence if the power has been lost during a flash memory modification.

Other factors have a minor influence. Listed below are the other factors that have a minor influence on the power-ON sequence:

- The number of parameters stored in EEPROM by the AT commands received so far
- The ageing of the hardware components, especially the flash memory
- The temperature conditions

The *recommended* way to de-assert the ON/~OFF signal is to use either an AT command or WIND indicators: the application has to detect the end of the power-up initialization and de-assert ON/~OFF afterwards.

To release the ON/~OFF signal, either of the following methods may be used:

- Using AT Commands

  Send an “AT” command and wait for the “OK” answer: once the initialization is complete the AT interface answers « OK » to “AT” message.

Note: If the application manages hardware flow control, the AT commands can be sent during the initialization phase.

- Using WIND Indicators

  Wait for the “+WIND: 3” message: after initialization, the module, if configured to do so, will return an unsolicited “+WIND: 3” message. The generation of this message is enabled or disabled via an AT command.

For more information, refer to document [3] Open AT Framework AT Commands Interface Guide for Firmware 7.0 or later. Proceeding thus – by software detection - will always prevent the application from de-asserting the ON/~OFF signal too early.

If WIND indicators are disabled or AT commands unavailable or not used, it is still possible to de-assert ON/~OFF after a delay long enough ($\mathbf{T_{on/off\text{-}hold}}$) to ensure that the firmware has already completed its power-up initialization.

The table below gives the minimum values of $\mathbf{T_{initialization.}}$

Table 50. $T_{on/off-hold}$ Minimum Values

Firmware	$T_{initialization}$
	Safe Evaluations of the Firmware Power-Up time
6.65 & above	8 s

The above figure take the worst cases into account: power-loss recovery operations, slow flash memory operations in high temperature conditions, and so on. But they are safe because they are large enough to ensure that ON/~OFF is not de-asserted too early.

Typical power-up initialization time figures for best cases conditions (no power-loss recovery, fast and new flash memory, etc.) approximately 3.5 seconds in every firmware version. But releasing ON/~OFF after this delay does not guarantee that the application will actually start-up if for example the power plug has been pulled off during a flash memory operation, like a phone book entry update or an AT&W command.

The ON/~OFF signal can be left at a high level until switch OFF. But this is not recommended as it will prevent the AT+CPOF command from performing a clean power-off. (See also the note in section 3.16.3.2, Power-OFF for an alternate usage.)

When using a battery as power source, it is not recommended to let this signal high:

If the battery voltage is too low and the ON/~OFF signal is at low level, an internal mechanism switches OFF module. This automatic process prevents the battery to be over discharged and optimize its life span.

During the power-ON sequence, an internal reset is automatically performed by the module for 40 ms (typically). Any external reset should be avoided during this phase.

Connecting a charger on the module has exactly the same effect than setting the ON/~OFF signal. In particular, the module will not POWER-OFF after the AT+CPOF command, unless the charger is disconnected.

After a reset (hardware or software), if the ON/~OFF signal is OFF (Low level), the module will switch OFF.

3.16.3.2. Power-OFF

To properly power OFF the module, the application must reset the ON/OFF signal and then send the AT+CPOF command to deregister from the network and switch off the module.

Once the « OK » response is issued by the module, the power supply can be switched off.

Caution: *All external signals must be inactive when the module is OFF to avoid any damage when starting.*

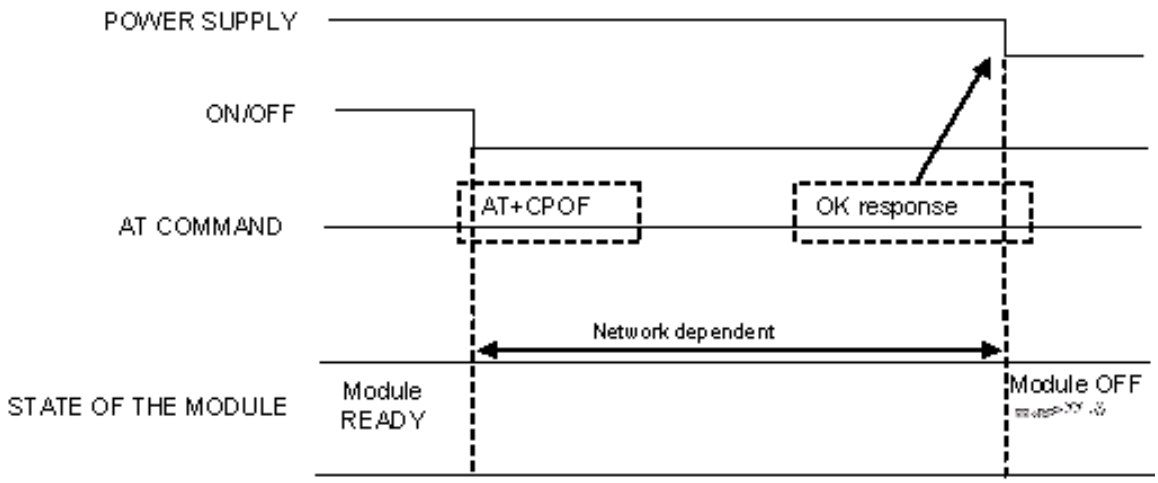


Figure 42. Power-OFF Sequence

Note: If the ON/~OFF pin is maintained at ON (High Level), then the module cannot be switched OFF.

3.17. BOOT Signal

A specific control pin BOOT is available to download the module only if the standard XMODEM download, controlled with AT command, is not possible.

Specific PC software, provided by Sierra Wireless, is needed to perform this download, specifically for the first download of the Flash memory.

3.17.1. Features

The BOOT pin must be connected to the VCC_1V8 for this specific download.

Table 51. BOOT Settings

BOOT	Operating mode	Comment
Leave open	Normal use	No download
Leave open	Download XMODEM	AT command for Download AT+WDWL
1	Download specific	Need Sierra Wireless PC software

For more information, refer to section 3.7.6, First Download.

This BOOT pin must be left open for normal use or XMODEM download.

However, in order to make development and maintenance phases easier, it is **highly recommended** to set a test point, either a jumper or a switch to VCC_1V8 (ball AD5) power supply.

3.17.2. Pin Description

Table 52. Boot Signal Pin Description

Signal	Pin number	I/O	I/O type	Description
BOOT	W18	I	1V8	Download mode selection

3.17.3. Application

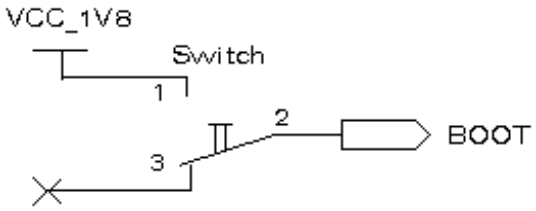


Figure 43. Example of BOOT Pin Implementation

3.18. Reset Signals

The module has two reset signals. The main is ~RESET which is the input reset of the module. The second is ~EXT-RESET which is derived from the main reset.

3.18.1. Features

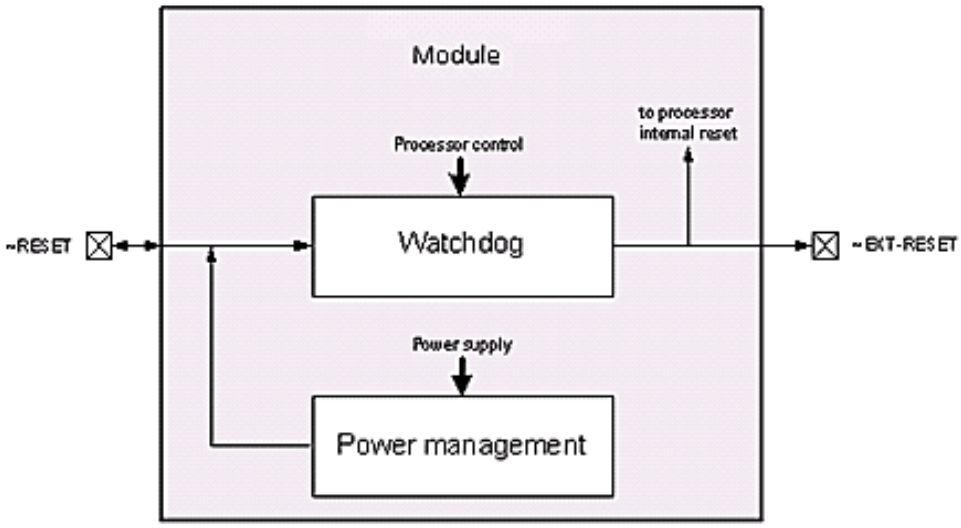


Figure 44. Reset Functional Block Diagram

The ~RESET signal is an input/output signal. It is controlled by the user as well as by an internal voltage supervisor. This ~RESET signal drives the reset of the processor through the watchdog unit.

The ~EXT-RESET is an output signal and is the result of the combination of the ~RESET and the watchdog reset. This signal is used to provide a reset to all the system components. Typically, the ~EXT-RESET is used to reset the NOR Flash memories state machine.

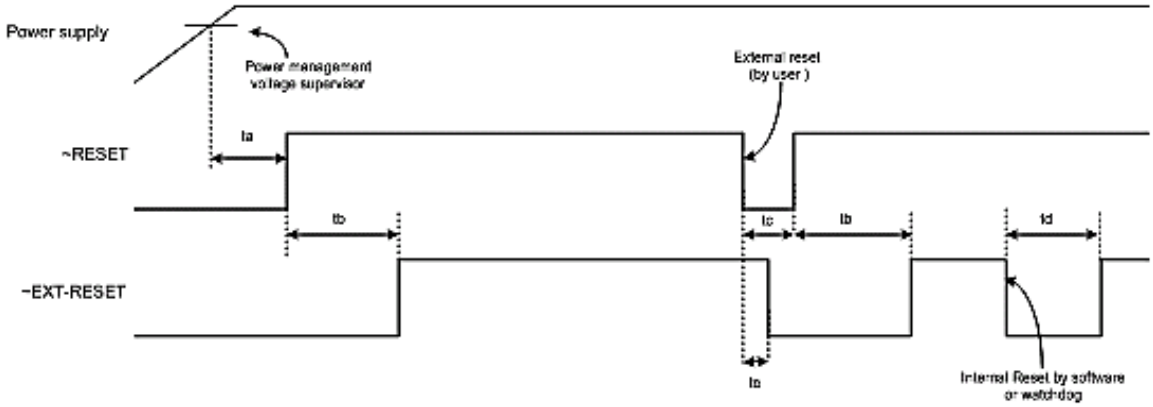


Figure 45. Reset Waveform Events

Three different reset events can occur as explained in the following subsections.

3.18.1.1. Power-on Reset

The power on reset is automatically controlled by the internal power management unit. It resets the ~RESET signal as long as the power supply voltage VCC_1V8 is under 1.60 V typ.

The ~RESET is always reset when the VCC_1V8 is high, after a cancellation time is launched (ta).

The ~EXT-RESET is always reset when the ~RESET signal is high, after a cancellation time is launched (tb).

3.18.1.2. External Reset (~RESET)

The external reset is managed by the user or by an external event of the module. This is the asynchronous reset of the module. The external reset must be generated on the ~RESET signal.

The ~Reset signal must be held low during the time (tc) to reset the module.

3.18.1.3. Internal Reset (~EXT-RESET)

The internal reset is launched by the watchdog unit, controlled by the processor. This reset affects only the ~EXT-RESET signal (td).

Sequence after an external reset event (~RESET):

To activate the « emergency » reset sequence, the ~RESET signal has to be set to low for 200µs minimum for example by a push button . As soon as the reset is complete, the interface answers « OK » to the application.

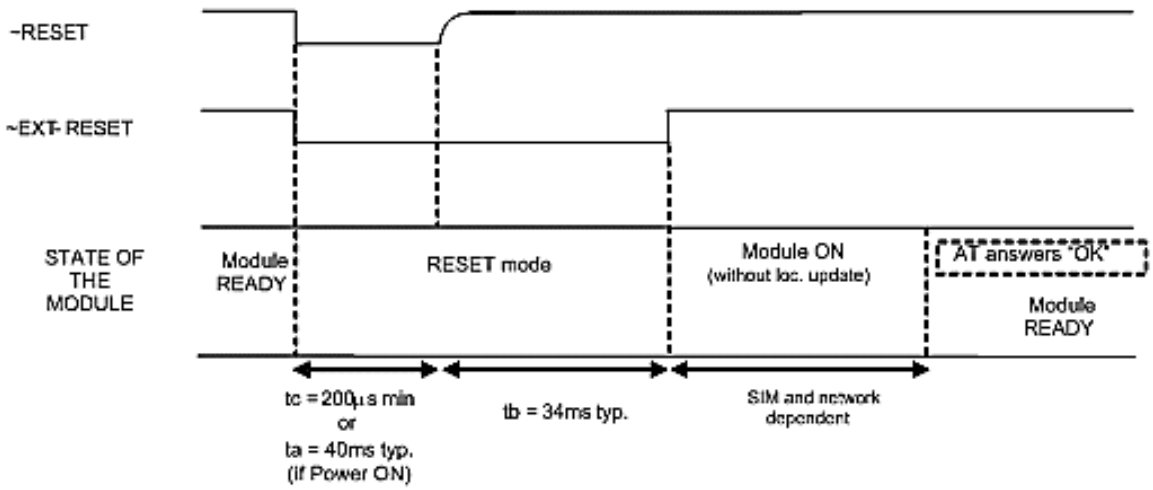


Figure 46. Reset Sequence Waveform

At power up, the ~RESET time (ta), is performed after switching ON the module. It is generated by the internal voltage supervisor of module.

The ~RESET time is provided by the internal RC component. To keep the same time, it's not recommended to plug another R or C component into the ~RESET signal. Only a switch or an open drain gate is recommended.

The (tb) time is the cancellation time needed for the module initialization. (tb) time is automatically done by the module itself, after a hardware reset.

The firsts access on ~CS0 after an internal reset event (~EXT-RESET):

After an internal reset (like a Watchdog reset) the delay of the active ~CS0 signal (chip select 0 for access to the external FLASH) depend of the BOOT signal state. Refer to section 3.17, BOOT Signal for further details about BOOT signal.

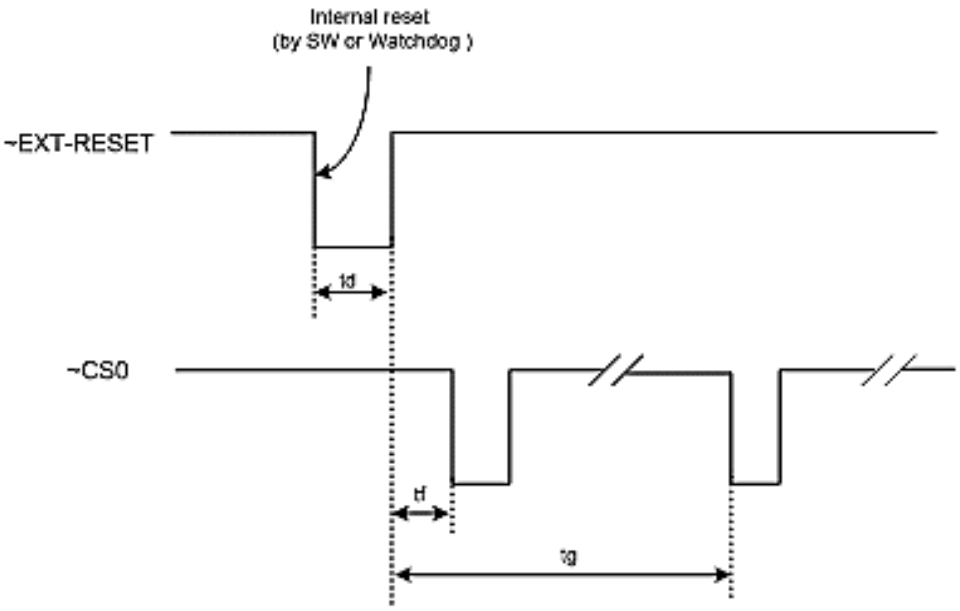


Figure 47. Boot Sequence Waveform

3.18.2. Pin Description

Table 53. Reset Signal Pin Description

Signal	Pin Number	I/O	I/O Type	Description
~RESET	V6	I/O Open Drain*	1V8	Module Reset
~EXT-RESET	AB14	O Push Drain	1V8	External Reset

(*): Internal pull-up. Refer to section 3.3, "Electrical Information for Digital I/O" for Open drain, 2V8 and 1V8 voltage characteristics and for Reset state definition.

3.18.3. Electrical Characteristics

Table 54. Electrical Characteristics of Reset Signal

Parameter			Minimum	Typical	Maximum	Unit
~RESET	Input Impedance (R)[1]			100K		Ω
	Input Impedance (C)			10n		F
	~Reset time (tc)		200			µs
	Cancellation time (ta) at power up only		20	40	100	ms
	VH[2]		0.57			V
	VIL		0		0.57	V
	VIH		1.33			V
~EXT-RESET	Watchdog reset (td)			300		µs
	Cancellation time (tb)			34	35	ms
	Delay after a ~RESET active (te)				122	µs
~CS0	First access time (tf)			17		µs
	Total boot time (tg)	BOOT = 1			200	ms
		BOOT = Leave open[3]			20	

(1): Internal pull-up

(2): V_H: Hysterisis Voltage

(3): Normal configuration. Refer to chapter 3.17, BOOT Signal for further details on the BOOT signal.

3.18.4. Application

If used (emergency reset), it has to be driven by an open collector or an open drain output (due to the internal pull-up resistor embedded into the module) as shown in the diagram hereunder.

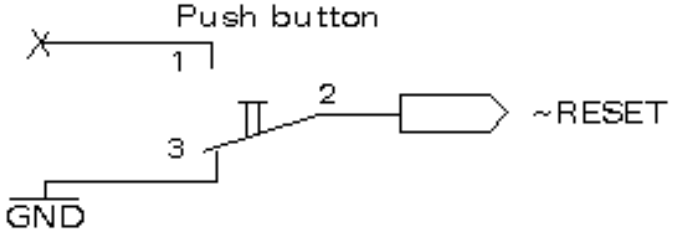


Figure 48. Example of ~RESET Pin Connection with Push Button Configuration

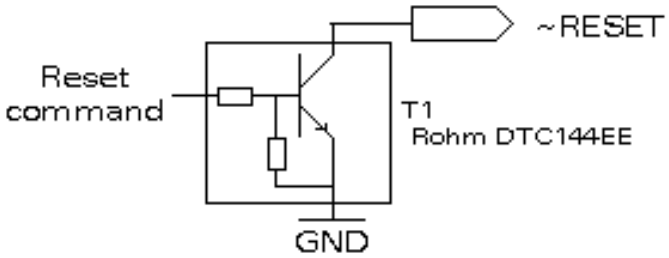


Figure 49. Example of ~RESET Pin Connection with Transistor Configuration

Open collector or open drain transistor can be used. If an open collector is chosen, T1 can be a Rohm DTC144EE.

Table 55. Reset Settings

Reset command	~RESET	Operating mode
1	0	Reset activated
0	1	Reset inactive

3.19. External Interrupt

The WMP50 embedded module supports up to five (5) external interrupts in two voltage ranges (1.8V and 2.8V); while the WMP100, WMP150, WMP100 ESIM and WMP150 ESIM embedded modules provide up to eleven (11) external interrupts, also in two voltage ranges (1.8V and 2.8V).

3.19.1. Features

Those interrupt inputs can be activated on:

- high to low edge
- low to high edge
- low to high and high to low edge
- Programmable debounce from 0 to 54ms by 7.8ms steps
- Asynchronous stretching to detect short events
- Bypass mode

When used, the interrupt inputs must not be left open; and when they are not used, they must be configured as GPIOs.

3.19.2. Pin Description

Table 56. External Input/Interrupt Pin Description for the WMP50 Embedded Module

Signal	Pin Number	I/O	I/O Type	Reset State	Description	Multiplexed with
INT0	Y19	I	2V8	Z	External Interrupt 0	Not mux
INT1	V18	I	2V8	Z	External Interrupt 1	Not mux

Signal	Pin Number	I/O	I/O Type	Reset State	Description	Multiplexed with
INT2	T13	I	2V8	1	External Interrupt 2	CT104/RXD1
INT3	M16	I	2V8	Z	External Interrupt 3	~CT108-2/DTR1
INT4	U17	I	1V8	0	External Interrupt 4	CT104/RXD2

Table 57. External Input/Interrupt Pin Description for the WMP100, WMP150, WMP100ESIM and WMP150ESIM Embedded Modules

Signal	Pin Number	I/O	I/O Type	Reset State	Description	Multiplexed with
INT0	V16	I	1V8	Z	External Interrupt 0	GPIO3 / A26
INT1	Y19	I	2V8	Z	External Interrupt 1	GPIO25
INT2	Y17	I	1V8	1	External Interrupt 2	GPIO45
INT3	V18	I	2V8	Z	External Interrupt 3	GPIO46
INT4	T18	I	2V8	Z	External Interrupt 4	GPIO35 / SPI2-LOAD
INT5	M14	I	2V8	Z	External Interrupt 5	GPIO31 / SPI1-LOAD
INT6	T16	I	1V8	Z	External Interrupt 6	GPIO14 / CT103/TXD2
INT7	V13	I	1V8	Z	External Interrupt 7	GPIO17 / ~CT105/RTS2
INT8	Y3	I	1V8	Z	External Interrupt 8	GPIO18 / SIMPRES
INT9	T13	I	2V8	Z	External Interrupt 9	GPIO37 / CT104/RXD1
INT10	M16	I	2V8	Z	External Interrupt 10	GPIO41 / ~CT108-2/DTR1
INT11	U17	I	1V8	0	External Interrupt 11	GPIO15 / CT104/RXD2

Refer to section 3.3, "Electrical Information for Digital I/O" for Open drain, 2V8 and 1V8 voltage characteristics and for Reset state definition.

3.19.3. Electrical Characteristics

Table 58. Electrical Characteristics of External Input/Interrupt

Parameter		Minimum	Maximum	Unit
Interrupt pin at 1V8	V_{IL}		0.54	V
	V_{IH}	1.33		V
Interrupt pin at 2V8	V_{IL}		0.84	V
	V_{IH}	1.96		V

3.19.4. Application

INTx (except for INT2) are high impedance input types, so it is important to set the interrupt input signal with pull up or pull down resistor if they are driven by an open drain, open collector or by a switch. If they are driven by a push-pull transistor, no pull up or pull down resistor is necessary.

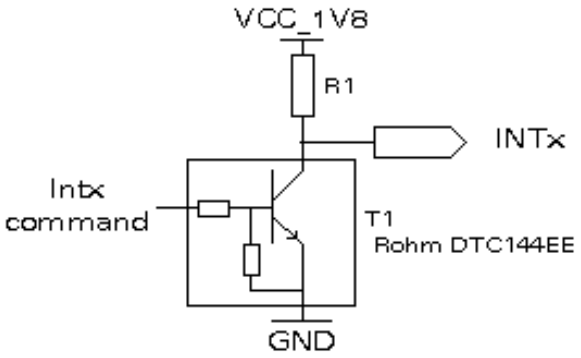


Figure 50. Example of INTx Driven by an Open Collector with Voltage 1.8V

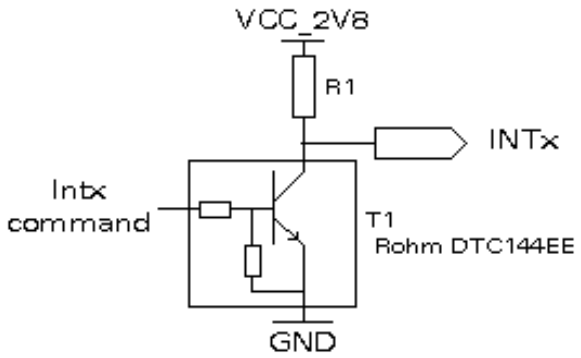


Figure 51. Example of INTx Driven by an Open Collector with Voltage 2.8V

Where:

- R1 value can be 47K Ohm.
- T1 can be a Rohm DTC144EE open collector transistor.

3.20. VCC_2V8 and VCC_1V8 output

VCC_2V8 output can be used only for pull-up resistor and can be used as a reference supply.

VCC_1V8 output is used to supply voltage for Flash and Ram memories; it can be used as well for pull-up resistors.

These voltage supplies are available when the module is on.

3.20.1. Pin Description

Table 59. VCC_2V8 and VCC_1V8 Pin Description

Signal	Pin Number	I/O	I/O Type	Description
VCC_1V8	AD5	O	Supply	Digital supply

Signal	Pin Number	I/O	I/O Type	Description
VCC_2V8	R1	O	Supply	Digital supply

Refer to section 3.3, "Electrical Information for Digital I/O" for Open drain, 2V8 and 1V8 voltage characteristics and for Reset state definition.

3.20.2. Electrical characteristics

Table 60. Electrical Characteristics of the VCC_2V8 and VCC_1V8 Signals

Parameter		Minimum	Typical	Maximum	Unit
VCC_1V8	Output Voltage	1.76	1.8	1.94	V
	Output Current			80*	mA
VCC_2V8	Output Voltage	2.74	2.8	2.86	V
	Output Current			15	mA

(*): Without the memory connected (Plan 60mA MAX for the memory, refer to the reference in section 3.27, Memory Interface).

3.20.3. Application

These digital power supplies are mainly used to:

- VCC_1V8 is used to supply Flash and Ram memory devices
- pull-up signals such as I/O
- supply the digital transistors driving LEDs
- supply the SIMPRES signal
- act as a voltage reference for ADC interface AUX-ADC (only for VCC_2V8)

3.21. Real Time Clock

The Real Time Clock of the module needs to be fed by a 32768Hz frequency. An internal oscillator is available to drive a crystal at the frequency of 32768Hz.

3.21.1. Features

Two pins are used to connect a crystal which is mandatory to setup and to run the module.

It is possible to access the 32768 Hz signal (buffered output) on GPIO44 (ball AB13); refer to the Analog-to-Digital Converter section for more information. For additional information regarding the use of the 32 kHz internal clock in Slow Idle Mode, refer to section 4.2.2.2, SLEEP Mode with GSM Stack in Idle.

Caution: *Ensure that the 32KHz clock is perfectly stable before starting up the AirPrime WMP module.*

3.21.2. Pin Description

Table 61. Real Time Clock Pin Description

Signal	Pin Number	I/O	I/O Type	Description
XIN_32K	AC24	I	analog	Oscillator input
XOUT_32K	AB24	O	analog	Oscillator output

3.21.3. Electrical Characteristics

Table 62. Electrical Characteristics of Real Time Clock Signals

Parameter		Minimum	Typical	Maximum	Unit
XIN_32K	32kHz oscillator input cycle time	-	1/32768	-	µs
	32kHz oscillator input high time	5	-	-	µs
	32kHz oscillator input low time	5	-	-	µs
Start Time	32kHz oscillator start time	-	-	2	s
GPIO44	Delay time with respect to XIN_32K	-	-	20	ns

3.21.4. Application

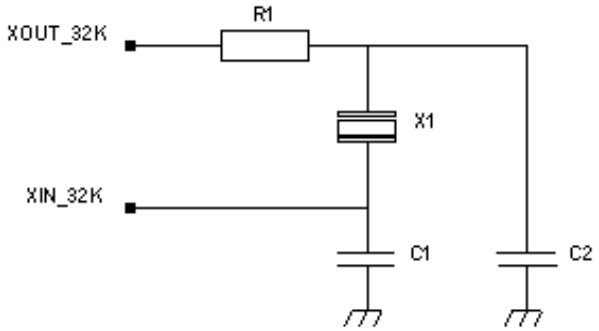


Figure 52. Example of a Real Time Clock Application

The R1 resistor is mandatory if the crystal maximum power dissipation is under 1µW.

The value of the components R1, C1 and C2 are tuned with the crystal MS3V-T1R.

It is important to place the crystal close to the module, to reduce to a minimum the length of the nets.

Recommended components:

- C1, C2 : 22pF
- R1 : 100Kohm
- X1: 32768Hz crystal. MS3V-T1R (+/- 20ppm @25°C) Microcrystal

3.21.5. Design Recommendations

The example below with the crystal MS3V-T1R is to illustrate the design.

Layer 1:

- Good ground under the crystal.
- Good ground connection of the crystal legs and the load capacitance of the crystal.
- Crystal as close as possible to the module in order to decreases as maximum as possible the parasite capacitance brought by the design of the layout

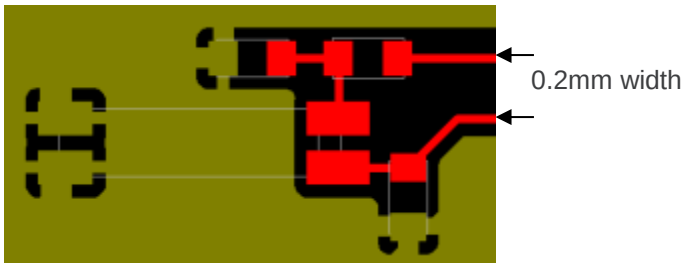


Figure 53. PCB Lay-out for the Crystal MS3V-T1R

Layer 2:

A complete layer of ground

3.22. BAT-RTC (Backup Battery)

The module provides an input/output to connect a Real Time Clock power supply.

3.22.1. Features

This pin is used as a back-up power supply for the internal **R**eal **T**ime **C**lock (RTC). The RTC is supported by the module when VBATT is available, but a back-up power supply is needed to save the date and hour when VBATT is removed.

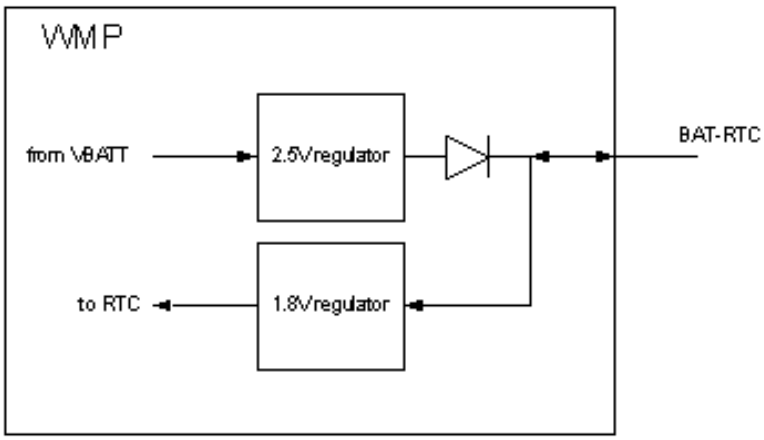


Figure 54. Real Time Clock Power Supply

If the RTC is not used this pin can be left open. If the VBATT is available, the back-up battery can be charged by the internal 2.5V power supply regulator.

3.22.2. Pin Description

Table 63. BAT-RTC Pin Description

Signal	Pin Number	I/O	I/O Type	Description
BAT-RTC	U6	I/O	Supply	RTC Back-up supply

3.22.3. Electrical Characteristics

Table 64. Electrical Characteristics of BAT-RTC Interface

Parameter	Minimum	Typical	Maximum	Unit
Input voltage	1.85		3.0	V
Input current consumption*		3.3		µA
Output voltage		2.45		V
Output current			2	mA

(*): Provided by a RTC back-up battery when the modules are off and VBATT = 0V.

If VBATT is present, refer to the consumption tables in section 4.3 and in particular the Alarm mode line.

3.22.4. Application

Back-up Power Supply can be provided by:

- A super capacitor
- A non rechargeable battery
- A rechargeable battery cell

3.22.4.1. Super Capacitor

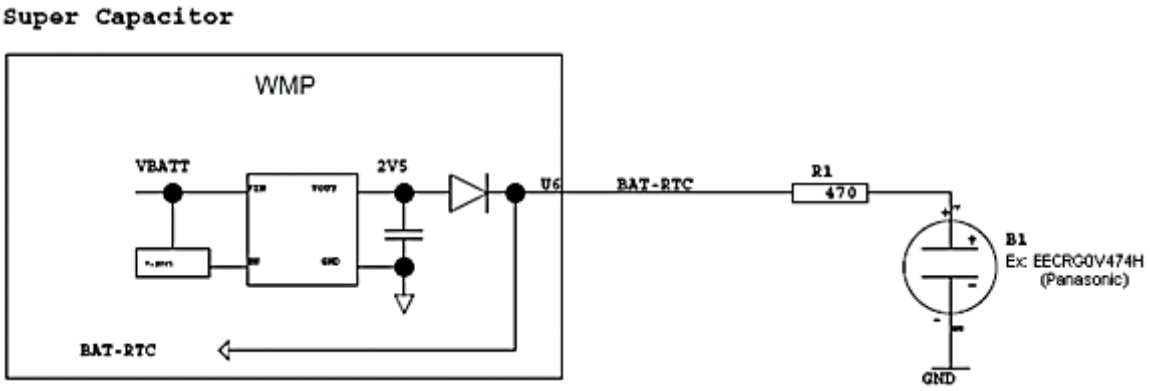


Figure 55. RTC Supplied by a Gold Capacitor

Estimated range with 0.47 Farad Gold Capacitor: 25 hours for 3µA.

Note: The gold capacitor maximum voltage is 2.5V.

3.22.4.2. Non Rechargeable Battery

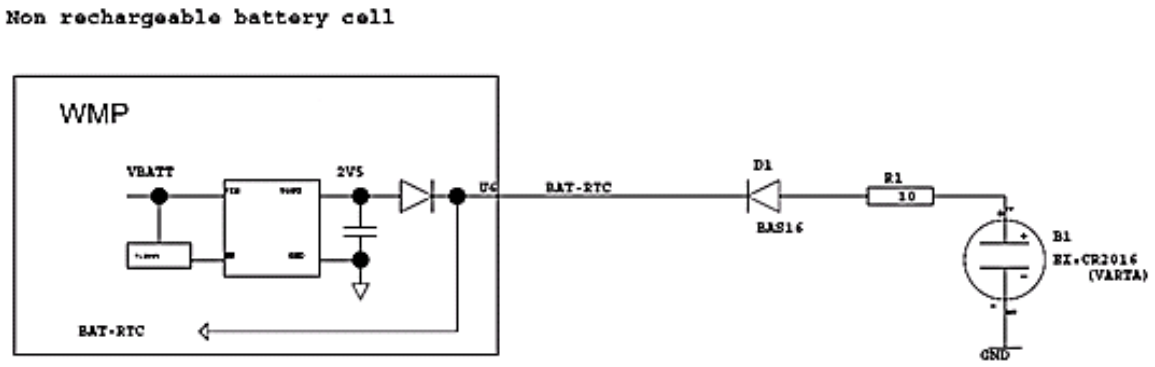


Figure 56. RTC Supplied by a Non-Rechargeable Battery

The diode D1 is mandatory to not damage the non rechargeable battery.

Estimated range with 85mAh battery: 800 H minimum.

3.22.4.3. Rechargeable Battery Cell

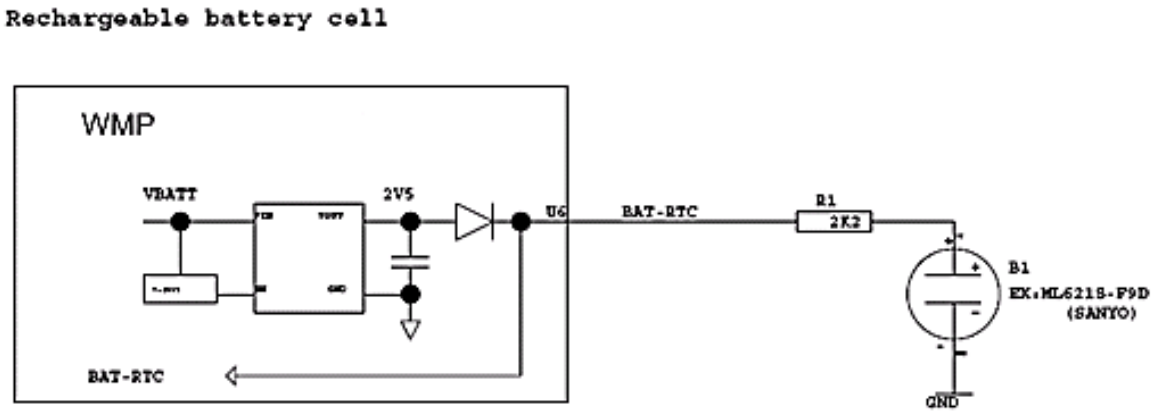


Figure 57. RTC Supplied by a Rechargeable Battery

Estimated range with 2mAh rechargeable battery: ~15 hours.

Warning: *Before battery cell assembly ensure that cell voltage is equal or lower than 3.0 V to avoid any damage to the module.*

3.23. LED0 Signal

3.23.1. Features

LED0 is an open drain output. An LED and a resistor can be directly connected between this output and VBATT.

When the module is OFF, if 2.8[1]V < VBATT < 3.2V and a charger is connected on the CHG-IN inputs, this output indicates, by flashing (100 ms ON, 900 ms OFF) , the pre-charging phase of the battery.

When the module is ON, this output is used to indicate the network status.

Table 65. FLASH-LED Status

State	VBATT Status	LED0 Status	WMP Status
OFF	VBATT<2.81V or VBATT> 3.2V	OFF	OFF
	2.81V < VBATT < 3.2V	Pre-charge flash LED ON for 100 ms, OFF for 900 ms	OFF, Pre-charging mode (charger must be connected on CHG-IN to activate this mode)
ON	VBATT > 3.2V	Permanent	ON, not registered on the network
		Slow flash LED ON for 200 ms, OFF for 2 s	ON, registered on the network
		Quick flash LED ON for 200 ms, OFF for 600 ms	ON, registered on the network, communication in progress
		Very quick flash LED ON for 100ms, OFF for 200ms	ON, software downloaded is either corrupted or non-compatible ("BAD SOFTWARE")

(1): Refer to the WARNING in section 3.15, Battery Charging Interface.

3.23.2. Pin Description

Table 66. FLASH-LED Pin Description

Signal	Pin Number	I/O	I/O Type	Reset State	Description
LED0	U3	O	Open Drain Output	1 *	LED driving

(*): This signal is undefined 2 seconds after the reset (initialization time).

Refer to section 3.3, "Electrical Information for Digital I/O" for Open drain, 2V8 and 1V8 voltage characteristics and for Reset state definition.

3.23.3. Electrical Characteristics

Table 67. Electrical Characteristics of the FLASH-LED Signal

Parameter	Condition	Minimum	Typical	Maximum	Unit
V_{OL}				0.4	V
I_{OUT}				8	mA

The LED0 state is high during the RESET time and undefined during the software initialization time. During software initialization time, during 2 seconds max after RESET cancellation, the LED0 signal is toggling and it doesn't provide the module status. After the 2s, the LED0 provides the true status of the module.

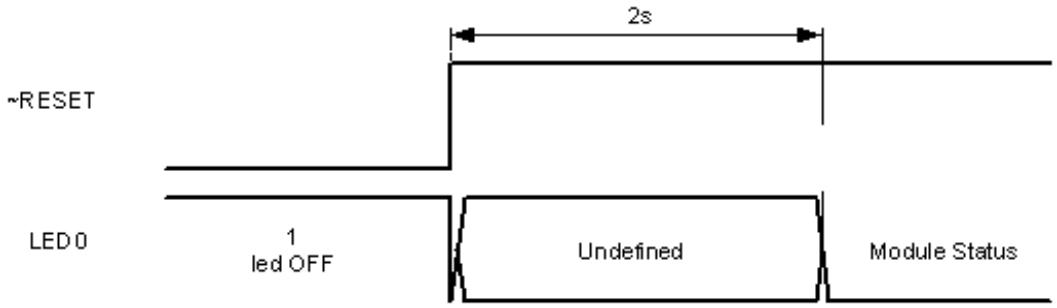


Figure 58. LED0 State During RESET and Initialization Time

3.23.4. Application

The GSM activity status indication signals LED0 (pin U3) can be used to drive a LED. This signal is an open-drain digital transistor according to the module activity status.

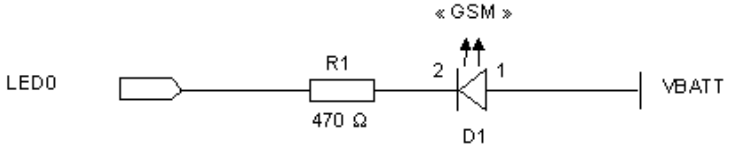


Figure 59. Example of GSM Activity Status Implementation

The value of R1 can be harmonized depending on the LED (D1) characteristics.

3.24. Digital Audio Interface (PCM)

The Digital audio interface (PCM) interface mode allows connectivity with standard audio peripherals. It can be used, for example, for connecting an external audio codec.

The programmability of this mode addresses a large range of audio peripherals.

Note: The AirPrime WMP50 does not have this capability. This section applies only to the WMP100 and WMP150 modules.

3.24.1. Features

PCM interface consists of 4 wires:

- PCM-SYNC (output): The frame synchronization signal delivers an 8KHz frequency pulse that synchronizes the frame data in and the frame data out.
- PCM-CLK (output): The frame bit clock signal controls the data transfer with the audio peripheral.
- PCM-OUT (output): The frame “data out” depends on the selected configuration mode.
- PCM-IN (input): The frame “data in” depends on the selected configuration mode.

The PCM-IN signal should be in HZ out of user slot. The Digital Audio Interface also features the following:

- IOM-2 compatible device on physical level
- Master mode only with 6 slots by frame, user only on slot 0
- Bit rate single clock mode at 768KHz only

- 16 bits data word MSB first only
- Linear Law only (no compression law)
- Long Frame Synchronization only
- Push pull configuration on PCM-OUT and PCM-IN

Note that the digital audio interface configuration cannot differ from those specified above.

3.24.2. Pin Description

Signal	Pin Number	I/O	I/O Type	Reset State	Description
PCM-SYNC	Y21	O	1V8	Pull down	Frame synchronization 8kHz
PCM-CLK	W21	O	1V8	Pull down	Data clock
PCM-OUT	W22	O	1V8	Pull up	Data output
PCM-IN	AA22	I	1V8	Pull up	Data input

Refer to section 3.3, "Electrical Information for Digital I/O" for Open drain, 2V8 and 1V8 voltage characteristics and for Reset state definition.

3.24.3. AC Characteristics

Table 68. AC Characteristics of the Digital Audio Interface

Signal	Description	Minimum	Typical	Maximum	Unit
$T_{sync\_low} + T_{sync\_high}$	PCM-SYNC period		125		µs
T_{sync_low}	PCM-SYNC low time		93		µs
T_{sync_high}	PCM-SYNC high time		32		µs
$T_{SYNC-CLK}$	PCM-SYNC to PCM-CLK time		-154		ns
$T_{CLK-cycle}$	PCM-CLK period		1302		ns
$T_{IN-setup}$	PCM-IN setup time	50			ns
$T_{IN-hold}$	PCM-IN hold time	50			ns
$T_{OUT-delay}$	PCM-OUT delay time			20	ns

3.24.4. PCM Waveforms

The following figures describe the PCM frame and sampling waveforms.

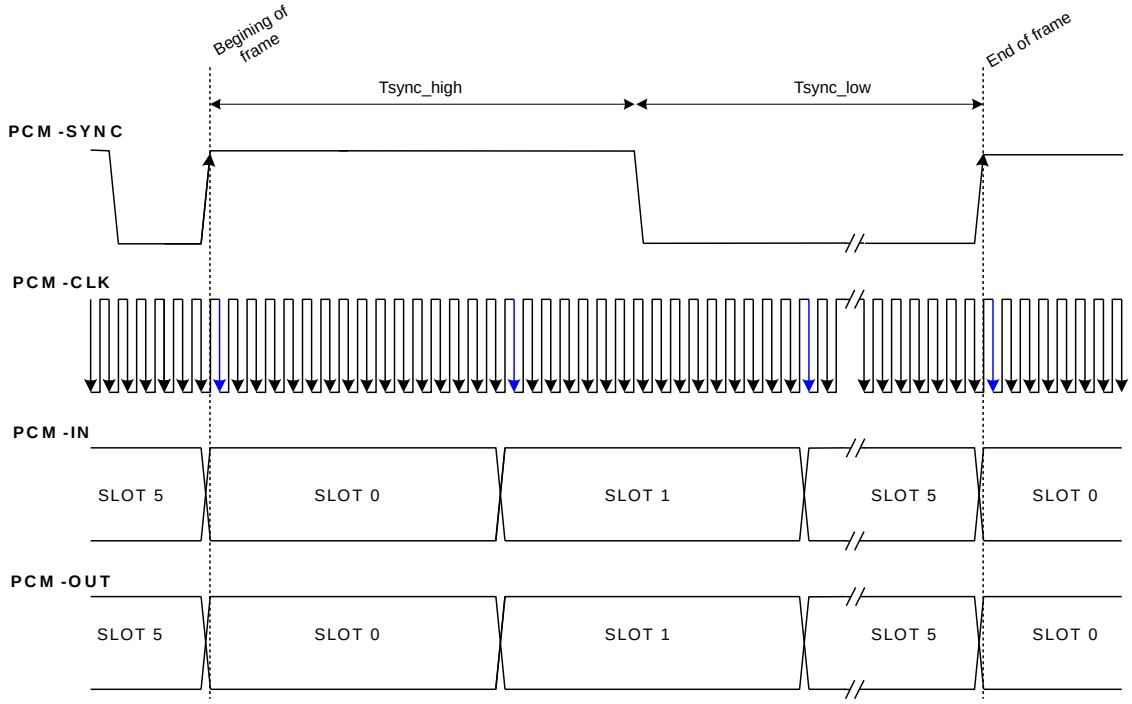


Figure 60. PCM Frame Waveform

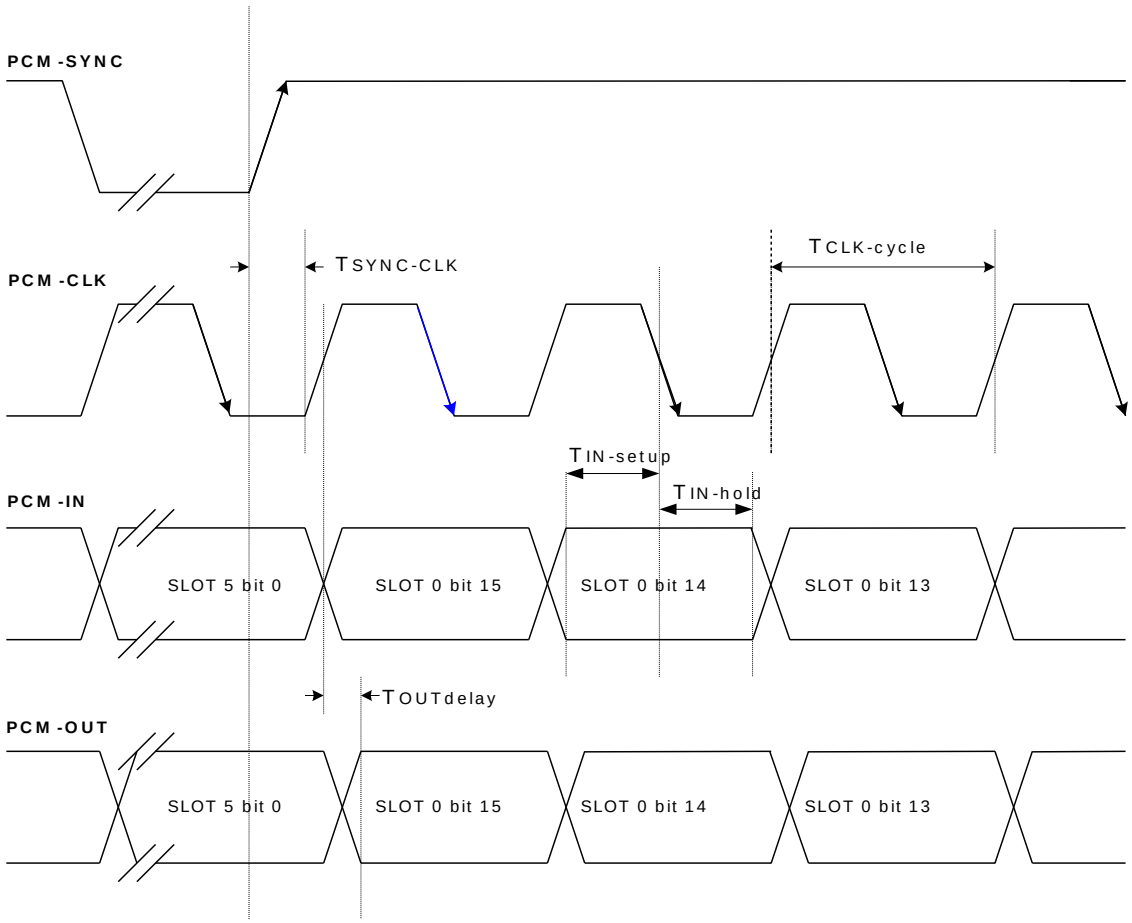


Figure 61. PCM Sampling Waveform

3.25. USB 2.0 Interface

A 5-wire USB slave interface is available, complying with USB 2.0 protocol signaling, but not with electrical interface, due to the not complying 5V of VPAD-USB.

The USB interface signals are VPAD-USB, USB-DP, USB-DM, USB-DET, USB-CN and GND.

3.25.1. Features

- 12Mbit/s full speed transfer rate
- 3.3V typical compatible
- USB Softconnect feature
- Download feature is not supported by USB
- CDC 1.1 – ACM compliant

Note: A 5V to 3.3V typical voltage regulator is needed between the external interface power in line (+5V) and the module line (VPAD-USB).

3.25.2. Pin Description

Refer to the following table for the pin description of the USB interface.

Table 69. USB Pin Description

Signal	Pin Number	I/O	I/O Type	Description	Multiplexed with
VPAD-USB	AB19	I	VPAD_USB	USB Power Supply	Not mux
USB-DP	W19	I/O	VPAD_USB	Differential data interface positive	Not mux
USB-DM	AA20	I/O	VPAD_USB	Differential data interface negative	Not mux
USB-CN	Y20	O	VPAD_USB	Connect (high or low speed)	Not mux
USB-DET	R14	I	VCC_1V8	Detection	Not mux

3.25.3. Electrical Characteristics

Table 70. Electrical Characteristics of the USB Interface

Parameter	Min.	Typ.	Max.	Unit
VPAD-USB, USB-DP, USB-DM, USB-CN	3	3.3	3.6	V
VPAD-USB Input current consumption		8		mA

3.25.4. Application

A typical schematic is shown below:

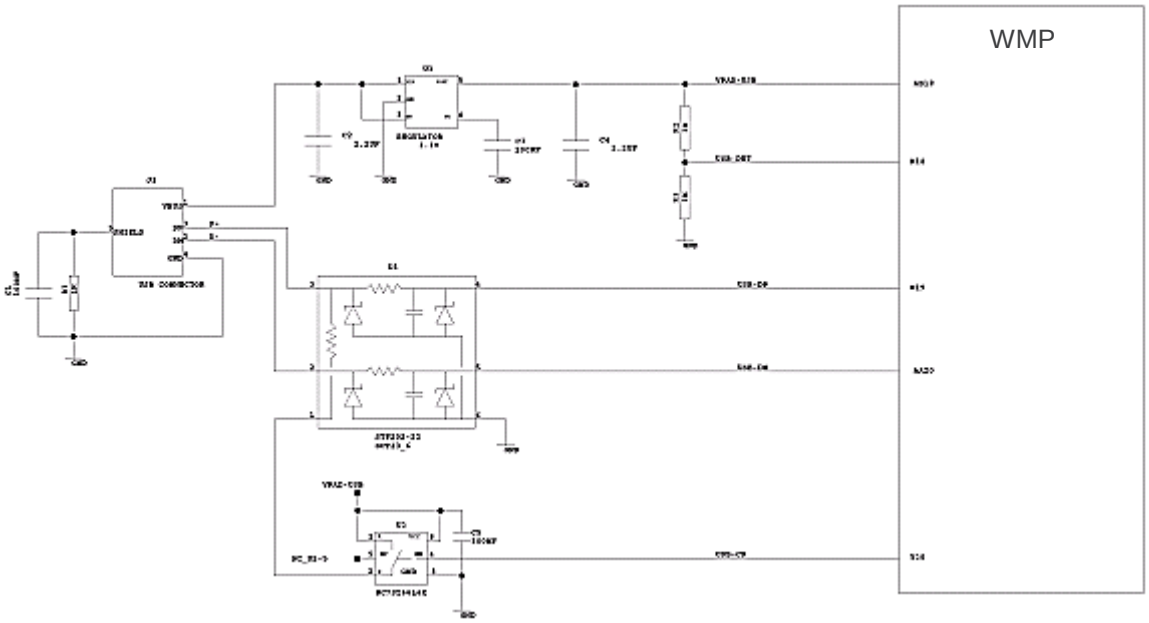


Figure 62. Example of a USB Implementation

The regulator used is a 3.3V one. It is supplied through J1 when the USB wire is plugged.

USB-DET is an external Interruption (R14) used for the USB wire presence detection.

The EMI/RFI filter with ESD protection is D1. The D1 integrated pull up resistor is used to detect full speed. USB-CN (Y20) drives this pull-up.

R1 and C1 have to be close to J1.

Recommended Components:

- R1,R2, R3 : 1MOhm
- C1, C3 : 100nF
- C2, C4 : 2.2µF
- D1 : STF202-22 from SEMTECH
- U1 : LP2985AIM 3.3V from NATIONAL SEMICONDUCTOR
- U2 : NC7SZ66L6X from FAIRCHILD

3.26. JTAG Interface

This is an in-circuit debugging solution capable of tracking down issues which may occur in routines but cannot be reproduced with the Remote Tasks Environment. That can step through the code of their application on the module.

We recommend to plan an access to the JTAG pins* on customer PCB for hardware debugging purpose. The JTAG interface should then be use to test the hardware without software running on the system. (The JTAG is locked for software debugging on the mass production version of the module).

A 6-wire JTAG interface is available powered to 1.8V. The JTAG interface signals are TDI, TMS, TCK, RTCK, TDO, ~TRST.

(*): Refer to the “reserved” balls in the Ball Grid Array pin out in section 5.1.

3.26.1. Features

- In-circuit debugging
- Step-over and step-in debugging operations
- Setting breakpoints and watchpoints
- Run, break, and continue debugging operations
- Memory retrieval and modification capabilities

3.26.2. Pin Description

Table 71. JTAG Interface Pin Description

Signal	Pin Number	I/O	I/O Type	Description	Multiplexed with
TDI	V19	I	1V8	JTAG input data	Not mux
TMS	P16	I	1V8	JTAG test mode select	Not mux
TCK	P17	I	1V8	JTAG scan clock	Not mux
RTCK	AB20	O	1V8	JTAG return test clock from the ARM JTAG for external debug HW	Not mux
TDO	R16	O	1V8	JTAG output data	Not mux
~TRST	W20	I	1V8	JTAG asynchronous reset	Not mux
BOOT	W18	I	1V8	Must be connected to high level1 to select the ARM946 JTAG module	Not mux
VCC_1V8	AD5	O	1V8	Digital Supply	Not mux
GND	AD62	-	-	GROUND	Not mux

(1): Refer to the BOOT paragraph in section 3.17.

(2): For example.

3.26.3. Application

A typical schematic is shown below:

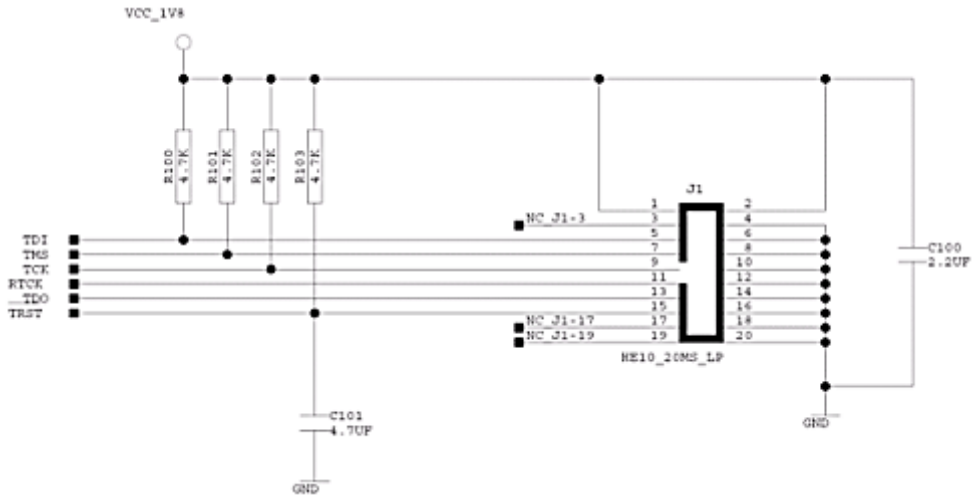


Figure 63. Example of a JTAG Implementation

Recommended Components

- R100,R101, R102, R103 : 4.7kOhm
- C101: 4.7µF

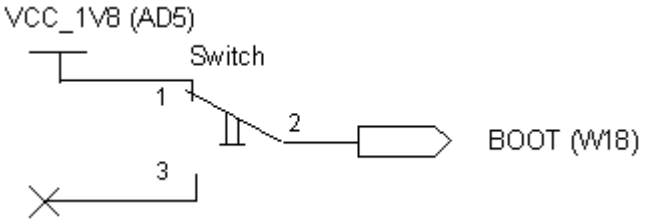


Figure 64. Example of a Boot Signal Configuration

Note: Typically, if the BOOT signal is not connected to HIGH level, the JTAG debugging interface cannot run.

3.27. Memory Interface

The memory interface is used to connect many memory parts technologies including Flash NOR, Flash NAND, SRAM and PSRAM components.

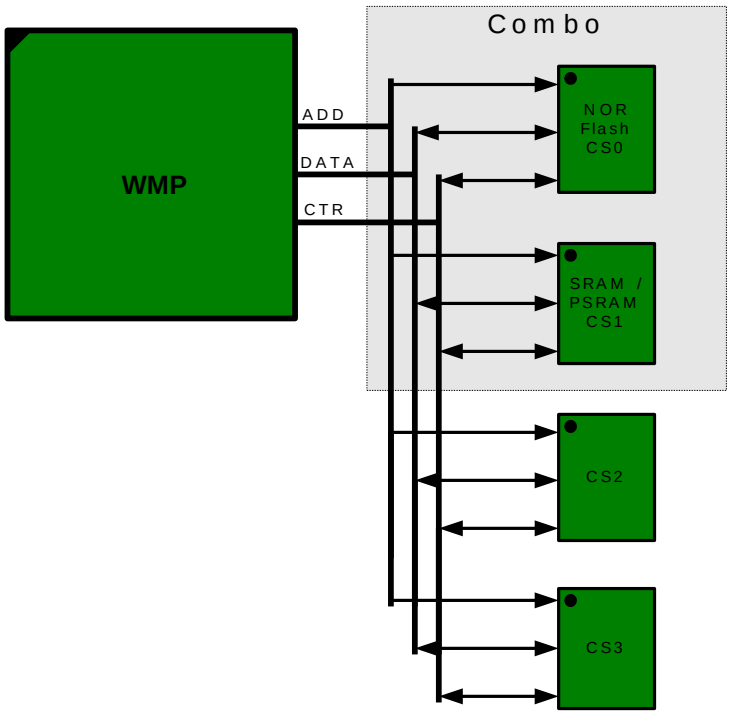


Figure 65. Memory Bus

The interface is able to drive up to 4 independents memories. Some memories can be enclosed in the same package, like the Combo memories.

Each Chip select space can be configured independently.

It is mandatory that the memory connected on CS0 is the FLASH and CS1 is the RAM. Because the parallel interface parameters are already automatically set up on chip selects CS0 and CS1, they are inaccessible to the user. Two chip selects remain open for use.

3.27.1. Features

3.27.1.1. Generic Description

- Up to 128 MByte address range per chip select (~CS0 and ~CS1 only)
- Up to 4 chip select available
- Support for 8, 16, and 32 bit (multiplexed synchronous mode) devices
- Byte enable signals for 16 bit and 32 bits operation
- Fully programmable timings based on hclk (a division of the ARM clock) cycles (except for synchronous mode which is based on CLKBURST cycles)
  - individually selectable timings for read and write
  - 0 to 7 clock cycles for setup
  - 1 to 32 clock cycles for access cycle
  - 1 to 8 clock cycles for page access cycle
  - 0 to 7 clock cycles for hold
  - 1 to 15 clock cycles for turnaround
- Page mode Flash memory support
  - page size of 4, 8, 16 or 32
- Burst mode Flash memory support up to hclk clock frequency (for devices sensitive to rising edge of the clock only)
  - hclk, hclk/2, hclk/4 or hclk/8 burst clock output
  - burst size of 4, 8, 16, 32
  - WAIT input
  - automatic CLKBURST power-down between accesses
- Intel mode (WE and OE) and Motorola mode (E and R/W) control signals
- Synchronous write mode
- Synchronous multiplexed data/address mode (x32 mode)
- Adaptation to word, halfword, and byte accesses to the external devices

3.27.1.2. Memory Configuration

Several memories configuration are possible in function of the module and the firmware used.

Two kinds of packaging are suggested:

- The combo memory (Flash and RAM dies are stacked inside the same package).
- The discrete memories (Flash and RAM are stand-alone)

Table 72. Memory Configuration

	FLASH (Mb) (stand-alone)	PSRAM(Mb) (stand-alone)	COMBO (Mb) (Flash/PSRAM)	Open AT Framework version
WMP50	N/A	N/A	32/16	R7.44
	N/A	N/A	64/16	R7.44
WMP100, WMP100 Embedded SIM	N/A	N/A	32/16	R7.44
	N/A	N/A	64/16	R7.44

	FLASH (Mb) (stand-alone)	PSRAM(Mb) (stand-alone)	COMBO (Mb) (Flash/PSRAM)	Open AT Framework version
WMP150, WMP150 Embedded SIM	32	128	N/A	R7.44
	64	16	N/A	R7.44
	64	32	N/A	R7.44
	N/A	N/A	32/16	R7.44
	N/A	N/A	64/16	R7.44

The following bus widths and modes combinations are not allowed on WMP100:

- With Asynchronous transfer mode, the bus width "32-bits non multiplexed" is not available.
- The "16-bits multiplexed" and "32-bits multiplexed" widths are allowed only with the "Synchronous read and synchronous write" transfer modes.

3.27.1.3. Memories References (Combo and Stand-alone)

For the stand alone memories:

- The FLASH 32Mbits from STMicroelectronics : M58WR032KT70ZB6F
- The FLASH 64Mbits from STMicroelectronics : M58WR064HT70ZB6F
- The PSRAM 16Mbits from Micron Technology : MT45W1MW16BDGB-701 IT
- The PSRAM 32Mbits from Micron Technology : MT45W2MW16BGB-701 IT
- The PSRAM 128Mbits from Micron Technology : MT45W8MW16BGX-701 IT

For the combo memories:

- The COMBO Flash/PSRAM 32/16Mbits from STMicroelectronics : M36W0R5040T5ZAQF
- The COMBO Flash/PSRAM 64/16Mbits from STMicroelectronics : M36W0R6040T7ZAQF

  M36W0R6040T8ZAQF

3.27.1.4. Open AT Framework 2.01 Flash Mapping

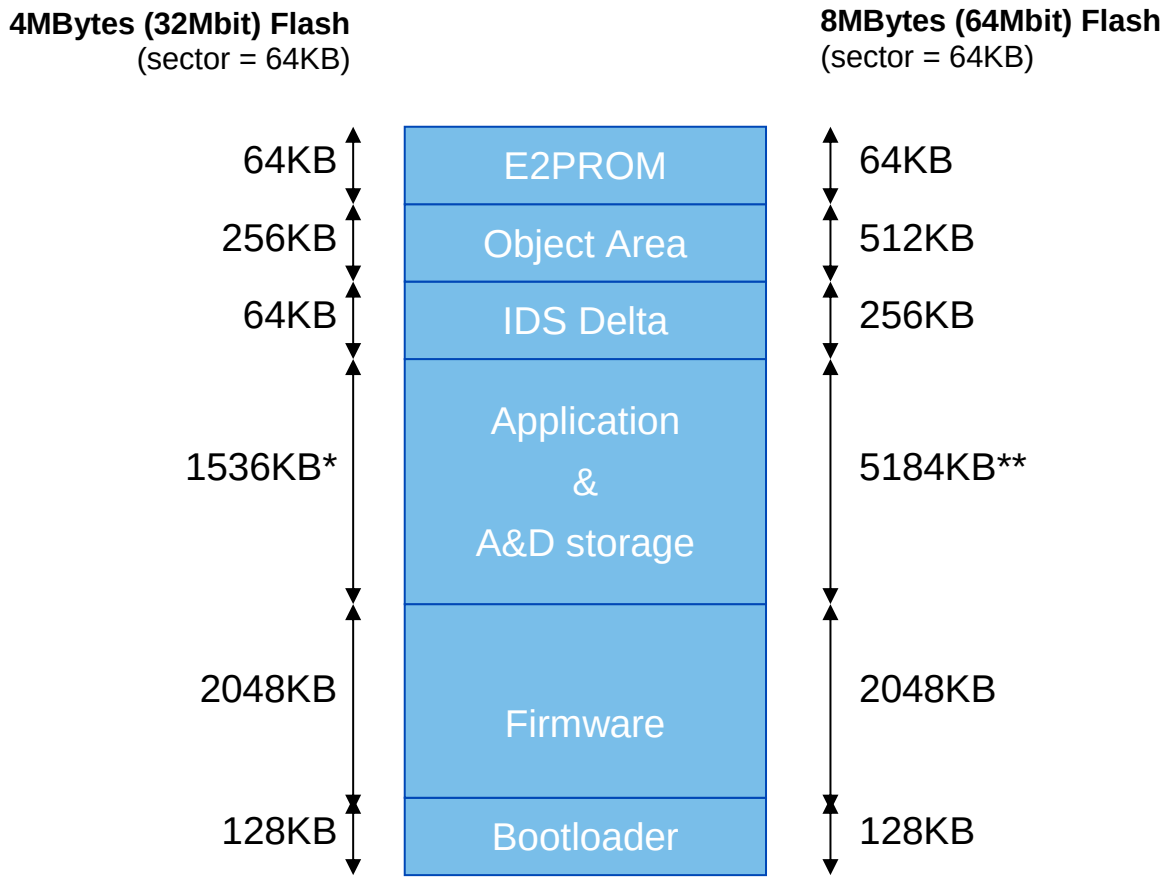


Figure 66. Open AT Framework 2.01 Flash Mapping Diagram

3.27.1.5. Case of ST 32/16 (M36W0R5040T5ZAQ)

- 32 Mbits FLASH: Mandatory configuration of CS0 space :
  - Bursted mode (Synchronous read / asynchronous write) Burst frequency: 26 MHz
  - Burst size: 4 half words
  - 3 clock cycles for read access cycle (read latency)
  - 5 clock cycles for write access cycle
  - 0 clock cycles for setup and hold
  - 1 clock cycle for turnaround
  - 16-bit wide data bus
  - “Top boot” type of flash architecture
  - Intel SW command set
- 16 Mbits PSRAM: Mandatory configuration of CS1 space :
  - Asynchronous mode
  - Intel mode (WE and OE)
  - Same configuration for Read and Write access
  - 1 clock cycle for setup
  - 2 clock cycles for access cycle
  - 0 clock cycles for hold
  - 1 clock cycle for turnaround

Refer to sections 3.27.1.7 and 3.27.1.8 respectively for the timing definition of the asynchronous read and write access.

3.27.1.6. Access Bus Waveform

3.27.1.6.1. Synchronous Timing Diagram

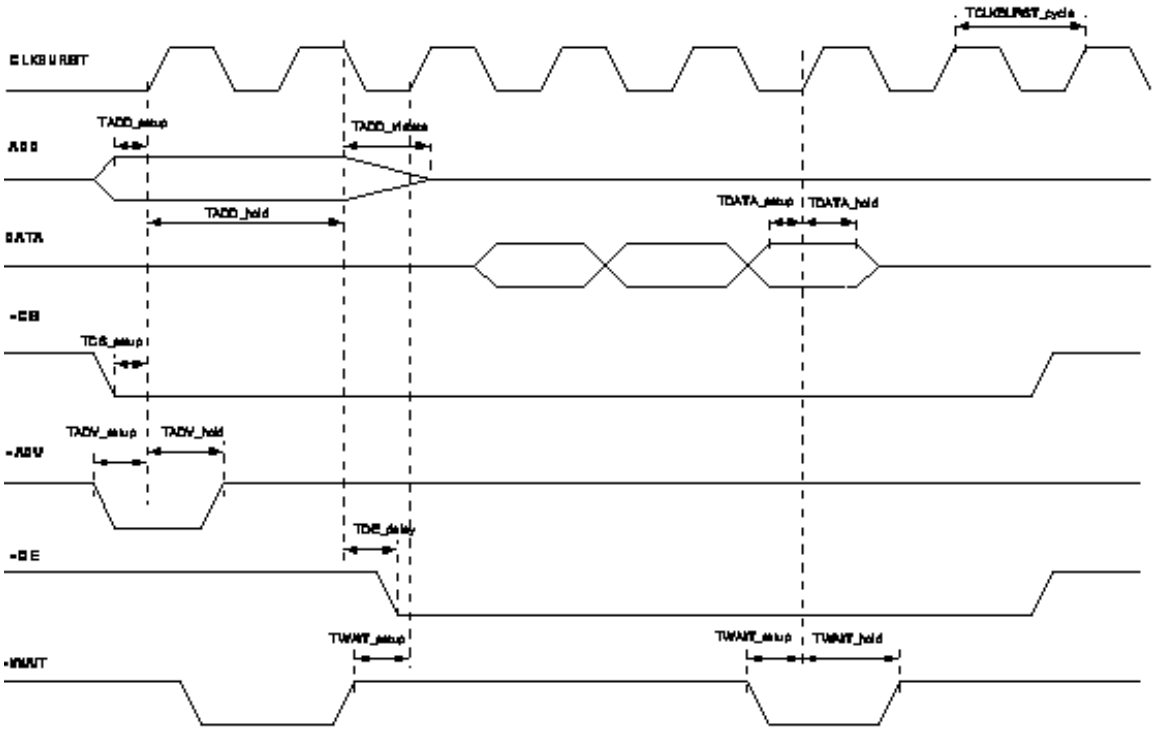


Figure 67. Read Synchronous Timing

Table 73. AC Characteristics of Read Synchronous Accesses

Signal	Description	Minimum	Typical	Maximum	Unit
$T_{CLKBURST}$	CLKBURST clock period time	19		78	ns
T_{ADD_setup}	Address bus setup time	7			ns
T_{ADD_hold}	Address bus hold time	19			ns
$T_{ADD\_tristate}$	Address bus tristate time			10	ns
T_{DATA_setup}	Data bus setup time	5			ns
T_{DATA_hold}	Data bus hold time	3			ns
T_{CS_setup}	Chip select setup time	7			ns
T_{ADV_setup}	ADV setup time	7			ns
T_{ADV_hold}	ADV hold time	7			ns
T_{OE_delay}	Output Enable delay time			13	ns
T_{WAIT_setup}	Wait setup time	5			ns
T_{WAIT_hold}	Wait hold time	5			ns

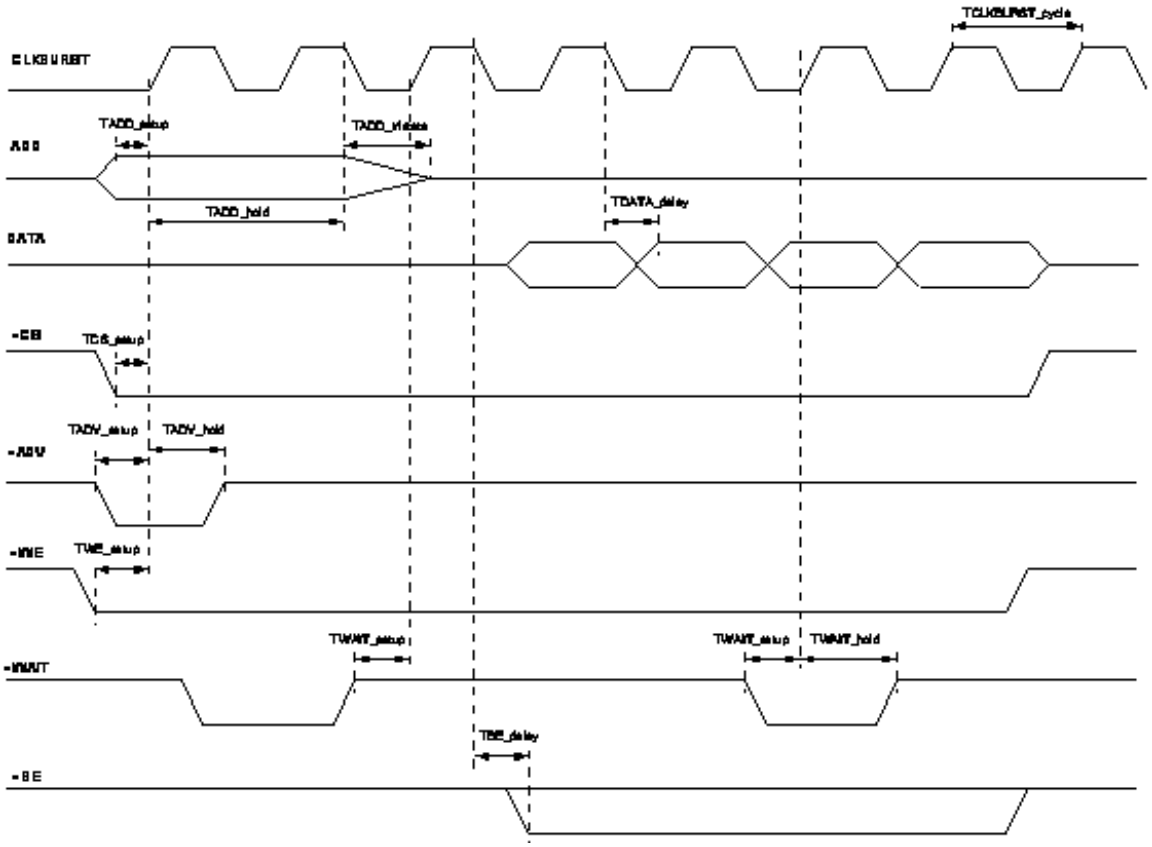


Figure 68. Write Synchronous Timing

Table 74. AC Characteristics of Write Synchronous Accesses

Signal	Description	Minimum	Typical	Maximum	Unit
T_{DATA_delay}	CLKBURTS falling edge to DATA valid delay			4	ns
T_{WE_setup}	WE to CLKBURST setup time	7			ns
T_{BE_delay}	CLKBURST falling edge to BE delay			4	ns

3.27.1.6.2. Asynchronous Timing Diagram

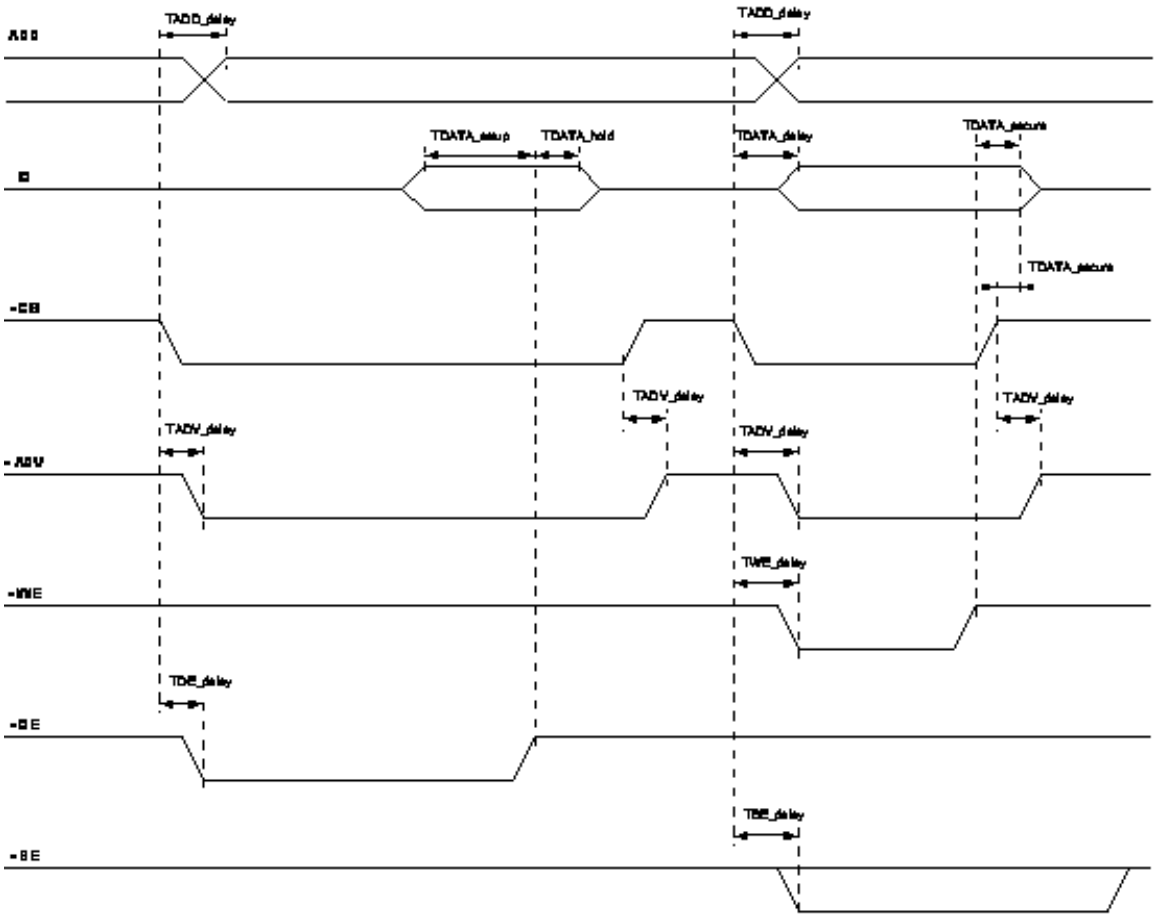


Figure 69. Read/Write Asynchronous Timing

Table 75. AC Characteristics of Asynchronous Accesses

Signal	Description	Minimum	Typical	Maximum	Unit
T_{ADD_delay}	Address delay time from Chip Select active			3	ns
T_{DATA_setup}	Data to Output Enable setup time	18			ns
T_{DATA_hold}	Data hold time after Output Enable inactive	3			ns
T_{DATA_delay}	Data delay time from Chip Select active			5	ns
T_{DATA_secure}	Data hold time after Write Enable inactive or Chip Select inactive	-5			ns
T_{ADV_delay}	ADV delay time from Chip Select active and inactive			3	ns
T_{WE_delay}	Write Enable delay time from Chip Select active			3	ns
T_{OE_delay}	Output Enable delay time from Chip Select active			5	ns
T_{BE_delay}	BE delay time from Chip Select active			3	ns

3.27.1.7. Access Bus Timing (Read Access)

The figure shows the definition of the read access timing.

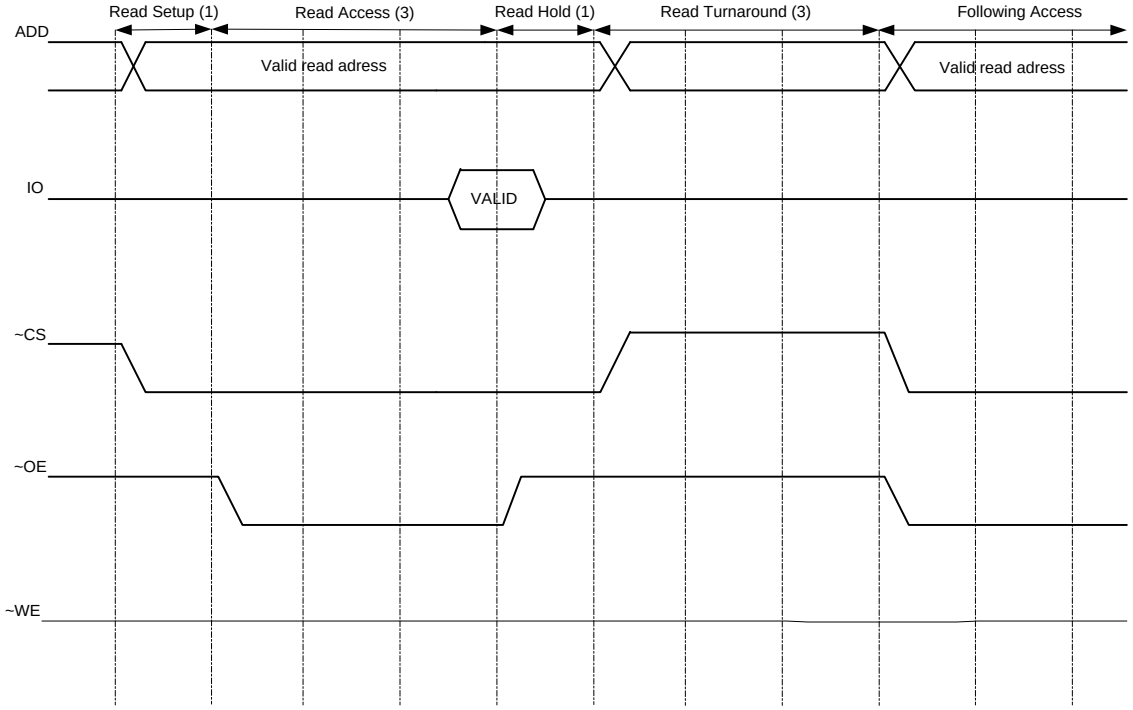


Figure 70. Read Access Timing

3.27.1.8. Access Bus Timing (Write Access)

The figure shows the definition of the write access timing.

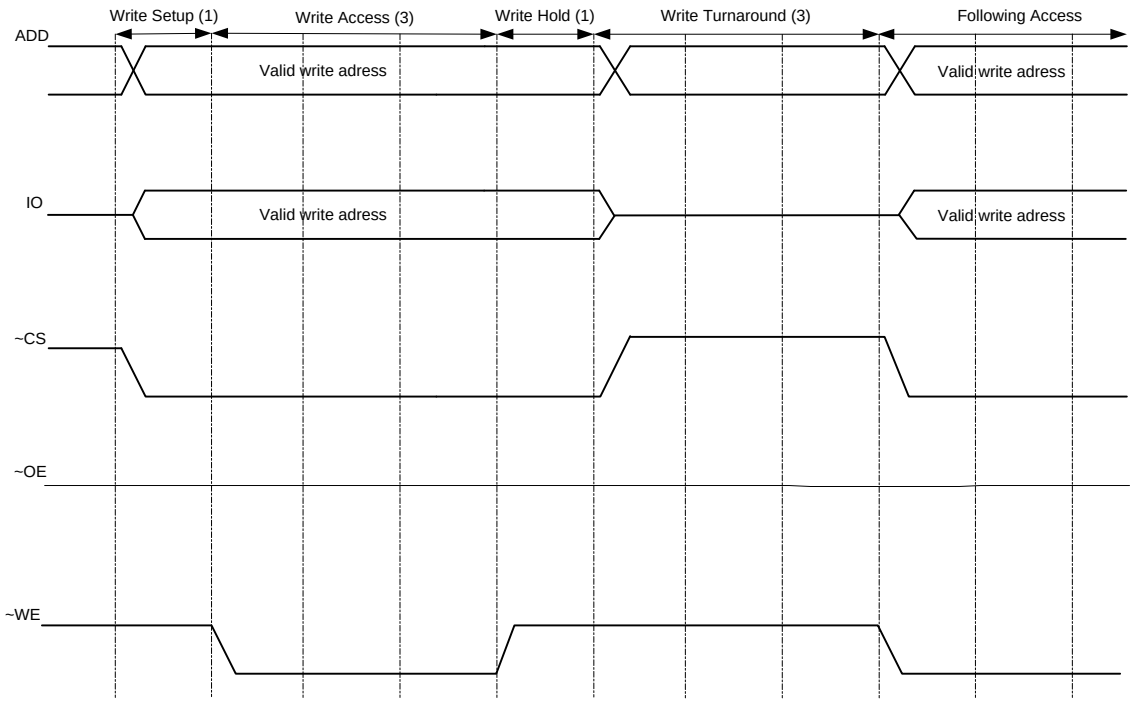


Figure 71. Write Access Timing

3.27.1.9. Flash Space

The Flash space (program memory) is dedicated on the CS0 pin chip select. This memory embeds the Open AT Framework 2.0, so this device has to run at a special configuration of the memory bus to ensure the full functionality of the module.

Refer to section 3.27.1.4, Open AT Framework 2.01 Flash Mapping for the details on the configuration.

3.27.1.10. RAM Space

The RAM space is dedicated on the CS1 pin chip select. This memory has to run at a special configuration of the memory bus to ensure the full functionality of the module.

Refer to section 3.27.1.4, Open AT Framework 2.01 Flash Mapping for the details on the configuration.

3.27.1.11. 16-bit Wide Data Bus User Space

The users' memory space is available on chip select CS2 and CS3.

User space range size is up to 64Mbytes.

Note: The AirPrime WMP50 does not have this capability. This section applies only to the WMP100 and WMP150 modules.

Refer to section 3.27.8, User Memory Space for further details.

3.27.2. Electrical Characteristics of the Signals

The memory interface voltage is provided by the VCC_1V8 power supply. So it is mandatory to supply the memories devices by VCC_1V8 power supply voltage provided by the module.

Table 76. Electrical Characteristics

Parameter		Min.	Typ.	Max.	Unit
VCC_1V8 (Module supply output)		1.76	1.9	1.94	V
Memory specification example (M36W0R5040T5ZAQ)	FLASH	1.7	-	1.95	V
	RAM	1.7	-	1.95	V
Load capacitance on the memory bus (with the memory connected)		-	-	10	pF

3.27.3. Pin Description

Table 77. Pin Description of Control Signal

Signal	Pin Number	I/O	I/O Type	Reset State	Description	Multiplexed with
~WAIT	R19	I	1V8	Pull up	Flash burst wait for synchronous operation	Not mux

Signal	Pin Number	I/O	I/O Type	Reset State	Description	Multiplexed with
~CS0	P19	O	1V8	1	Flash chip select	Not mux
~CS1	R20	O	1V8	1	RAM chip select	Not mux
~CS2 (*)	R18	O	1V8	Z	User chip select	GPIO1 / A25
~CS3	T17	O	1V8	1	User chip select	Not mux
CLKBURST	M19	O	1V8	Z	Burst Clock	Not mux
~ADV	U19	O	1V8	1	Burst address valid	Not mux
~WE-E	P20	O	1V8	1	write enable (Intel mode) / enable signal (Motorola mode)	Not mux
~OE-R/W	N20	O	1V8	1	output enable (Intel mode) / read not write (Motorola mode)	Not mux
~BE1	P18	O	1V8	1	select for 16 or 32 bits devices	Not mux

(*): Add a pull-up for the Reset State

Table 78. Pin Description of Data and Address Signal

Signal	Pin Number	I/O	I/O Type	Reset State	Description	Multiplexed with
D0	W24	I/O	1V8	Pull down	Data	Not mux
D1	W23	I/O	1V8	Pull down	Data	Not mux
D2	AA24	I/O	1V8	Pull down	Data	Not mux
D3	Y23	I/O	1V8	Pull down	Data	Not mux
D4	U21	I/O	1V8	Pull down	Data	Not mux
D5	Y22	I/O	1V8	Pull down	Data	Not mux
D6	Y24	I/O	1V8	Pull down	Data	Not mux
D7	V21	I/O	1V8	Pull down	Data	Not mux
D8	V20	I/O	1V8	Pull down	Data	Not mux
D9	U20	I/O	1V8	Pull down	Data	Not mux
D10	V24	I/O	1V8	Pull down	Data	Not mux
D11	V22	I/O	1V8	Pull down	Data	Not mux
D12	V23	I/O	1V8	Pull down	Data	Not mux
D13	AA23	I/O	1V8	Pull down	Data	Not mux
D14	U23	I/O	1V8	Pull down	Data	Not mux
D15	T23	I/O	1V8	Pull down	Data	Not mux
A0	T19	O	1V8	1	Address	Not mux
A1	U18	O	1V8	1	Address	Not mux
A2	U24	I/O	1V8	Pull down	Address	Not mux
A3	P24	I/O	1V8	Pull down	Address	Not mux
A4	N24	I/O	1V8	Pull down	Address	Not mux
A5	M21	I/O	1V8	Pull down	Address	Not mux
A6	M24	I/O	1V8	Pull down	Address	Not mux
A7	N23	I/O	1V8	Pull down	Address	Not mux
A8	R24	I/O	1V8	Pull down	Address	Not mux

Signal	Pin Number	I/O	I/O Type	Reset State	Description	Multiplexed with
A9	R22	I/O	1V8	Pull down	Address	Not mux
A10	P22	I/O	1V8	Pull down	Address	Not mux
A11	T22	I/O	1V8	Pull down	Address	Not mux
A12	R23	I/O	1V8	Pull down	Address	Not mux
A13	M22	I/O	1V8	Pull down	Address	Not mux
A14	P21	I/O	1V8	Pull down	Address	Not mux
A15	R21	I/O	1V8	Pull down	Address	Not mux
A16	P23	I/O	1V8	Pull down	Address	Not mux
A17	T21	I/O	1V8	Pull down	Address	Not mux
A18	T24	O	1V8	0	Address	Not mux
A19	M23	O	1V8	0	Address	Not mux
A20	N21	O	1V8	0	Address	Not mux
A21	N22	O	1V8	0	Address	Not mux
A22	M20	O	1V8	0	Address	Not mux
A23	N19	O	1V8	0	Address	Not mux
A24	U22	O	1V8	Z	Address	GPIO2
A25	R18	O	1V8	Z	Address	GPIO1 / ~CS2
A26	V16	O	1V8	Z	Address	GPIO3 / INT0*

* The multiplexed interrupt pin is only applicable to the WMP100 and WMP150 embedded module variant. Refer to section 3.19, External Interrupt for more information about interrupt pins and their multiplexes.

3.27.4. Application with a Combo Memory

An application is given with one 64/16Mb combo memory ST (M36W0R6040T1ZAQ) which embedded a PSRAM and FLASH memories.

The schematic is compatible with the 32/16Mb combo memory ST (M36W0R5040T5ZAQF).

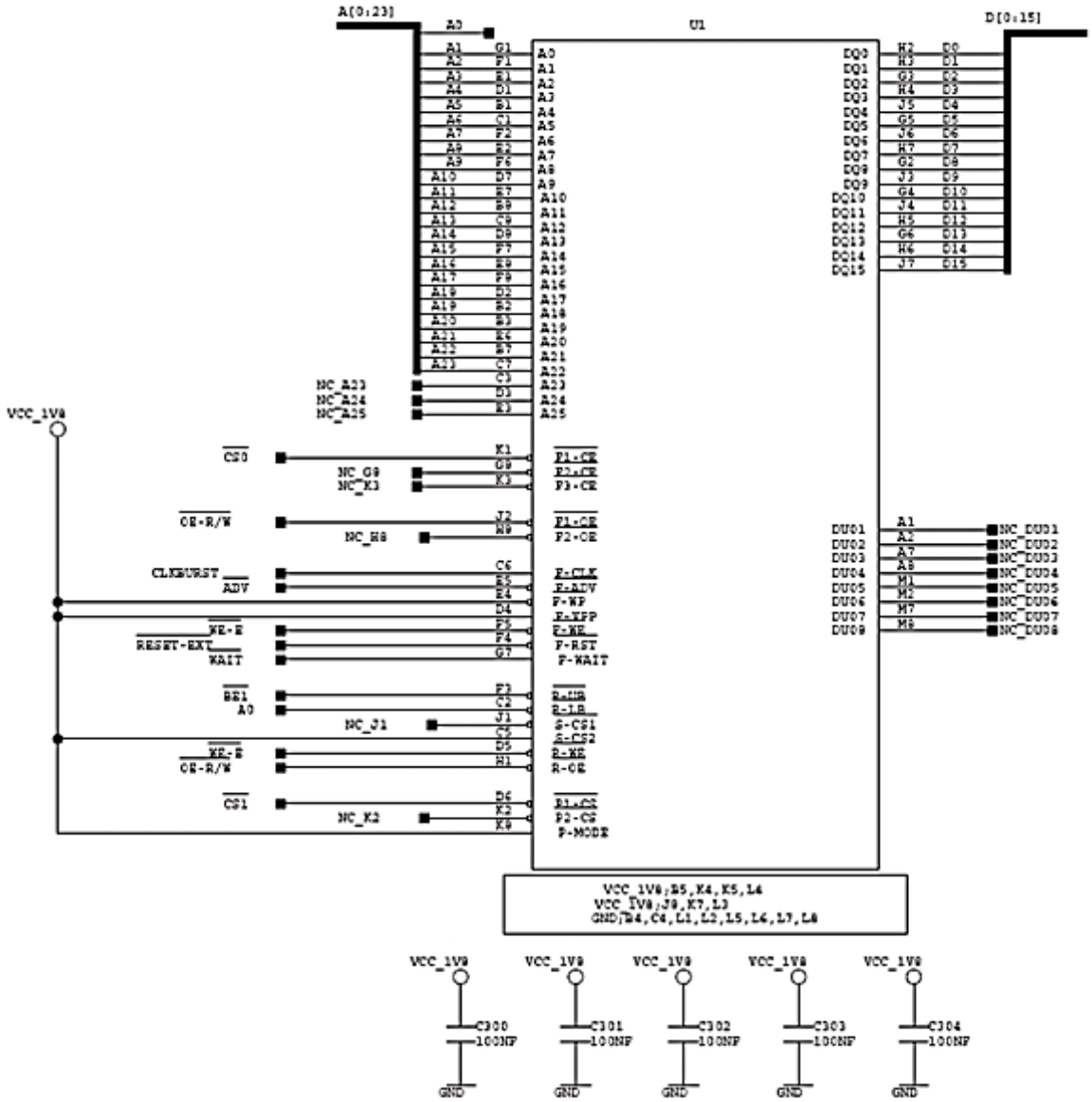


Figure 72. Schematic of Combo Memory Connection

NC: not connected

Recommended Components

- U1 : Can be the combo memory **M36W0R5040T5ZAQF** from STMicroelectronics :
  - 32Mbits of Bursted Flash (synchronous), Top type.
  - 16Mbits of PSRAM (asynchronous).
  - Temperature range from –30°C to +85°C.
  - 16Bit bus Data wide type
  - 1.8 Volt core and I/O type
- U1 : Can be the combo memory **M36W0R6040T1ZAQF** from STMicroelectronics :
  - 64Mbits of Bursted Flash (synchronous), Top type.
  - 16Mbits of PSRAM (asynchronous).
  - Temperature range from –30°C to +85°C.
  - 16Bit bus Data wide type
  - 1.8 Volt core and I/O type
- Decoupling capacitors: 100nF

Note: It is not necessary to connect the A22 signal (ball M20) if you use the 32/16Mbits combo memory (M36W0R5040T5ZAQF).

It is necessary to connect the ~CS1 signal to the D6 ball of the both combos (for the references M36W0R5040T5ZAQF and M36W0R6040T1ZAQF)

3.27.5. Constraints with a Combo Memory

The following constraints are identical for WMP modules.

3.27.5.1. Electrical Constraints

- The Flash type must be a “Top” type, see on the part number: i.e:M36W0R5040T5ZAQF
- The reset of the Flash must be done by the **~EXT-RESET** (ball AB14) signal, (see section 3.18, Reset Signals).
- Decoupling capacitors have to be used and to be placed close to the memory power supply pins. (Refer to Figure 73 Combo Memory Location below)
- The power supply **VCC_1V8** (ball AD5) is provided by the module.
- Because it is a 16Bit bus data wide implementation, the Address signal A0 has to be used to select the Low value of the data bus (8 bits LSB). So ~BE1 and A0 have to be connected to ~R-UB and ~R-LB of the memory (See schematic).
- The Flash must be connected on ~CS0 and the RAM on the ~CS1.

3.27.5.2. PCB Constraints

The memory must be placed close to the module (refer to Figure 73 Combo Memory Location below).

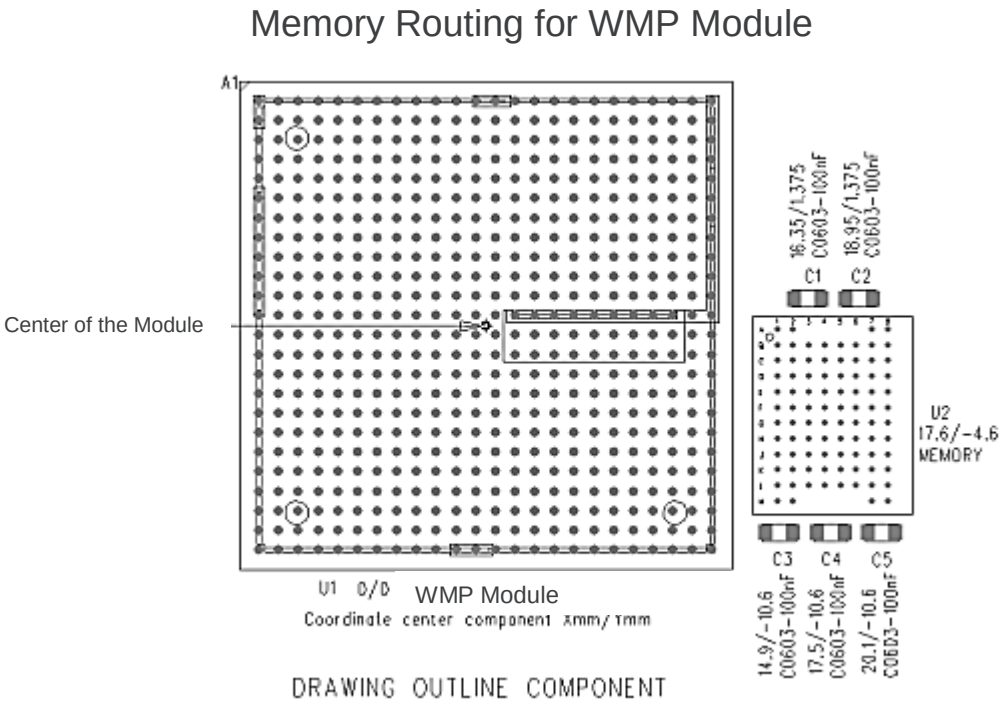


Figure 73. Combo Memory Location

The radio receiver performances are very sensitive to all kinds of interferences generated by active components on the customer board.

For product designs utilizing a WMP module, the external memory activity could interfere with the GSM antenna when a PCB antenna or an external antenna (when the box housing is not metallic) is situated close to the module and its memory.

This interference does not occur when the antenna is ≥20cm away from the memory or when the product enclosure is shielded (ex: metallic housing or spayed conductive paint).

Memory bus of the module should be shielded using either of the following options:

Option 1) External shielding cover for memory when memory tracks on the outer PCB layers

A 4 layers PCB could be designed with a memory bus on 3 of the layers and the bottom layer acting as the ground. The tracks on top layer may require being shielded (depending on the product design) with a metallic casing on this layer as shown below.

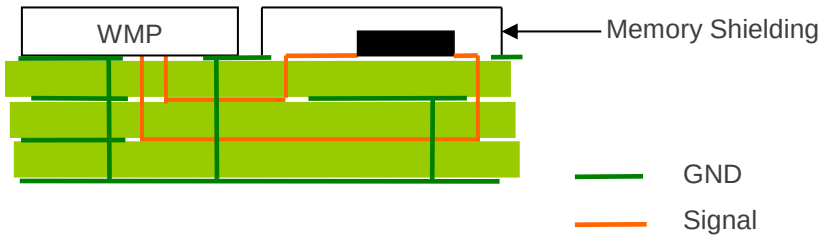


Figure 74. Memory Shielding: External Memory Shield

Option 2) Memory tracks integrated into the inner PCB layers (no external mechanical shielding cover).

In this option, the top and bottom layers are grounded / filled with ground plan. In this case, a minimum 6 layer PCB is required.

The footprint of an optional shielding cover can also be implemented to secure the best radio performances. Sierra Wireless can propose footprint/CAO for such shielding cover.

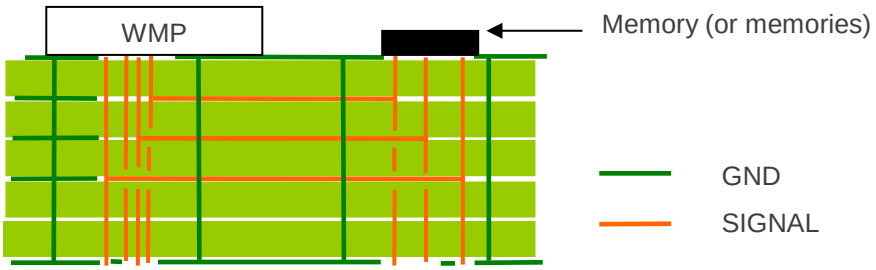


Figure 75. Memory Shielding: Memory Tracks Integration

- The memories must be placed close to the module (refer to the discrete memories location figure below)
- All the memory bus nets must have a maximum length of 50 mm ±10%.
- It is recommended to shield around all the signals (refer to the Memory PCB figure below).
- All signals must be routed with adjoining layers (refer to the Memory PCB figure below). It is not recommended adding other signals between the module and the memory.
- PCB structure example: refer to the Memory PCB figure below.
  - Inner layer trace 100 µm, clearance 100 µm
  - Layer top and bottom trace 150 µm, clearance 150 µm
  - Vias: pads 0.5 mm, drill 0.25 mm

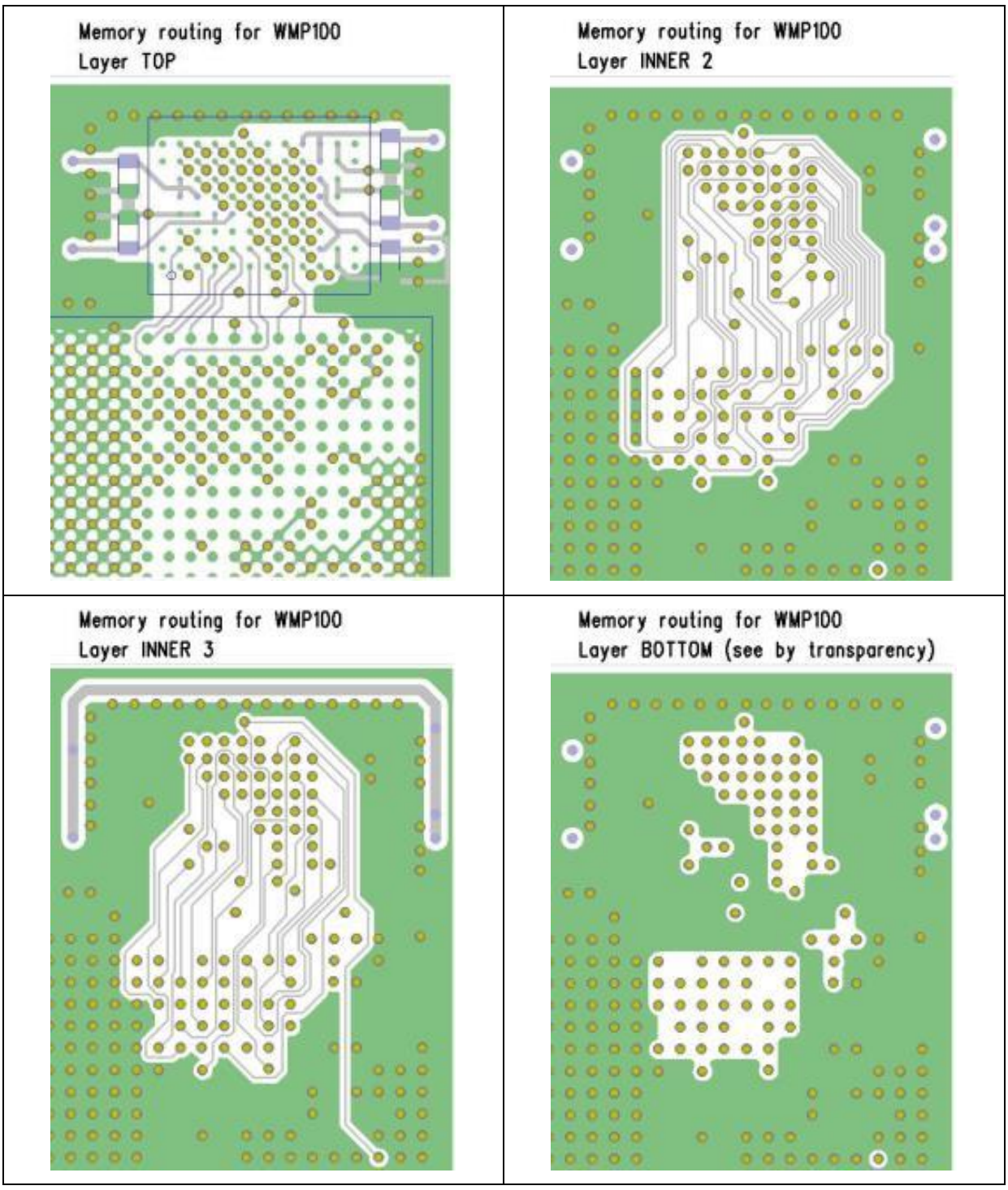


Figure 76. Combo Memory PCB for WMP100 Module Application

3.27.6. Application with Discrete Memories

An application is given with discrete memories ST FLASH (M58WR064HT70ZB6F) & MICRON PSRAM (MT45W1MW16BDGB-701 IT).

FLASH and PSRAM memories are in stand-alone package it is the 64Mb + 16Mb configuration.

The schematic is compatible with the 32Mb + 128Mb discrete memories configuration.

Refer to section 3.27.1.2, Memory Configuration for the several configurations.

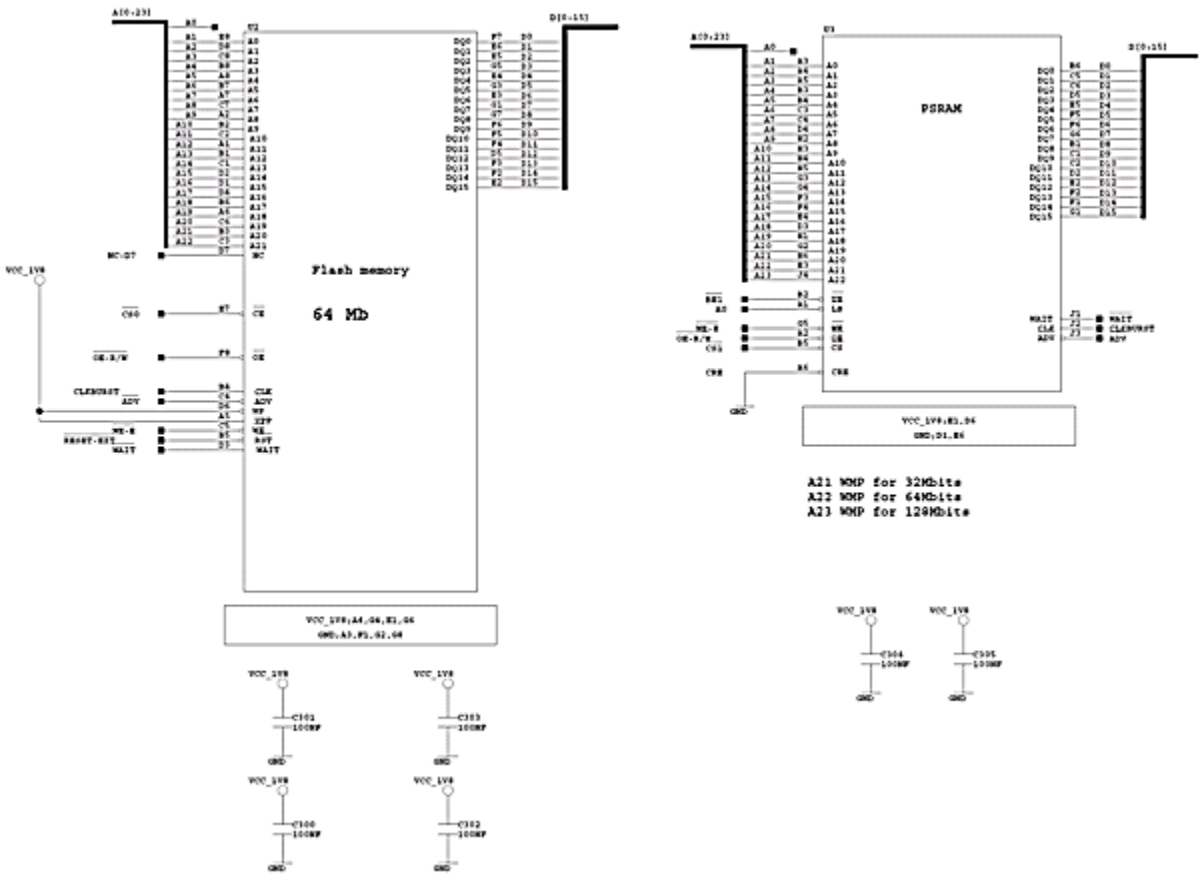


Figure 77. Schematic of Discrete Memories Connection

NC: not connected

Recommended Components

- U2 : Can be the discrete memory M58WR064HT70ZB6F from STMicroelectronics :
  - 64Mbits of Bursted Flash (synchronous), Top type.
  - Temperature range from –40°C to +85°C.
  - 16Bit bus Data wide type
  - 1.8 Volt core and I/O type
- U3 : Can be the discrete memory MT45W1MW16BDGB-701 IT from MICRON:
  - 16Mbits of PSRAM (asynchronous SW configuration).
  - Temperature range from –40°C to +85°C.
  - 16Bit bus Data wide type
  - 1.8 Volt core and I/O type
- Decoupling capacitors: 100nF

Note: Refer to section 3.27.1.2, Memory Configuration for the several memories configurations.

3.27.7. Constraints with Discrete Memories

3.27.7.1. Electrical Constraints

- The Flash type must be a "**Top**" type, see on the part number: i.e.: M58WR064H**T**70ZB6F
- The reset of the Flash must be done by the **~EXT-RESET** (ball AB14) signal (refer to section 3.18, Reset Signals).
- Decoupling capacitors have to be used and to be placed close to the memory power supply pins. (see the Memory location figure below)
- The power supply **VCC_1V8** (ball AD5) is provided by the module.
- Because it is a 16 Bit bus data wide implementation, the Address signal A0 has to be used to select the Low value of the data bus (8 bits LSB). So ~BE1 and A0 have to be connected to ~R-UB and ~R-LB of the memory (refer to schematic).
- The Flash must be connected on ~CS0 and the RAM on the ~CS1.

3.27.7.2. PCB Constraints

The radio receiver performances are very sensitive to all kinds of interferences generated by active components on the customer board.

For product designs utilizing a WMP module, the external memory activity could interfere with the GSM antenna when a PCB antenna or an external antenna (when the box housing is not metallic) is situated close to the module and its memory.

This interference does not occur when the antenna is ≥20cm away from the memory or when the product enclosure is shielded (ex: metallic housing or spayed conductive paint).

Memory bus of the module should be shielded using either of the following options:

Option 1) External shielding cover for memory when memory tracks on the outer PCB layers

A 4 layers PCB could be designed with a memory bus on 3 of the layers and the bottom layer acting as the ground. The tracks on top layer may require being shielded (depending on the product design) with a metallic casing on this layer as shown below.

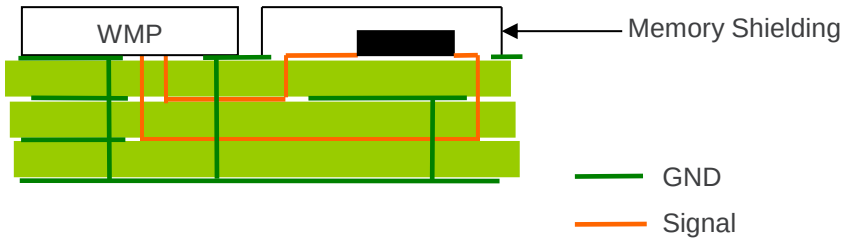


Figure 78. Memory Shielding: External Memory Shield

Option 2) Memory tracks integrated into the inner PCB layers (no external mechanical shielding cover).

In this option, the top and bottom layers are grounded / filled with ground plan. In this case, a minimum 6 layer PCB is required.

The footprint of an optional shielding cover can also be implemented to secure the best radio performances. Sierra Wireless can propose footprint/CAO for such shielding cover.

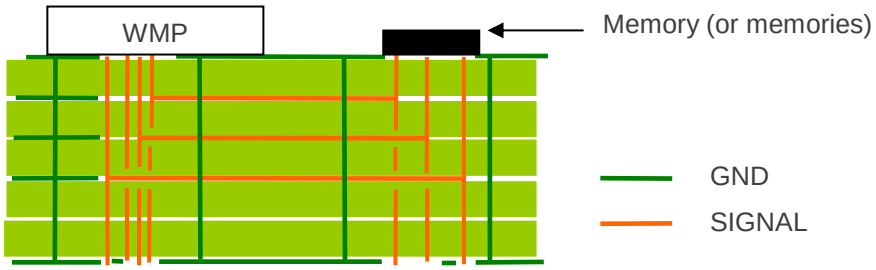


Figure 79. Memory Shielding: Memory Tracks Integration

- The memories must be placed close to the module (refer to the discrete memories location figure below)
- All the memory bus nets must have a maximum length of 50 mm ±10%.
- It is recommended to shield around all the signals (refer to the Memory PCB figure below).
- All signals must be routed with adjoining layers (refer to the Memory PCB figure below). We do not recommend adding other signals between the module and the memory.
- PCB structure example: see the Memory PCB figure below.
  - Inner layer trace 100 µm, clearance 100 µm
  - Layer top and bottom trace 150 µm, clearance 150 µm
  - Vias: pads 0.5 mm, drill 0.25 mm

3.27.8. User Memory Space

The user memory space is available on chip select CS2 and CS3.

User space range size is up to 64Mbytes.

Note: The AirPrime WMP50 does not have this capability. This section applies only to the WMP100 and WMP150 modules.

Few signals are multiplexed. It's possible to have these configurations.

- ~CS3, A24, GPIO1
- ~CS3, A24, A25
- ~CS3, ~CS2, A24

For further details please refer to document [3] Open AT Framework AT Commands Interface Guide for Firmware 7.0 or later.

3.28. RF Interface

The impedance is 50 Ohms nominal and the DC resistance is 0 Ohm.

3.28.1. RF Connection

The RF antenna connection uses a unique BGA Ball associated with grounded BGA balls all around.

This ball must be connected, using a PCB via, to an embedded RF 50 ohms line, in order to avoid any interference coming from base-band signals.

For the same reasons, the RF connection and the RF embedded line must be kept 1 cm away from any noisy base-band signal. Without following this rule the RX sensitivity might be degraded.

The other side of the embedded 50 ohms RF line can be connected to a RF connector or a soldering pad in order to connect an antenna.

It's also possible to use a CMS antenna or to design an antenna directly on the same PCB.

Note: *The WMP module does not support an antenna switch for a car kit but this function can be implemented externally and it can be driven using a GPIO.*

The antenna cable and connector should be chosen in order to minimize losses in the frequency bands used for GSM 850/900MHz and 1800/1900MHz.

0.5dB can be considered as a maximum value for loss between the module and an external connector.

3.28.2. RF Performances

RF performances are compliant with the ETSI recommendation GSM 05.05.

The main parameters for Receiver are:

- GSM850 Reference Sensitivity = -108 dBm Static & TUHigh
- E-GSM900 Reference Sensitivity = -108 dBm Static & TUHigh
- GSM850 Reference Sensitivity = -109 dBm typ. (ambient & nominal voltage) Static & TUHigh
- E-GSM900 Reference Sensitivity = -109 dBm typ. (ambient & nominal voltage) Static & TUHigh

- DCS1800 Reference Sensitivity = -107 dBm Static & TUHigh
- PCS1900 Reference Sensitivity = -107 dBm Static & TUHigh
- DCS1800 Reference Sensitivity = -108 dBm typ. (ambient & nominal voltage) Static & TUHigh
- PCS1900 Reference Sensitivity = -108 dBm typ. (ambient & nominal voltage) Static & TUHigh

- Selectivity @ 200 kHz : > +9 dBc
- Selectivity @ 400 kHz : > +41 dBc
- Linear dynamic range: 63 dB
- Co-channel rejection: >= 9 dBc

The main parameters for Transmitter are:

- Maximum output power (EGSM & GSM850): 33 dBm +/- 2 dB at ambient temperature (-1/+2 dB at nominal voltage)
- Maximum output power (GSM1800 & PCS1900): 30 dBm +/- 2 dB at ambient temperature (-1/+2 dB at nominal voltage)
- Minimum output power (EGSM & GSM850): 5 dBm +/- 5 dB at ambient temperature
- Minimum output power (GSM1800 & PCS1900): 0 dBm +/- 5 dB at ambient temperature

3.28.3. Antenna Specifications

The antenna must fulfill the requirements that are specified in the table below. The optimum operating frequency depends on the application. A dual band or a quad band antenna shall work in these frequency bands and have the following characteristics:

Table 79. Antenna Specifications

Characteristic		WMP Module			
		E-GSM 900	DCS 1800	GSM 850	PCS 1900
TX Frequency		880 to 915 MHz	1710 to 1785 MHz	824 to 849 MHz	1850 to 1910 MHz
RX Frequency		925 to 960 MHz	1805 to 1880 MHz	869 to 894 MHz	1930 to 1990 MHz
Impedance		50 Ohms			
VSWR	Rx max	1.5 :1			
	Tx max	1.5 :1			
Typical radiated gain		0dBi in one direction at least			

3.28.4. Antenna

The RF antenna connection uses a unique BGA Ball associated with grounded BGA balls all around.

This BGA ball must be connected, using a PCB via, to an embedded RF 50 ohms line, in order to protect the antenna line from the noise coming from base-band signals.

The figure below shows the RF ball and the ground balls around, and a PCB via placement example.

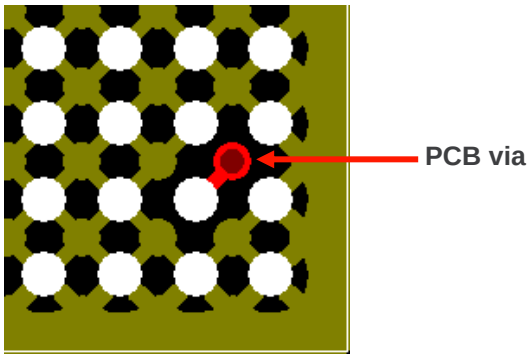


Figure 80. Antenna and Ground Ball Placement

The figure below shows the RF embedded line and the PCB via.

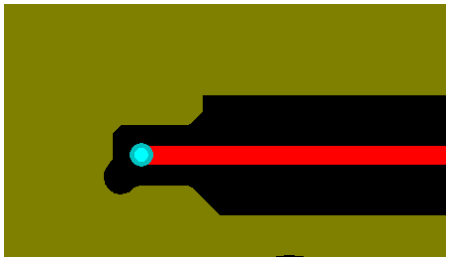


Figure 81. RF 50Ω Embedded Line

This 50 ohms line is surrounded by **two ground planes** in order to protect this antenna line from noise. The length of the line shouldn't be too high (more than a few cm) because of RF insertion losses. The **width of the line must be calculated** in order to ensure 50 Ohms characteristic impedance.

For the same reasons, not only the RF connection but also the RF embedded line should be kept about 1 cm away from any (noisy) Base-band signal in order to ensure a good RX sensitivity level.

The figure below shows a keep away area for the antenna connection point. This restricted area must not contain any noisy base-band signals (like any bus or clock signal).

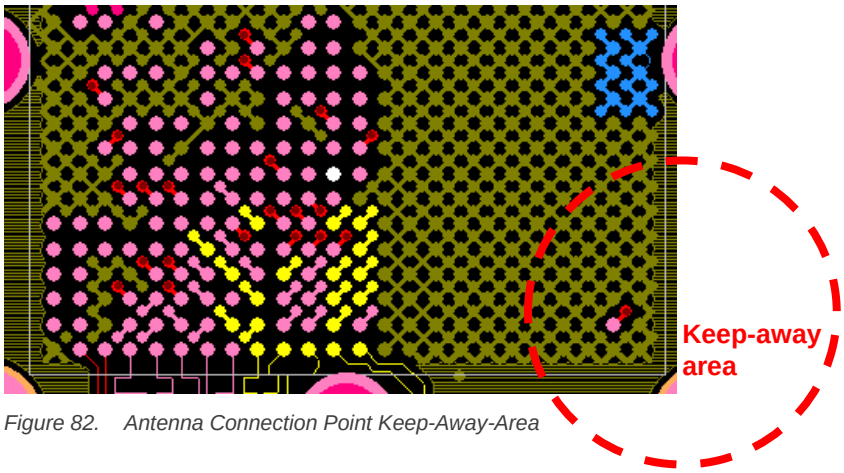


Figure 82. Antenna Connection Point Keep-Away-Area

The other end of the embedded 50 ohms RF line can be connected to an RF connector or a soldering pad in order to connect an antenna.

It's recommended to add an ESD protection component on the antenna line, in order to increase the final product's ESD tolerance.

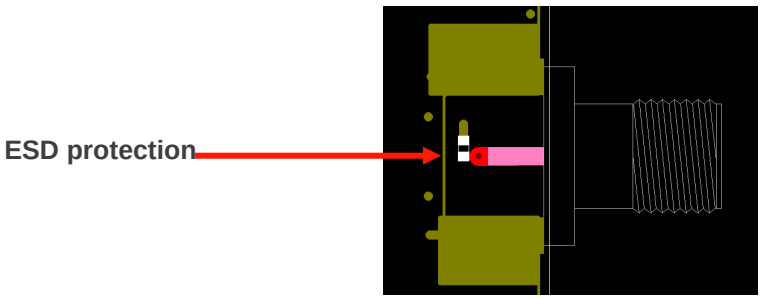


Figure 83. Example of RF Connector and ESD Protection

This ESD protection component can be an 82 nH Multi-Layer HF inductor (0603 case). It must be connected between RF output and ground as short as possible.

It's also possible to use an antenna chip or to choose to design an antenna directly on the same PCB.

Warning: *Sierra Wireless strongly recommends working with an antenna manufacturer either to develop an antenna adapted to the application or to adapt an existing solution to the application.*

Both the mechanical and electrical antenna adaptation is one of the key issues in the design of the GSM terminal.

Note: This product is classified as a "mobile device" and the antenna must be installed to provide a minimum distance of 20 cm from all persons.

The antenna system gain implemented with this OEM module must not exceed 6.9 dBi for the GSM 850 MHz band and 3.1 dBi for the GSM 1900 MHz band. This device is approved as a module to be integrated within other devices.

4. Consumption Measurement Procedure

This section describes the consumption measurement procedure used to obtain the WMP module consumption specification

WMP modules/Open AT Framework 2.0 consumption specification values are measured for all working modes available on this product. Refer to the appendix of document [3] Open AT Framework AT Commands Interface Guide for Firmware 7.0 or later. Consumption results are highly dependent on the hardware configuration used during measurement, this section describes the hardware configuration settings to be used to obtain optimum consumption measurements.

4.1. Hardware Configuration

The hardware configuration includes both the measurement equipment and the module with its motherboard.

4.1.1. Equipment

Four devices are used to perform consumption measurement.

- A communication tester
- A current measuring power supply
- A standalone power supply
- A computer, to control the module and save measurement data.

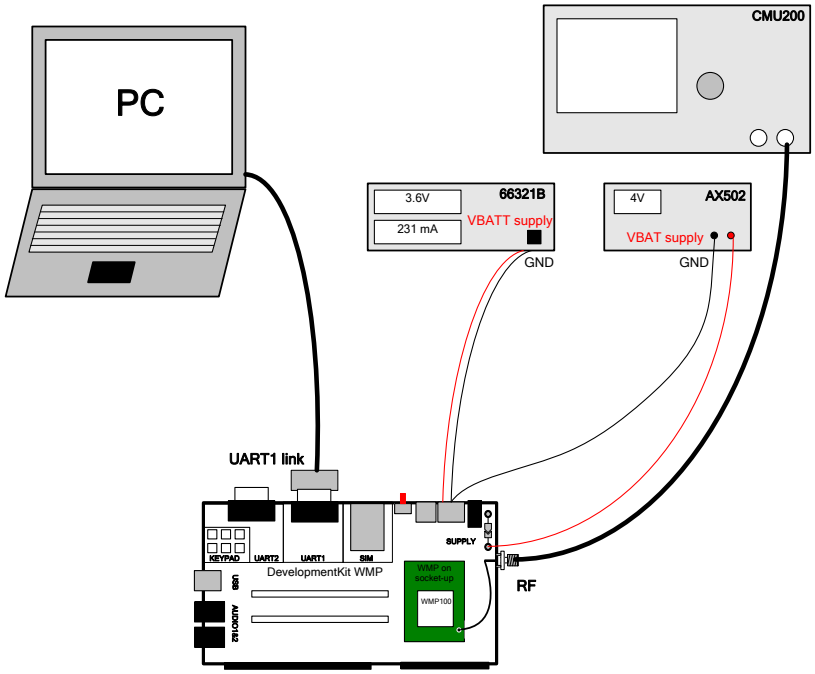


Figure 84. Typical Hardware Configuration

The communication tester is a **CMU 200** from **Rhode & Schwartz**. This tester offers all GSM/GPRS network configurations required and allows a wide range of network configurations to be set.

The **AX502** standalone power supply is used to supply all motherboard components except the module. The goal is to separate motherboard consumption from module consumption -which is measured by the other power supply, the **66321B** “current measuring power supply”.

The “current measuring power supply” is also connected and controlled by the computer (GPIB control not shown in the previous figure).

A SIM must be inserted in the Development Kit board during all consumption measurements.

Table 80. Equipment Reference List

Device	Manufacturer	Reference	
Communication Tester	Rhode & Schwartz	CMU 200	Quad Band GSM/DCS/GPRS
Current measuring power supply	Agilent	66321B	Used for VBATT (for WMP alone)
Stand alone power supply	Metrix	AX502	Used for VBAT (for boards peripherals)

4.1.2. Module Motherboard

The module board used is the Development Kit Wireless Microprocessor V2. This board can be used to perform consumption measurement with several settings. For a description of the settings, refer to document [2] AirPrime WMP Series Development Kit User Guide.

The module is only powered by VBATT. The Development Kit board is powered by the standalone power supply at VBAT. It is for this reason that the link between VBATT and VBAT (J605) must be opened (by removing the solder at the top of board in the SUPPLY area).

- VBATT powered by the current measuring power supply (**66321B**).
- VBAT powered by the standalone power supply (**AX502**).

The R600, resistor, and D603, D604 diodes (around the BAT-TEMP connector) must be removed.

The UART2 link is not used, therefore J201, J202, J203, J204 must be opened (by removing the solder).

The “LED0” must be not used, so J602 must be opened (by removing the solder).

The USB link is not used, therefore J301, J302, J303, J304, J305 must be opened (by removing the solder).

Around “CONFIG” area, the switch BOOT must be to OFF position.

The goal of the settings is to eliminate all bias current from VBATT and to supply the entire board (except the module) via VBAT only.

The standalone power supply may be set to 4 Volts.

4.1.3. SIM Cards Used

Consumption measurement may be performed with 3-Volt or 1.8-Volt SIM cards. However, all specified consumption values are for a 3-Volt SIM card.

Caution: *The SIM card is supplied by the module, consumption measurement results may vary depending of the SIM card used.*

4.2. Software Configurations

Software configuration for the equipment and the module settings are explained in the subsections below.

4.2.1. Module Configuration

Software configuration is simply performed by selecting the working mode to be used to perform the measurement.

More details of the working modes and the procedure used to change working mode are given in the appendix of document [3] Open AT Framework AT Commands Interface Guide for Firmware 7.0 or later.

4.2.2. Working Mode Description

The module can work in different modes. Each one is characterized by:

- Power consumption
- Firmware power processing
- Feature availability

4.2.2.1. ACTIVE Mode with GSM Stack in Idle

This is the default mode for the module.

There is no feature restriction in this mode.

4.2.2.2. SLEEP Mode with GSM Stack in Idle

This mode is a low power consumption mode. In this mode, the module has restricted access to peripheral interfaces; thereby UARTs, USB, SPIs, I^2C, GPIOs, ADCs and Buzzer are not available.

To enable or disable this mode, you can use the AT+W32K command.

The mode activation and deactivation is initiated when the customer device is connected to the serial interface (DTE). DTR signal (ball M16) must be pulled UP for requesting activation of the slow idle mode. To deactivate this mode DTR signal (ball M16) must be pulled DOWN.

When this mode is activated, the module requires 1 to 15 seconds to power down consumption. In this state, a 32 kHz internal clock is used during the inactivity stage.

Then, the module can automatically wake up on unsolicited events such as:

- GSM paging
- external interruption
- key press
- alarm
- timer expiration

During the wake up period, the module will have the same characteristic as fast idle mode in terms of power consumption and firmware power processing.

The module automatically switches back to idle state after all treatments.

4.2.2.3. ACTIVE Mode

In this mode, SIM device and GSM/GPRS/EDGE-Rx features like GSM voice or data call, SMS, GPRS/EDGE-Rx data transfer are not available. The embedded application is running and the serial port remains active (AT commands are available). If any data has to be transmitted over the network, this mode has to be turned off.

To switch the module to this mode use "AT+WBHV=1,1" command. The module must be restarted in order to take the new behavior into account.

To disable this mode, use the "AT+WBHV=1,0" command and restart the module.

4.2.2.4. SLEEP Mode

This mode is a low power consumption mode. It combines ACTIVE mode and SLEEP idle mode in terms of feature availability.

In this mode, SIM device and GSM/GPRS/EDGE-Rx features like GSM voice or data call, SMS, GPRS/EDGE-Rx data transfer are not available. In addition, the module has restricted access to peripheral interfaces; thereby UARTs, USB, SPIs, I^2C, GPIOs, ADCs and Buzzer are not available.

In this mode, the module can automatically wake up on unsolicited events such as:

- external interruption
- key press
- alarm
- timer expiration

During the wake up period, the module has the same characteristics as ACTIVE mode in terms of power consumption and firmware power processing.

The module automatically switches back to idle state after all treatments.

To switch the module to this mode, use "AT+WBHV=1,2" command. The module must be restarted in order to take the new behavior into account.

To disable this mode, use "AT+WBHV=1,0" command and restart.

Note: The USB port must be deactivated to enter SLEEP mode.

4.2.2.5. GSM Connected Mode

The module is in this mode during circuit switch voice or data call.

4.2.2.6. GPRS Transfer Mode

The module is in this mode during packet data transmission.

4.2.2.7. Alarm Mode

This mode is a low power consumption mode. The only feature which is available in this mode is the alarm wake up.

To use it, an alarm wake up has to be previously recorded by AT+CALA command before switching to this mode.

To activate the module in this mode, use the "AT+CPOF" command, when the ON/OFF switch is LOW. Deactivate this mode by placing the ON/OFF switch to HIGH or after alarm wake up.

4.2.3. Working Mode Features

The table below sums up feature availability in each mode.

Table 81. Feature Availability In Each Mode

Features	Alarm Mode	ACTIVE Mode with GSM Stack in Idle	SLEEP Mode with GSM Stack in Idle	ACTIVE Mode	SLEEP Mode	Connected Mode	Transfer Mode
Alarm	√	√	√	√	√	√	√
Wake-up Open AT Framework application on timer events	-	√	√	√	√	√	√
GSM/GPRS/EDGE-Rx paging (alert from the network for incoming call, incoming SMS or incoming GPRS/EDGE-Rx data)	-	√	√	-	-	√	√
SIM	-	√	-	-	-	√	√
UARTs	-	√	-	√	-	√	√
USB	-	√	-	√	-	√	√
SPIs	-	√	-	√	-	√	√
I2C	-	√	-	√	-	√	√
GPIO	-	√	-	√	-	√	√
ADCs	-	√	-	√	-	√	√
Buzzer	-	√	-	√	-	√	√
Keypad	-	√	√	√	√	√	√
External IT	-	√	√	√	√	√	√
LED0	-	√	√	√	√	√	√

4.2.4. Equipment Configuration

The communication tester is set according to the working mode of the module.

Paging during idle modes, Tx burst power, RF band and GSM/DCS/GPRS/EDGE-Rx may be selected on the communication tester.

Network analyzer configuration according to working mode:

Table 82. Operating Mode Configuration

Operating Mode	Network Analyzer Configuration
ALARM Mode	N/A
SLEEP Mode	N/A
ACTIVE Mode	N/A
SLEEP mode with telecom stack in Idle Mode	Paging 9/Rx burst occurrence ~2s
	Paging 2/Rx burst occurrence ~0,5s
ACTIVE mode with telecom stack in Idle Mode	Paging 9/Rx burst occurrence ~2s
	Paging 2/Rx burst occurrence ~0,5s
Peak current in GSM/GPRS Mode	850/900 MHz - PCL5/gam.3 (TX power 33dBm)
	1800/1900 MHz - PCL0/gam.3 (TX power 30dBm)
GSM Connected Mode (Voice)	850/900 MHz - PCL5 (TX power 33dBm)
	850/900 MHz - PCL19 (TX power 5dBm)
	1800/1900 MHz - PCL0 (TX power 30dBm)
	1800/1900 MHz - PCL15 (TX power 0dBm)
GPRS Transfer Mode class 10 (3Rx/2Tx)	850/900 MHz - gam.3 (TX power 33dBm)
	1800/1900 MHz - gam.3 (TX power 30dBm)

The standalone power supply may be set from 3.2V to 4.5V.

The power supply (VBATT) used for measurement may be set from 3.2V to 4.8V according to the module VBATT specifications.

4.3. Power Consumption

Power consumption depends on the configuration used. It is for this reason that the following consumption values are given for each mode, RF band and type of software used (with or without an Open AT Framework application).

Note: All of the following information is given assuming a 50 Ω RF output.

The following consumption values were obtained by performing measurements on module samples at a temperature of 25° C.

Three VBATT values are used to measure the consumption, $VBATT_{MIN}$ (3.2V), $VBATT_{MAX}$ (4.8V) and $VBATT_{TYP}$ (3.6V).

The average current is given for the three VBATT values and the peak current given is the maximum current peak measured with the three VBATT voltages.

For a more detailed description of the working modes, (refer to document [3] Open AT Framework AT Commands Interface Guide for Firmware 7.0 or later).

4.3.1. Power Consumption without Open AT Framework

The following measurement results are relevant when:

- there is no Open AT Framework application
- the Open AT Framework application is disabled
- no processing is required by an Open AT Framework application

*Note: Power consumption performance is software related. The values listed below using an external SIM were based on Firmware **7.45**, while the values listed using an Embedded SIM were based on Firmware **7.44**.*

$_{TX}$ means that the current peak is the RF transmission burst (Tx burst).

$_{RX}$ means that the current peak is the RF reception burst (Rx burst).

Table 83. Power Consumption without Open AT Framework (Typical Values)

Operating Mode	Parameter	Module Type	$I_{Average}$			I_{Peak}	Unit
			VBATT				
			3.2V	3.6V	4.8V		
ALARM Mode	-	External SIM	17.30	18.00	22.00	N/A	µA
		Embedded SIM	20.9	22.8	34.0	N/A	
SLEEP Mode[3]	-	External SIM	0.29	0.31	0.29	3.26	mA
		Embedded SIM	0.427	0.426	0.425	1.67	
ACTIVE Mode	-	External SIM	24.44	22.28	19.44	49.26	mA
		Embedded SIM	49.7	45.5	36.2	57.7	
SLEEP mode with GSM stack in Idle Mode[1]	Paging 9/Rx burst occurrence ~2s	External SIM	2.21	2.24	2.22	164.64	mA
		Embedded SIM	1.96	1.85	1.60	165	
	Paging 2/Rx burst occurrence ~0,5s	External SIM	6.36	5.92	5.44	166.34	mA
		Embedded SIM	5.99	5.62	4.84	166	
ACTIVE mode with GSM stack in Idle Mode[2]	Paging 9/Rx burst occurrence ~2s	External SIM	24.59	22.50	19.55	162.94	mA
		Embedded SIM	23.4	22.2	18.6	162	
	Paging 2/Rx burst occurrence ~0,5s	External SIM	26.27	23.54	20.58	164.00	mA
		Embedded SIM	25.2	23.9	20.0	163	
Peak current in GSM/GPRS Mode	850/900 MHz - PCL5 / gam.3 (TX power 33dBm) 1800/1900 MHz - PCL0 / gam.3 (TX power 30dBm)	External SIM	1587	1548	1491	1587	mA
		Embedded SIM	1593	1564	1492	1593	
GSM Connected Mode (Voice)	850/900 MHz - PCL5 (TX power 33dBm)	External SIM	251.7	243.8	232.7	1559.9	mA
		Embedded SIM	246	241	225	1593	
	850/900 MHz - PCL19 (TX power 5dBm)	External SIM	101.0	96.2	87.8	265.1	mA
		Embedded SIM	103	99	88	271	
	1800/1900 MHz - PCL0 (TX power 30dBm)	External SIM	174.2	168.1	158.8	890.2	mA
		Embedded SIM	179	174	163	972	
	1800/1900 MHz - PCL15 (TX power 0dBm)	External SIM	97.0	92.2	83.6	228.1	mA
		Embedded SIM	99	94	84	244	
GPRS Transfer Mode class 10 (3Rx/2Tx)	850/900 MHz - gam.3 (TX power 33dBm)	External SIM	427.2	416.7	402.9	1565.2	mA
		Embedded SIM	414	407	385	1580	
	1800/1900 MHz - gam.3 (TX power 30dBm)	External SIM	275.0	267.9	257.5	893.6	mA
		Embedded SIM	283	277	265	945	

(1): SLEEP Idle Mode consumption is dependent on the SIM card used. Some SIM cards respond faster than others; the longer the response time, the higher the consumption.

(2): ACTIVE Idle Mode the signal ~CT108-2/DTR1 (ball M16) is at high level.

(3): To enter SLEEP mode must deactivate the USB port first.

4.3.2. Power Consumption with Open AT Framework

The following consumption results were measured during the run of Dhrystone application. There are two tables for the CPU clock programmed at 26MHz and 104MHz respectively.

*Note: Power consumption performance is software related. The values listed in the tables below were based on Firmware **7.44**.*

$_{TX}$ means that the current peak is the RF transmission burst (Tx burst).

$_{RX}$ means that the current peak is the RF reception burst (Rx burst).

Table 84. Power Consumption with the Application of CPU @ 26MHz (Typical Values)

Operating Mode	Parameter	Module Type	$I_{Average}$			I_{Peak}	Unit
			VBATT				
			3.2V	3.6V	4.8V		
ALARM Mode	-	External SIM	N/A*	N/A*	N/A*	N/A*	µA
		Embedded SIM	N/A*	N/A*	N/A*	N/A*	
SLEEP Mode	-	External SIM	N/A*	N/A*	N/A*	N/A*	mA
		Embedded SIM	N/A*	N/A*	N/A*	N/A*	
ACTIVE Mode	-	External SIM	48.2	43.6	34.3	61.7	mA
		Embedded SIM	47.2	43.5	34.6	58.4	
SLEEP mode with GSM stack in Idle Mode1	Paging 9/Rx burst occurrence ~2s	External SIM	N/A*	N/A*	N/A*	N/A*	mA
		Embedded SIM	N/A*	N/A*	N/A*	N/A*	
	Paging 2/Rx burst occurrence ~0,5s	External SIM	N/A*	N/A*	N/A*	N/A*	mA
		Embedded SIM	N/A*	N/A*	N/A*	N/A*	
ACTIVE mode with GSM stack in Idle Mode2	Paging 9/Rx burst occurrence ~2s	External SIM	46.9	42.2	33.3	169	mA
		Embedded SIM	45.9	42.2	33.6	162	
	Paging 2/Rx burst occurrence ~0,5s	External SIM	47.9	43.4	34.3	168	mA
		Embedded SIM	46.9	43.3	34.6	163	
Peak current in GSM/GPRS Mode	850/900 MHz - PCL5 / gam.3 (TX power 33dBm) 1800/1900 MHz - PCL0 / gam.3 (TX power 30dBm)	External SIM	1621	1561	1522	1621	mA
		Embedded SIM	1679	1626	1561	1679	
GSM Connected Mode (Voice)	850/900 MHz - PCL5 (TX power 33dBm)	External SIM	244	237	221	1621	mA
		Embedded SIM	244	238	223	1679	
	850/900 MHz - PCL19 (TX power 5dBm)	External SIM	102	96	86	273	mA
		Embedded SIM	101	97	86	272	
	1800/1900 MHz - PCL0 (TX power 30dBm)	External SIM	177	171	160	982	mA
		Embedded SIM	177	172	162	1018	
	1800/1900 MHz - PCL15 (TX power 0dBm)	External SIM	98	93	82	257	mA
		Embedded SIM	97	93	83	239	

Operating Mode	Parameter	Module Type	$I_{Average}$			I_{Peak}	Unit
			VBATT				
			3.2V	3.6V	4.8V		
GPRS Transfer Mode class 10 (3Rx/2Tx)	850/900 MHz - gam.3 (TX power 33dBm)	External SIM	409	401	382	1597	mA
		Embedded SIM	412	405	385	1651	
	1800/1900 MHz - gam.3 (TX power 30dBm)	External SIM	280	272	261	965	mA
		Embedded SIM	281	275	264	992	

(*): N/A doesn't mean that no Open AT Framework application is possible in this specific mode. That means that the specific Dhrystone application can't allow this specific mode. (This is a worst case for the consumption measurement).

Table 85. Power Consumption with the Application of CPU @ 104MHz (Typical Values)

Operating Mode	Parameter	Module Type	$I_{Average}$			I_{Peak}	Unit
			VBATT				
			3.2V	3.6V	4.8V		
ALARM Mode	-	External SIM	N/A*	N/A*	N/A*	N/A*	µA
		Embedded SIM	N/A*	N/A*	N/A*	N/A*	
SLEEP Mode	-	External SIM	N/A*	N/A*	N/A*	N/A*	mA
		Embedded SIM	N/A*	N/A*	N/A*	N/A*	
ACTIVE Mode	-	External SIM	89.7	78.9	60.3	110	mA
		Embedded SIM	86.5	77.7	60.7	102	
SLEEP mode with GSM stack in Idle Mode1	Paging 9/Rx burst occurrence ~2s	External SIM	N/A*	N/A*	N/A*	N/A*	mA
		Embedded SIM	N/A*	N/A*	N/A*	N/A*	
	Paging 2/Rx burst occurrence ~0,5s	External SIM	N/A*	N/A*	N/A*	N/A*	mA
		Embedded SIM	N/A*	N/A*	N/A*	N/A*	
ACTIVE mode with GSM stack in Idle Mode2	Paging 9/Rx burst occurrence ~2s	External SIM	88.0	77.4	59.1	212	mA
		Embedded SIM	84.9	76.3	59.6	205	
	Paging 2/Rx burst occurrence ~0,5s	External SIM	89.0	78.3	60.1	213	mA
		Embedded SIM	85.8	77.2	60.5	205	
Peak current in GSM/GPRS Mode	850/900 MHz - PCL5 / gam.3 (TX power 33dBm) 1800/1900 MHz - PCL0 / gam.3 (TX power 30dBm)	External SIM	1663	1622	1551	1663	mA
		Embedded SIM	1696	1658	1585	1696	
GSM Connected Mode (Voice)	850/900 MHz - PCL5 (TX power 33dBm)	External SIM	284	272	247	1663	mA
		Embedded SIM	283	272	248	1696	
	850/900 MHz - PCL19 (TX power 5dBm)	External SIM	142	132	111	321	mA
		Embedded SIM	139	131	111	319	
	1800/1900 MHz - PCL0 (TX power 30dBm)	External SIM	217	206	185	1021	mA
		Embedded SIM	215	205	186	1069	
	1800/1900 MHz - PCL15 (TX power 0dBm)	External SIM	138	128	107	290	mA
		Embedded SIM	135	126	108	288	

Operating Mode	Parameter	Module Type	$I_{Average}$			I_{Peak}	Unit
			VBATT				
			3.2V	3.6V	4.8V		
GPRS Transfer Mode class 10 (3Rx/2Tx)	850/900 MHz - gam.3 (TX power 33dBm)	External SIM	450	437	407	1642	mA
		Embedded SIM	451	438	410	1695	
	1800/1900 MHz - gam.3 (TX power 30dBm)	External SIM	319	308	286	1003	mA
		Embedded SIM	319	308	289	1028	

(*): N/A doesn't mean that no Open AT Framework application is possible in this specific mode. That means that the specific Dhrystone application can't allow this specific mode. (This is a worst case for the consumption measurement).

4.3.3. Consumption Waveform Samples

The consumption waveforms presented below are for an EGSM900 network configuration with the Open AT Framework running on the WMP module.

The typical VBATT voltage is 3.6V.

Four significant working mode consumption waveforms are described:

- Connected Mode (PCL5: Tx power 33dBm)
- SLEEP Idle Mode (Paging 9)
- ACTIVE Idle Mode (Paging 9)
- Transfer Mode (GPRS class 10, gam.3: Tx power 33dBm)

The following waveform shows only the form of the current.

4.3.3.1. Connected Mode Current Waveform

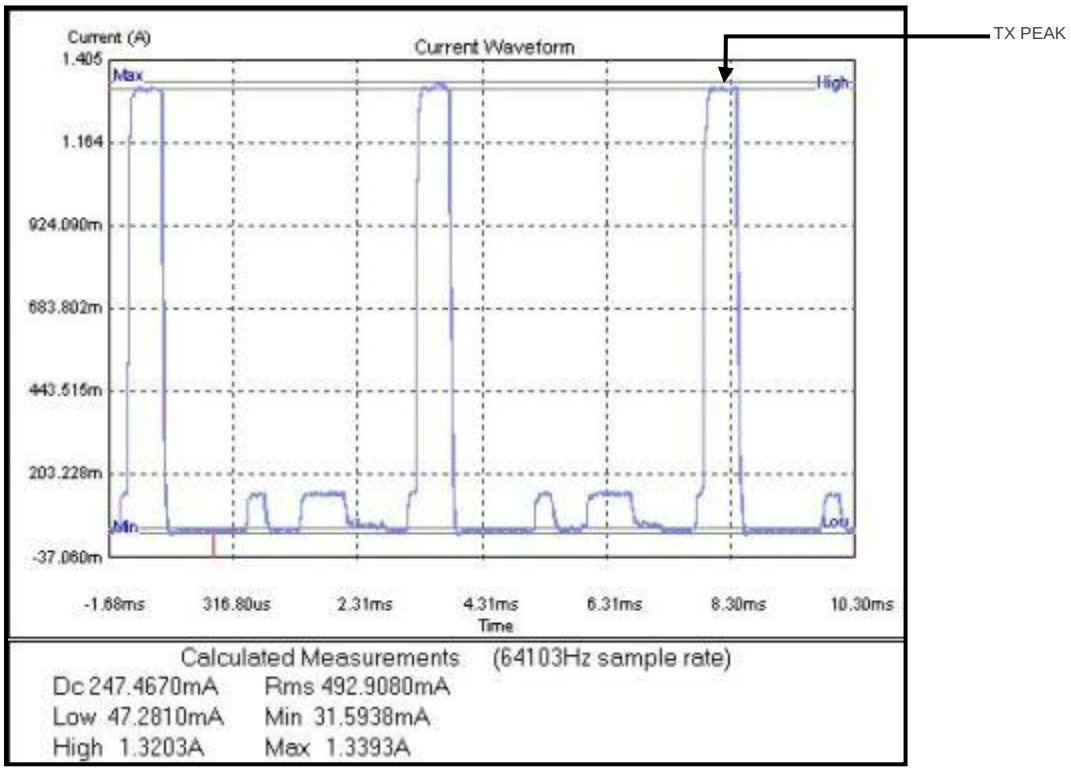


Figure 85. Current Waveform of Connected Mode

4.3.3.2. SLEEP Idle Mode Current Waveform

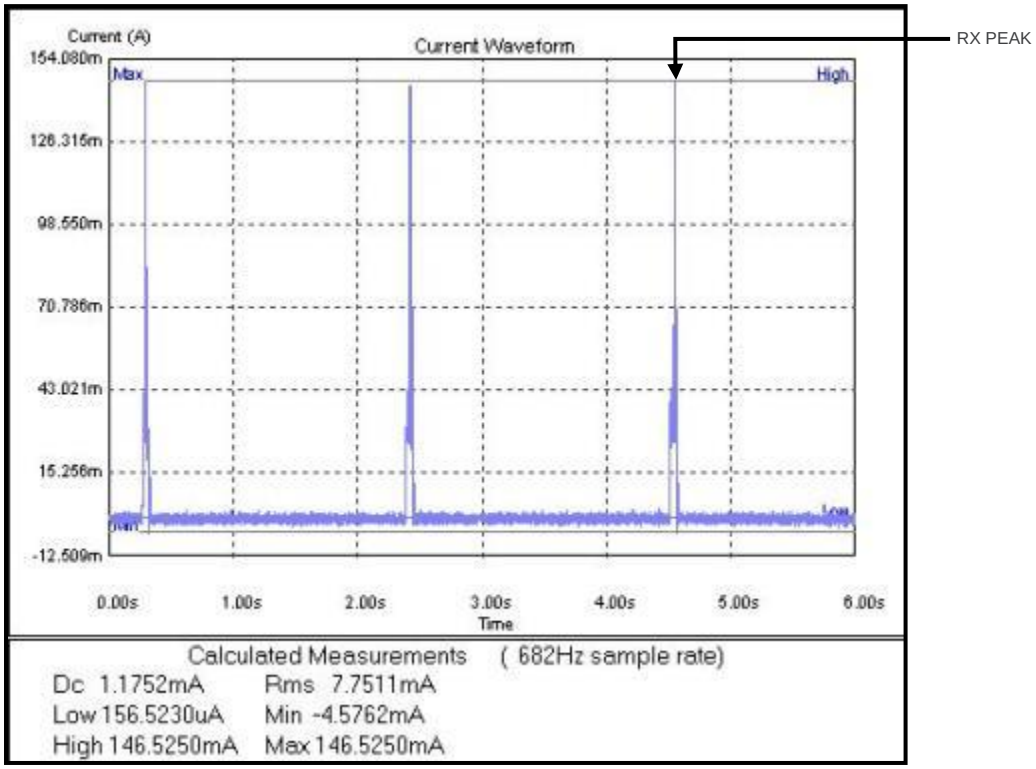


Figure 86. Current Waveform of SLEEP Idle Mode

4.3.3.3. ACTIVE Idle Mode Current Waveform

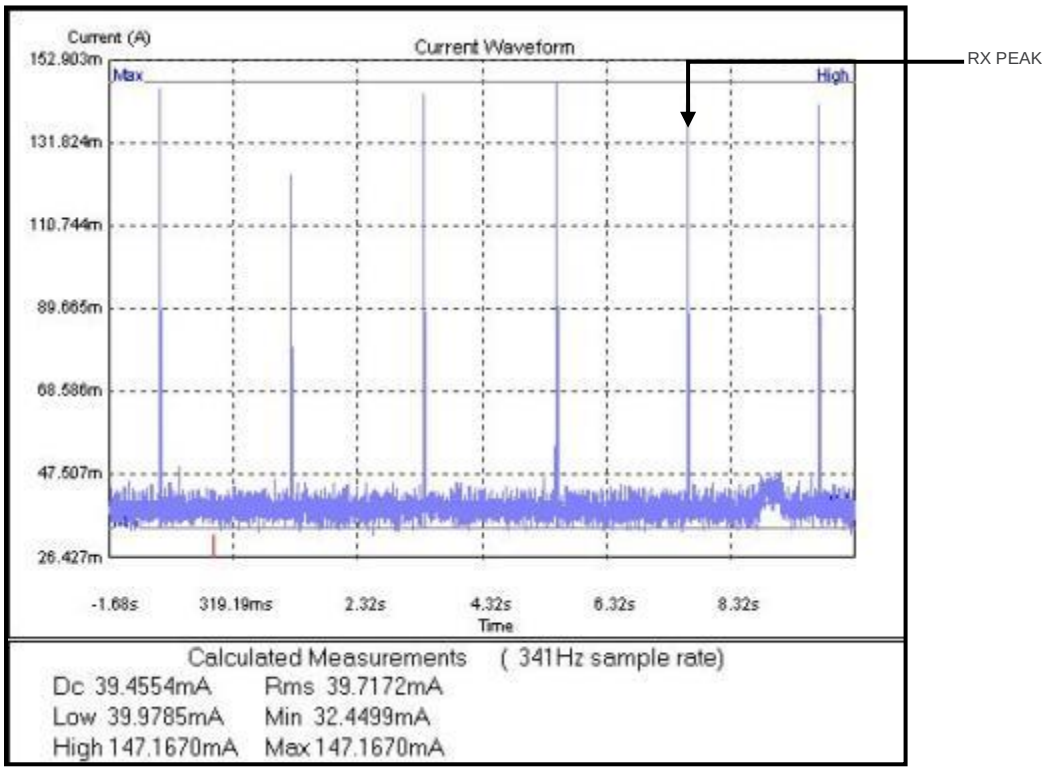


Figure 87. Current Waveform of ACTIVE Idle Mode

4.3.3.4. Transfer Mode Class 10 Current Waveform

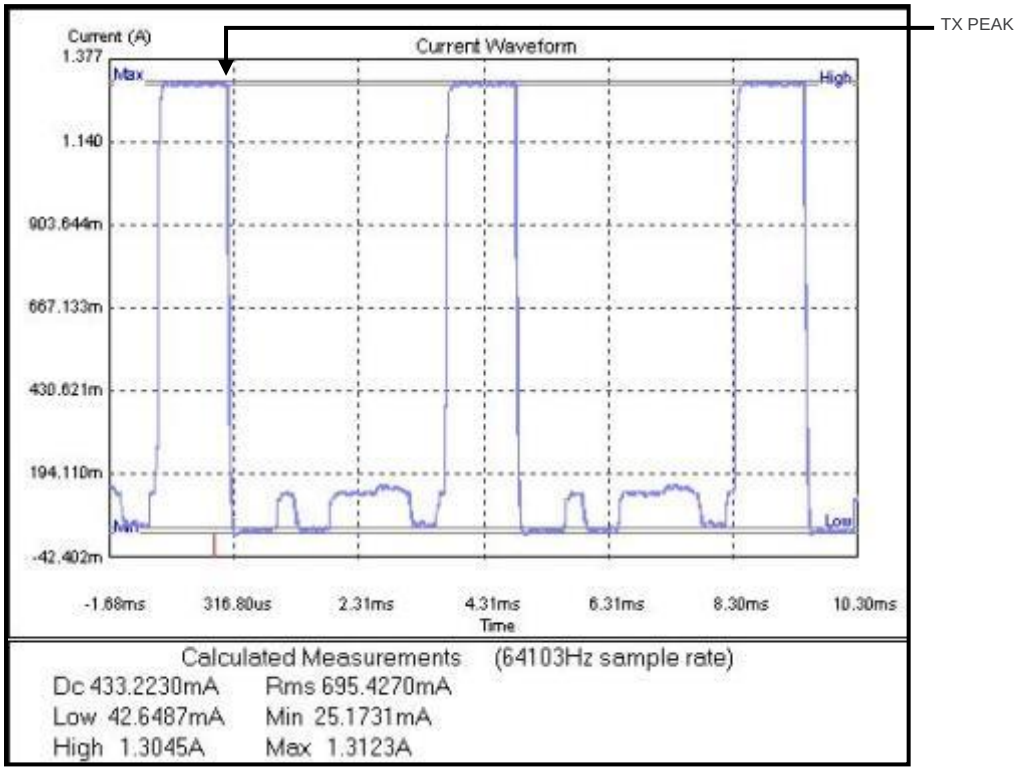


Figure 88. Current Waveform of Transfer Mode Class 10

4.3.4. Startup Current

Measures of the maximum peak current have been performed during one second.

Table 86. Typical Startup Current of the Module During First Second

Power supply	3.2 V[1]	3.3V[2]	3.6 V	4.8 V
$I_{peak\ for\ the\ first\ second}$	88 mA	88mA	76 mA	64 mA

(1): Only for WMP50, WMP100, and WMP150.

(2): Only for WMP100 Embedded SIM and WMP150 Embedded SIM.

4.3.5. Recommendations for Less Current Consumption

For better consumption, in particular for the quiescent current, it is recommended to drive the GPIOs as shown in the table below.

Table 87. Less Current Consumption Recommendations for GPIOs

Signal	Pin number	I/O	I/O type	Reset state	SW driver recommended (output state)
GPIO0	W15	I/O	1V8	0	0 logic level
GPIO1	R18	I/O	1V8	Z	0 logic level
GPIO2	U22	I/O	1V8	Z	0 logic level
GPIO3	V16	I/O	1V8	Z	0 logic level
GPIO4	AD19	I/O	1V8	Pull up	1 logic level
GPIO5	AD20	I/O	1V8	Pull up	1 logic level
GPIO6	AC20	I/O	1V8	Pull up	1 logic level
GPIO7	AC19	I/O	1V8	Pull up	1 logic level
GPIO8	AC21	I/O	1V8	Pull up	1 logic level
GPIO9	AC23	I/O	1V8	0	0 logic level
GPIO10	AD22	I/O	1V8	0	0 logic level
GPIO11	AD21	I/O	1V8	0	0 logic level
GPIO12	AC22	I/O	1V8	0	0 logic level
GPIO13	AD23	I/O	1V8	0	0 logic level
GPIO14	T16	I/O	1V8	Z	0 logic level
GPIO15	U17	I/O	1V8	Z	0 logic level
GPIO16	W17	I/O	1V8	Z	0 logic level
GPIO17	V13	I/O	1V8	Z	0 logic level
GPIO18	Y3	I/O	1V8	Z	0 logic level
GPIO19	AA17	I/O	2V8	Z	0 logic level
GPIO20	Y13	I/O	2V8	Undefined	0 logic level
GPIO21	AA13	I/O	2V8	Undefined	0 logic level
GPIO22	M15	I/O	2V8	Z	0 logic level
GPIO23	V17	I/O	2V8	Z	0 logic level
GPIO24	N16	I/O	2V8	Z	0 logic level

Signal	Pin number	I/O	I/O type	Reset state	SW driver recommended (output state)
GPIO25	Y19	I/O	2V8	Z	0 logic level
GPIO26	AA15	I/O	Open drain	Z	0 logic level
GPIO27	AA16	I/O	Open drain	Z	0 logic level
GPIO28	U15	I/O	2V8	Z	0 logic level
GPIO29	V12	I/O	2V8	Z	0 logic level
GPIO30	R13	I/O	2V8	Z	0 logic level
GPIO31	M14	I/O	2V8	Z	0 logic level
GPIO32	R15	I/O	2V8	Z	0 logic level
GPIO33	M13	I/O	2V8	Z	0 logic level
GPIO34	U16	I/O	2V8	Z	0 logic level
GPIO35	T18	I/O	2V8	Z	0 logic level
GPIO44	AB13	I/O	2V8	Undefined	0 logic level
GPIO45	Y17	I/O	1V8	Z	0 logic level
GPIO47	Y15	I/O	1V8	0	0 logic level
GPIO48	Y16	I/O	1V8	0	0 logic level

If the KEYBOARD and/or LED0 are not necessary, it is possible to disable them. Please refer to document [3] Open AT Framework AT Commands Interface Guide for Firmware 7.0 or later.

5. Technical Specifications

5.1. Ball Grid Array Pin Out

Pin labeling on the WMP module with Open AT Framework 2.0 is shown as below.

Table 88. Pin-out Labeling of Modules

WMP50 Signal Name	WMP 100 Signal Name	WMP 150 Signal Name	Description	I/O	Voltage Domain	MUX	MUX	MUX	Ball #
VBATT-RF	VBATT-RF	VBATT-RF	Power Supply	I	VBATT	VBATT-RF	–	–	A12, A13, A14, B12, B13, B14
VBATT-BB	VBATT-BB	VBATT-BB	Power Supply	I	VBATT	VBATT-BB	–	–	AC1, AC2, AD1, AD2
RF-OUT	RF-OUT	RF-OUT	Radio antenna connection	I/O	Analog RF	RF-OUT	–	–	B23
VCC_2V8	VCC_2V8	VCC_2V8	Power Supply	O	VCC_2V8	VCC_2V8	–	–	R1
VCC_1V8	VCC_1V8	VCC_1V8	Power Supply	O	VCC_1V8	VCC_1V8	–	–	AD5
BAT-RTC	BAT-RTC	BAT-RTC	Power Supply	I/O	BAT-RTC	BAT-RTC	–	–	U6
SIM-CLK	SIM-CLK	SIM-CLK	SIM clock	O	1V8 / 2V9	SIM-CLK	–	–	Y2
~SIM-RST	~SIM-RST	~SIM-RST	SIM reset	O	1V8 / 2V9	~SIM-RST	–	–	Y1
SIM-IO	SIM-IO	SIM-IO	SIM data	I/O	1V8 / 2V9	SIM-IO	–	–	W1
SIM-VCC	SIM-VCC	SIM-VCC	SIM power supply	O	1V8 / 2V9	SIM-VCC	–	–	W2
SIMPRES	SIMPRES	SIMPRES	SIM presence detection	I/O	VCC_1V8	SIMPRES	INT8#	GPIO18	Y3
MIC1P	MIC1P	MIC1P	Microphone input 1 positive	I	Analog	MIC1P	_	_	AC10
MIC1N	MIC1N	MIC1N	Microphone input 1 negative	I	Analog	MIC1N	_	_	AB10
MIC2P	MIC2P	MIC2P	Microphone input 2 positive	I	Analog	MIC2P	_	_	AC9
MIC2N	MIC2N	MIC2N	Microphone input 2 negative	I	Analog	MIC2N	_	_	AB9
SPK1P	SPK1P	SPK1P	Speaker output 1 positive	O	Analog	SPK1P	_	_	AC8

WMP50 Signal Name	WMP 100 Signal Name	WMP 150 Signal Name	Description	I/O	Voltage Domain	MUX	MUX	MUX	Ball #
SPK1N	SPK1N	SPK1N	Speaker output 1 negative	O	Analog	SPK1N	_	_	AB8
SPK2P	SPK2P	SPK2P	Speaker output 2 positive	O	Analog	SPK2P	_	_	AC7
SPK2N	SPK2N	SPK2N	Speaker output 2 negative	O	Analog	SPK2N	_	_	AB7
CHG-IN	CHG-IN	CHG-IN	Charger input voltage	I	Analog	CHG-IN	_	_	V2, V3
CHG-GATE	CHG-GATE	CHG-GATE	Charger transistor control output	O	Analog current	CHG-GATE	–	–	V4
ADC1 / BAT-TEMP	ADC1 / BAT-TEMP	ADC1 / BAT-TEMP	Analog to Digital converter 1	I	Analog	ADC1 / BAT-TEMP	_	_	N18
n/a	ADC3	ADC3	Analog to Digital converter 3	I	Analog	ADC3	_	_	M17
n/a	ADC2	ADC2	Analog to Digital converter 2	I	Analog	ADC2	_	_	N17
n/a	DAC0	DAC0	Digital to Analog converter	O	Analog	DAC0	_	_	V14
XIN_32K	XIN_32K	XIN_32K	Oscillator crystal input	I	Analog	XIN_32K	_	_	AC24
XOUT_32K	XOUT_32K	XOUT_32K	Oscillator crystal output	O	Analog	XOUT_32K	–	–	AB24
~RESET	~RESET	~RESET	Input Reset signal	I/O	VCC_1V8	~RESET	_	_	V6
~EXT-RESET	~EXT-RESET	~EXT-RESET	Output External reset	O	VCC_1V8	~EXT-RESET	–	–	AB14
ON/~OFF	ON/~OFF	ON/~OFF	Power ON	I	VBATT-BB	ON/~OFF	-	-	U5
BOOT	BOOT	BOOT	BOOT control	I	VCC_1V8	BOOT	_	_	W18
LED0	LED0	LED0	WMP100 & WMP150 Status LED	O	Open Drain VBATT	LED0	_	_	U3
BUZZER0	BUZZER0	BUZZER0	Buzzer output control	O	Open Drain VBATT	BUZZER0	–	–	U4
ROW0	ROW0	ROW0	Row Scan of keypad	I/O	VCC_1V8	ROW0	GPIO9	_	AC23
ROW1	ROW1	ROW1	Row Scan of keypad	I/O	VCC_1V8	ROW1	GPIO10	_	AD22
ROW2	ROW2	ROW2	Row Scan of keypad	I/O	VCC_1V8	ROW2	GPIO11	_	AD21
ROW3	ROW3	ROW3	Row Scan of keypad	I/O	VCC_1V8	ROW3	GPIO12	_	AC22
ROW4	ROW4	ROW4	Row Scan of keypad	I/O	VCC_1V8	ROW4	GPIO13	_	AD23

WMP50 Signal Name	WMP 100 Signal Name	WMP 150 Signal Name	Description	I/O	Voltage Domain	MUX	MUX	MUX	Ball #
COL0	COL0	COL0	Column Scan of keypad	I/O	VCC_1V8	COL0	GPIO4	_	AD19
COL1	COL1	COL1	Column Scan of keypad	I/O	VCC_1V8	COL1	GPIO5	_	AD20
COL2	COL2	COL2	Column Scan of keypad	I/O	VCC_1V8	COL2	GPIO6	_	AC20
COL3	COL3	COL3	Column Scan of keypad	I/O	VCC_1V8	COL3	GPIO7	_	AC19
COL4	COL4	COL4	Column Scan of keypad	I/O	VCC_1V8	COL4	GPIO8	_	AC21
n/a	PCM-SYNC	PCM-SYNC	PCM frame synchronization	O	VCC_1V8	PCM-SYNC	_	_	Y21
n/a	PCM-CLK	PCM-CLK	PCM clock	O	VCC_1V8	PCM-CLK	_	_	W21
n/a	PCM-OUT	PCM-OUT	PCM data output	O	VCC_1V8	PCM-OUT	_	_	W22
n/a	PCM-IN	PCM-IN	PCM data input	I	VCC_1V8	PCM-IN	_	_	AA22
CT103 / TXD1	CT103 / TXD1	CT103 / TXD1	Transmit serial data	I/O	VCC_2V8	CT103 / TXD1	GPIO36	_	R17
CT104 / RXD1	CT104 / RXD1	CT104 / RXD1	Receive serial data	I/O	VCC_2V8	CT104 / RXD1	GPIO37	INT9/INT2#	T13
~CT105 / RTS1	~CT105 / RTS1	~CT105 / RTS1	Ready To Send	I/O	VCC_2V8	~CT105 / RTS1	GPIO38	_	Y18
~CT106 / CTS1	~CT106 / CTS1	~CT106 / CTS1	Clear To Send	I/O	VCC_2V8	~CT106 / CTS1	GPIO39	_	N15
~CT107 / DSR1	~CT107 / DSR1	~CT107 / DSR1	Data Set Ready	I/O	VCC_2V8	~CT107 / DSR1	GPIO40	_	T12
~CT108-2 / DTR1	~CT108-2 / DTR1	~CT108-2 / DTR1	Data Serial Ready	I/O	VCC_2V8	~CT108-2 / DTR1	GPIO41	INT10/INT3#	M16
~CT109 / DCD1	~CT109 / DCD1	~CT109 / DCD1	Data Carrier Detect	I/O	VCC_2V8	~CT109 / DCD1	GPIO43	_	AB16
~CT125 / RI1	~CT125 / RI1	~CT125 / RI1	Ring Indicator	I/O	VCC_2V8	~CT125 / RI1	GPIO42	_	AA18
CT103 / TXD2	CT103 / TXD2	CT103 / TXD2	Transmit serial data	I/O	VCC_1V8	CT103 / TXD2	INT6#	GPIO14	T16
CT104 / RXD2	CT104 / RXD2	CT104 / RXD2	Receive serial data	I/O	VCC_1V8	CT104 / RXD2	GPIO15	INT11/INT4#	U17
~CT105 / RTS2	~CT105 / RTS2	~CT105 / RTS2	Ready To Send	I/O	VCC_1V8	~CT105 / RTS2	INT7#	GPIO17	V13
~CT106 / CTS2	~CT106 / CTS2	~CT106 / CTS2	Clear To Send	I/O	VCC_1V8	~CT106 / CTS2	GPIO16	_	W17
n/a	SCL1	SCL1	I²C serial clock	I/O	Open drain	SCL1	GPIO26	_	AA15
n/a	SDA1	SDA1	I²C serial data	I/O	Open Drain	SDA1	GPIO27	_	AA16
SPI1_CLK	SPI1_CLK	SPI1_CLK	SPI serial clock	I/O	VCC_2V8	SPI1-CLK	GPIO28	_	U15

WMP50 Signal Name	WMP 100 Signal Name	WMP 150 Signal Name	Description	I/O	Voltage Domain	MUX	MUX	MUX	Ball #
SPI1_IO	SPI1_IO	SPI1_IO	SPI serial data input and output	I/O	VCC_2V8	SPI1-IO	GPIO29	_	V12
SPI1-I	SPI1-I	SPI1-I	SPI serial data input only input	I/O	VCC_2V8	SPI1-I	GPIO30	_	R13
SPI1-LOAD	SPI1-LOAD	SPI1-LOAD	SPI load	I/O	VCC_2V8	SPI1-LOAD	INT5#	GPIO31	M14
n/a	SPI2-CLK	SPI2-CLK	SPI serial clock	I/O	VCC_2V8	SPI2-CLK	GPIO32	_	R15
n/a	SPI2-IO	SPI2-IO	SPI serial data input and output	I/O	VCC_2V8	SPI2-IO	GPIO33	_	M13
n/a	SPI2-I	SPI2-I	SPI serial data input only input	I/O	VCC_2V8	SPI2-I	GPIO34	_	U16
n/a	SPI2-LOAD	SPI2-LOAD	SPI load	I/O	VCC_2V8	SPI2-LOAD	INT4#	GPIO35	T18
INT1	INT3	INT3	Interruption input	I/O	VCC_2V8	INT1/INT3#	Not mux	_	V18
VPAD-USB	VPAD-USB	VPAD-USB	USB power supply	I	VPAD-USB	VPAD-USB	-	-	AB19
USB-DP	USB-DP	USB-DP	Universal Serial Bus Data positive	I/O	VPAD-USB	USB-DP	_	_	W19
USB-DM	USB-DM	USB-DM	Universal Serial Bus Data negative	I/O	VPAD-USB	USB-DM	_	_	AA20
USB-CN	USB-CN	USB-CN	Universal Serial Bus Connect	O	VPAD-USB	USB-CN	_	_	Y20
USB-DET	USB-DET	USB-DET	Universal Serial Bus interruption	I	VCC_1V8	USB-DET	_	_	R14
GPIO10	GPIO44	GPIO44	General Purpose Input Output	I/O	VCC_2V8	GPIO44	_	_	AB13
GPIO0	GPIO19	GPIO19	General Purpose Input Output	I/O	VCC_2V8	GPIO19	_	_	AA17
GPIO2	GPIO21	GPIO21	General Purpose Input Output	I/O	VCC_2V8	GPIO21	_	_	AA13
GPIO1	GPIO20	GPIO20	General Purpose Input Output	I/O	VCC_2V8	GPIO20	_	_	Y13
n/a	GPIO47	GPIO47	General Purpose Input Output	I/O	VCC_1V8	GPIO47	_	_	Y15
n/a	GPIO48	GPIO48	General Purpose Input Output	I/O	VCC_1V8	GPIO48	_	_	Y16

WMP50 Signal Name	WMP 100 Signal Name	WMP 150 Signal Name	Description	I/O	Voltage Domain	MUX	MUX	MUX	Ball #
n/a	GPIO0	GPIO0	General Purpose Input Output	I/O	VCC_1V8	GPIO0	_	_	W15
GPIO5	GPIO24	GPIO24	General Purpose Input Output	I/O	VCC_2V8	GPIO24	_	_	N16
GPIO3	GPIO22	GPIO22	General Purpose Input Output	I/O	VCC_2V8	GPIO22	_	_	M15
GPIO4	GPIO23	GPIO23	General Purpose Input Output	I/O	VCC_2V8	GPIO23	_	_	V17
n/a	INT0	INT0	Interruption input	I/O	VCC_1V8	INT0#	A26	GPIO3	V16
INT0	INT1	INT1	Interruption input	I/O	VCC_2V8	INT1/INT0#	GPIO25	_	Y19
GPIO11	INT2	INT2	Interruption input	I/O	VCC_1V8	INT2#	GPIO45	_	Y17
A0	A0	A0	Address bus	O	VCC_1V8	A0	_	_	T19
A1	A1	A1	Address bus	O	VCC_1V8	A1	_	_	U18
A2	A2	A2	Address bus	O	VCC_1V8	A2	_	_	U24
A3	A3	A3	Address bus	O	VCC_1V8	A3	_	_	P24
A4	A4	A4	Address bus	O	VCC_1V8	A4	_	_	N24
A5	A5	A5	Address bus	O	VCC_1V8	A5	_	_	M21
A6	A6	A6	Address bus	O	VCC_1V8	A6	_	_	M24
A7	A7	A7	Address bus	O	VCC_1V8	A7	_	_	N23
A8	A8	A8	Address bus	O	VCC_1V8	A8	_	_	R24
A9	A9	A9	Address bus	O	VCC_1V8	A9	_	_	R22
A10	A10	A10	Address bus	O	VCC_1V8	A10	_	_	P22
A11	A11	A11	Address bus	O	VCC_1V8	A11	_	_	T22
A12	A12	A12	Address bus	O	VCC_1V8	A12	_	_	R23
A13	A13	A13	Address bus	O	VCC_1V8	A13	_	_	M22
A14	A14	A14	Address bus	O	VCC_1V8	A14	_	_	P21
A15	A15	A15	Address bus	O	VCC_1V8	A15	_	_	R21
A16	A16	A16	Address bus	O	VCC_1V8	A16	_	_	P23
A17	A17	A17	Address bus	O	VCC_1V8	A17	_	_	T21
A18	A18	A18	Address bus	O	VCC_1V8	A18	_	_	T24
A19	A19	A19	Address bus	O	VCC_1V8	A19	_	_	M23
A20	A20	A20	Address bus	O	VCC_1V8	A20	_	_	N21
A21	A21	A21	Address bus	O	VCC_1V8	A21	_	_	N22
A22	A22	A22	Address bus	O	VCC_1V8	A22	_	_	M20
A23	A23	A23	Address bus	O	VCC_1V8	A23	_	_	N19
A24	A24	A24	Address bus	I/O	VCC_1V8	A24	GPIO2	_	U22

WMP50 Signal Name	WMP 100 Signal Name	WMP 150 Signal Name	Description	I/O	Voltage Domain	MUX	MUX	MUX	Ball #
D0	D0	D0	Data bus	I/O	VCC_1V8	D0	_	_	W24
D1	D1	D1	Data bus	I/O	VCC_1V8	D1	_	_	W23
D2	D2	D2	Data bus	I/O	VCC_1V8	D2	_	_	AA24
D3	D3	D3	Data bus	I/O	VCC_1V8	D3	_	_	Y23
D4	D4	D4	Data bus	I/O	VCC_1V8	D4	_	_	U21
D5	D5	D5	Data bus	I/O	VCC_1V8	D5	_	_	Y22
D6	D6	D6	Data bus	I/O	VCC_1V8	D6	_	_	Y24
D7	D7	D7	Data bus	I/O	VCC_1V8	D7	_	_	V21
D8	D8	D8	Data bus	I/O	VCC_1V8	D8	_	_	V20
D9	D9	D9	Data bus	I/O	VCC_1V8	D9	_	_	U20
D10	D10	D10	Data bus	I/O	VCC_1V8	D10	_	_	V24
D11	D11	D11	Data bus	I/O	VCC_1V8	D11	_	_	V22
D12	D12	D12	Data bus	I/O	VCC_1V8	D12	_	_	V23
D13	D13	D13	Data bus	I/O	VCC_1V8	D13	_	_	AA23
D14	D14	D14	Data bus	I/O	VCC_1V8	D14	_	_	U23
D15	D15	D15	Data bus	I/O	VCC_1V8	D15	_	_	T23
~WAIT	~WAIT	~WAIT	Burst Wait signal	I	VCC_1V8	~WAIT	_	_	R19
~CS0	~CS0	~CS0	Chip select Flash	O	VCC_1V8	~CS0	_	_	P19
~CS1	~CS1	~CS1	Chip select RAM	O	VCC_1V8	~CS1	_	_	R20
n/a	~CS2	~CS2	Chip select	I/O	VCC_1V8	~CS2	A25	GPIO1	R18
n/a	~CS3	~CS3	Chip select	O	VCC_1V8	~CS3	_	_	T17
CLKBURST	CLKBURST	CLKBURST	Burst clock	O	VCC_1V8	CLKBURST	_	_	M19
~ADV	~ADV	~ADV	Burst address valid signal	O	VCC_1V8	~ADV	_	_	U19
~WE-E	~WE-E	~WE-E	Write enable	O	VCC_1V8	~WE-E	_	_	P20
~OE-R/W	~OE-R/W	~OE-R/W	Read enable	O	VCC_1V8	~OE-R/W	_	_	N20

WMP50 Signal Name	WMP 100 Signal Name	WMP 150 Signal Name	Description	I/O	Voltage Domain	MUX	MUX	MUX	Ball #
~BE1	~BE1	~BE1	2nd byte enable	O	VCC_1V8	~BE1	_	_	P18
n/a	InSIM-Test 1	InSIM-Test 1	Embedded SIM personalization	I	1V8 / 2V9	InSIM-Test	_	_	U2

Note: The ground and reserved pins differ between the WMP100/150 and the WMP50. These pin-outs are presented in the following two tables.

(1): Pin "InSIM-Test" is connected to ground in normal operation mode. There is no impact on current application. This pin is not available on WMP50.

* The I/O direction information is concerning only the nominal signal. When the signal is configured in GPIO, it can always be an Input or an Output.

** For more information about the multiplexing of those signals, refer to section 3.10, General Purpose Input/Output.

The multiplexed external interrupt pin varies depending on the WMP embedded module variant. Refer to section 3.19, External Interrupt for more information.

Table 89. Ground and Reserved Pin-out Labeling of WMP50 Module

WMP100 Signal Name	WMP150 Signal Name	Definition	Pin
GND	GND	Ground	AA14, AD18, AA7, AD6, P9, U11, Y10, B6, D3, F10, G7, J3, L10, AA19, AD24, AA8, AD7, R10, U12, Y12, B7, D4, F11, G8, J4, L11, AA21, P15, AA9, AD8, R11, U2, Y7, B8, D5, F12, G9, J5, L12, AB15, T14, AB1, AD9, R12, U7, A1, B9, D6, F2, H1, J6, L2, AB17, T15, AB12, N1, R2, U8, A10, C1, D7, F3, H10, J7, L3, AB18, U14, AB2, N10, R3, U9, A11, C10, D8, F4, H11, J8, L4, AB21, V15, AB3, N2, R4, V1, A2, C11, D9, F5, H12, J9, L5, AB22, W13, AB4, N3, R5, V10, A3, C12, E1, F6, H2, K1, L6, AB23, W14, AB5, N7, R6, V11, A4, C3, E10, F7, H3, K10, L7, AC13, W16, AB6, N8, R7, V7, A5, C4, E11, F8, H4, K11, L8, AC14, Y14, AC12, N9, R8, V8, A6, C5, E12, F9, H5, K12, L9, AC15, AA1, AC3, P1, P13, P14, U13, R9, V9, A7, C6, E2, G1, H6, K2, M1, AC16, AA10, AC4, P10, T1, W10, A8, C7, E3, G10, H7, K3, M10, AC17, AA11, AC5, P2, T10, W11, A9, C8, E4, G11, H8, K4, M11, AC18, AA12, AC6, P3, T11, W12, B1, C9, E5, G12, H9, K5, M12, AD13, AA2, AD10, P4, T2, W3, B10, D1, E6, G2, J1, K6, M2, AD14, AA3, AD11, P5, T8, W6, B11, D10, E7, G3, J10, K7, M3, AD15, AA4, AD12, P6, T9, W7, B3, D11, E8, G4, J11, K8, M4, AD16, AA5, AD3, P7, U1, W8, B4, D12, E9, G5, J12, K9, M5, AD17, AA6, AD4, P8, U10, W9, B5, D2, F1, G6, J2, L1, M6, M7, B22, D19, F15, G23, J19, L15, M8, B24, D20, F16, G24, J20, L16, M9, C13, D21, F17, H13, J21, L17, A15, C14, D22, F18, H14, J22, L18, A16, C15, D23, F19, H15, J23, L19, A17, C16, D24, F20, H16, J24, L20, A18, C17, E13, F21, H17, K13, L21, A19, C18, E14, F22, H18, K14, L22, A20, C19, E15, F23, H19, K15, L23, A21, C20, E16, F24, H20, K16, L24A22, C21, E17, G13, H21, K17, M18A23, C22, E18, G14, H22, K18, A24, C23, E19, G15, H23, K19, B15, C24, E20, G16, H24, K20, B16, D13, E21, G17, J13, K21, B17, D14, E22, G18, J14, K22, B18, D15, E23, G19, J15, K23, B19, D16, E24, G20, J16, K24, B20, D17, F13, G21, J17, L13, B21, D18, F14, G22, J18, L14, M17 ,
RESERVED	RESERVED	Do not connect. (Left opened)	N13, N14, P16, P17, R16, V19, AB20, W20, N4, N5, N6, N11, N12, P11, P12, T3, T4, T5, T6, T7, V5, AC11, AB11, Y11, Y8, Y9, Y6, Y5, Y4, W4, W5, C2, B2, V14, Y17, Y15, Y16, W15, Y21, W21, W22, AA22, M13, U16, T17, N17, T20.

Table 90. Ground and Reserved Pin-out Labeling of WMP100 and WMP150 Modules

WMP50 Signal Name	Definition	Pin
GND	Ground	A1, A10, A11, A15, A16, A17, A18, A19, A2, A20, A21, A22, A23, A24, A3, A4, A5, A6, A7, A8, A9, B1, B10, B11, B15, B16, B17, B18, B19, B20, B21, B22, B24, B3, B4, B5, B6, B7, B8, B9, C1, C10, C11, C12, C13, C14, C15, C16, C17, C18, C19, C20, C21, C22, C23, C24, C3, C4, C5, C6, C7, C8, C9, D1, D10, D11, D12, D13, D14, D15, D16, D17, D18, D19, D2, D20, D21, D22, D23, D24, D3, D4, D5, D6, D7, D8, D9, E1, E10, E11, E12, E13, E14, E15, E16, E17, E18, E19, E2, E20, E21, E22, E23, E24, E3, E4, E5, E6, E7, E8, E9, F1, F10, F11, F12, F13, F14, F15, F16, F17, F18, F19, F2, F20, F21, F22, F23, F24, F3, F4, F5, F6, F7, F8, F9, G1, G10, G11, G12, G13, G14, G15, G16, G17, G18, G19, G2, G20, G21, G22, G23, G24, G3, G4, G5, G6, G7, G8, G9, H1, H10, H11, H12, H13, H14, H15, H16, H17, H18, H19, H2, H20, H21, H22, H23, H24, H3, H4, H5, H6, H7, H8, H9, J1, J10, J11, J12, J13, J14, J15, J16, J17, J18, J19, J2, J20, J21, J22, J23, J24, J3, J4, J5, J6, J7, J8, J9, K1, K10, K11, K12, K13, K14, K15, K16, K17, K18, K19, K2, K20, K21, K22, K23, K24, K3, K4, K5, K6, K7, K8, K9, L1, L10, L11, L12, L13, L14, L15, L16, L17, L18, L19, L2, L20, L21, L22, L23, L24, L3, L4, L5, L6, L7, L8, L9, M1, M10, M11, M12, M18, M2, M3, M4, M5, M6, M7, M8, M9, N1, N10, N2, N3, N7, N8, N9, P1, P10, P13, P14, P15, P2, P3, P4, P5, P6, P7, P8, P9, R10, R11, R12, R2, R3, R4, R5, R6, R7, R8, R9, T1, T10, T11, T14, T15, T2, T8, T9, U1, U10, U11, U12, U13, U14, U7, U8, U9, V1, V10, V11, V15, V7, V8, V9, W10, W11, W12, W13, W14, W16, W3, W6, W7, W8, W9, Y10, Y12, Y14, Y7, AA1, AA10, AA11, AA12, AA14, AA19, AA2, AA21, AA3, AA4, AA5, AA6, AA7, AA8, AA9, AB1, AB12, AB15, AB17, AB18, AB2, AB21, AB22, AB23, AB3, AB4, AB5, AB6, AC12, AC13, AC14, AC15, AC16, AC17, AC18, AC3, AC4, AC5, AC6, AD10, AD11, AD12, AD13, AD14, AD15, AD16, AD17, AD18, AD24, AD3, AD4, AD6, AD7, AD8, AD9
RESERVED	Do not connect. (Left opened)	B2, C2, N11, N12, N13, N14, N4, N5, N6, P11, P12, P16, P17, R16, T20, T3, T4, T5, T6, T7, V19, V5, W20, W4, W5, Y11, Y4, Y5, Y6, Y8, Y9, AB11, AB20, AC11

5.2. Recall of the Previous Labeling on Module with Open AT Framework 1.0

This table gives the correspondence labeling signals between WMP100 and WMP150 modules.

Each signal has strictly the same characteristics; this is only a new design.

Table 91. Pin-out Labeling Difference

Signal Name On WMP100	Signal Name On WMP150	Description	I/O	Ball Number
VBATT-RF	VBATT-RF	Power Supply	I	A12, A13, A14, B12, B13, B14
VBATT-BB	VBATT-BB	Power Supply	I	AC1, AC2, AD1, AD2
RF-OUT	RF-OUT	Radio antenna connection	I/O	B23
VCC_2V8	VCC_2V8	Power Supply	O	R1
VCC_1V8	VCC_1V8	Power Supply	O	AD5
BAT-RTC	BAT-RTC	Power Supply	I/O	U6
SIM-CLK	SIM-CLK	SIM clock	O	Y2
~SIM-RST	~SIM-RST	SIM reset	O	Y1

Signal Name On WMP100	Signal Name On WMP150	Description	I/O	Ball Number
SIM-IO	SIM-IO	SIM data	I/O	W1
SIM-VCC	SIM-VCC	SIM power supply	O	W2
SIMPRES / INT8 / GPIO18	SIMPRES	SIM presence detection	I/O	Y3
MIC1P	MIC1P	Microphone input 1 positive	I	AC10
MIC1N	MIC1N	Microphone input 1 negative	I	AB10
MIC2P	MIC2P	Microphone input 2 positive	I	AC9
MIC2N	MIC2N	Microphone input 2 negative	I	AB9
SPK1P	SPK1P	Speaker output 1 positive	O	AC8
SPK1N	SPK1N	Speaker output 1 negative	O	AB8
SPK2P	SPK2P	Speaker output 2 positive	O	AC7
SPK2N	SPK2N	Speaker output 2 negative	O	AB7
CHG-IN	CHG-IN	Charger input voltage	I	V2, V3
CHG-GATE	CHG-GATE	Charger transistor control output	O	V4
AUX-ADC2 / BAT-TEMP	ADC1 / BAT-TEMP	Analog to Digital converter 3	I	N18
AUX-ADC1	ADC3	Analog to Digital converter 2	I	M17
AUX-ADC0	ADC2	Analog to Digital converter 1	I	N17
AUX-DAC0	DAC0	Digital to Analog converter	O	V14
XIN_32K	XIN_32K	Oscillator crystal input	I	AC24
XOUT_32K	XOUT_32K	Oscillator crystal output	O	AB24
~RESET	~RESET	Input Reset signal	I/O	V6
~EXT-RESET	~EXT-RESET	Output External reset	O	AB14
ON/~OFF	ON/~OFF	Power ON	I	U5
BOOT	BOOT	BOOT control	I	W18
Flash LED	LED0	WMP100 & WMP150 Status LED	O	U3
BUZZ-OUT	BUZZER0	Buzzer output control	O	U4
ROW0 / GPIO9	ROW0	Row Scan of keypad	I/O	AC23
ROW1 / GPIO10	ROW1	Row Scan of keypad	I/O	AD22
ROW2 / GPIO11	ROW2	Row Scan of keypad	I/O	AD21
ROW3 / GPIO12	ROW3	Row Scan of keypad	I/O	AC22
ROW4 / GPIO13	ROW4	Row Scan of keypad	I/O	AD23
COL0 / GPIO4	COL0	Column Scan of keypad	I/O	AD19
COL1 / GPIO5	COL1	Column Scan of keypad	I/O	AD20
COL2 / GPIO6	COL2	Column Scan of keypad	I/O	AC20
COL3 / GPIO7	COL3	Column Scan of keypad	I/O	AC19
COL4 / GPIO8	COL4	Column Scan of keypad	I/O	AC21
PCM-SYNC	PCM-SYNC	PCM frame synchronization	O	Y21
PCM-CLK	PCM-CLK	PCM clock	O	W21
PCM-OUT	PCM-OUT	PCM data output	O	W22
PCM-IN	PCM-IN	PCM data input	I	AA22

Signal Name On WMP100	Signal Name On WMP150	Description	I/O	Ball Number
CT103 / TXD1 / GPIO36	CT103 / TXD1	Transmit serial data	I/O	R17
CT104 / RXD1 / GPIO37	CT104 / RXD1	Receive serial data	I/O	T13
~CT105 / RTS1 / GPIO38	~CT105 / RTS1	Ready To Send	I/O	Y18
~CT106 / CTS1 / GPIO39	~CT106 / CTS1	Clear To Send	I/O	N15
~CT107 / DSR1	~CT107 / DSR1	Data Set Ready	I/O	T12
~CT108-2 / DTR1 / GPIO41	~CT108-2 / DTR1	Data Serial Ready	I/O	M16
~CT109 / DCD1 / GPIO43	~CT109 / DCD1	Data Carrier Detect	I/O	AB16
~CT125 / RI1 / GPIO42	~CT125 / RI1	Ring Indicator	I/O	AA18
CT103 / TXD2 / INT6 / GPIO14	CT103 / TXD2	Transmit serial data	I/O	T16
CT104 / RXD2 / GPIO15	CT104 / RXD2	Receive serial data	I/O	U17
~CT105 / RTS2 / INT7 / GPIO17	~CT105 / RTS2	Ready To Send	I/O	V13
~CT106 / CTS2 / GPIO16	~CT106 / CTS2	Clear To Send	I/O	W17
SCL / GPIO26	SCL1	I²C serial clock	I/O	AA15
SDA / GPIO27	SDA1	I²C serial data	I/O	AA16
SPI1-CLK / GPIO28	SPI1_CLK	SPI serial clock	I/O	U15
SPI1-IO / GPIO29	SPI1_IO	SPI serial data input and output	I/O	V12
SPI1-I / GPIO30	SPI1-I	SPI serial data input only input	I/O	R13
SPI1-CS / INT5 / GPIO31	SPI1-LOAD	SPI load	I/O	M14
SPI2-CLK / GPIO32	SPI2-CLK	SPI serial clock	I/O	R15
SPI2-IO / GPIO33	SPI2-IO	SPI serial data input and output	I/O	M13
SPI2-I / GPIO34	SPI2-I	SPI serial data input only input	I/O	U16
SPI2-CS / INT4 / GPIO35	SPI2- LOAD	SPI load	I/O	T18
INT3	INT3	Interruption input	I/O	V18
VPAD-USB	VPAD-USB	USB power supply	I	AB19
USB-DP	USB-DP	Universal Serial Bus Data positive	I/O	W19
USB-DM	USB-DM	Universal Serial Bus Data negative	I/O	AA20
USB-CN	USB-CN	Universal Serial Bus Connect	O	Y20
USB-DET	USB-DET	Universal Serial Bus interruption	I	R14
GPIO44	GPIO44	General Purpose Input Output	I/O	AB13

Signal Name On WMP100	Signal Name On WMP150	Description	I/O	Ball Number
GPIO19	GPIO19	General Purpose Input Output	I/O	AA17
GPIO21	GPIO21	General Purpose Input Output	I/O	AA13
GPIO20	GPIO20	General Purpose Input Output	I/O	Y13
GPIO47	GPIO47	General Purpose Input Output	I/O	Y15
GPIO48	GPIO48	General Purpose Input Output	I/O	Y16
GPIO0	GPIO0	General Purpose Input Output	I/O	W15
GPIO24	GPIO24	General Purpose Input Output	I/O	N16
GPIO22	GPIO22	General Purpose Input Output	I/O	M15
GPIO23	GPIO23	General Purpose Input Output	I/O	V17
INT0 / A26 / GPIO3	INT0	Interruption input	I/O	V16
INT1 / GPIO25	INT1	Interruption input	I/O	Y19
INT2 / GPIO45	INT2	Interruption input	I/O	Y17
A0	A0	Address bus	O	T19
A1	A1	Address bus	O	U18
A2	A2	Address bus	O	U24
A3	A3	Address bus	O	P24
A4	A4	Address bus	O	N24
A5	A5	Address bus	O	M21
A6	A6	Address bus	O	M24
A7	A7	Address bus	O	N23
A8	A8	Address bus	O	R24
A9	A9	Address bus	O	R22
A10	A10	Address bus	O	P22
A11	A11	Address bus	O	T22
A12	A12	Address bus	O	R23
A13	A13	Address bus	O	M22
A14	A14	Address bus	O	P21
A15	A15	Address bus	O	R21
A16	A16	Address bus	O	P23
A17	A17	Address bus	O	T21
A18	A18	Address bus	O	T24
A19	A19	Address bus	O	M23
A20	A20	Address bus	O	N21
A21	A21	Address bus	O	N22
A22	A22	Address bus	O	M20
A23	A23	Address bus	O	N19
A24 / GPIO2	A24	Address bus	I/O	U22
D0	D0	Data bus	I/O	W24
D1	D1	Data bus	I/O	W23
D2	D2	Data bus	I/O	AA24
D3	D3	Data bus	I/O	Y23
D4	D4	Data bus	I/O	U21

Signal Name On WMP100	Signal Name On WMP150	Description	I/O	Ball Number
D5	D5	Data bus	I/O	Y22
D6	D6	Data bus	I/O	Y24
D7	D7	Data bus	I/O	V21
D8	D8	Data bus	I/O	V20
D9	D9	Data bus	I/O	U20
D10	D10	Data bus	I/O	V24
D11	D11	Data bus	I/O	V22
D12	D12	Data bus	I/O	V23
D13	D13	Data bus	I/O	AA23
D14	D14	Data bus	I/O	U23
D15	D15	Data bus	I/O	T23
~WAIT	~WAIT	Burst Wait signal	I	R19
~CS0	~CS0	Chip select Flash	O	P19
~CS1	~CS1	Chip select RAM	O	R20
~CS2 / A25 / GPIO1	~CS2	Chip select	I/O	R18
~CS3	~CS3	Chip select	O	T17
CLKBURST	CLKBURST	Burst clock	O	M19
~ADV	~ADV	Burst address valid signal	O	U19
~WE-E	~WE-E	Write enable	O	P20
~OE-R/W	~OE-R/W	Read enable	O	N20
~BE1	~BE1	2nd byte enable	O	P18
GND	Ground	A1, A10, A11, A15, A16, A17, A18, A19, A2, A20, A21, A22, A23, A24, A3, A4, A5, A6, A7, A8, A9, B1, B10, B11, B15, B16, B17, B18, B19, B20, B21, B22, B24, B3, B4, B5, B6, B7, B8, B9, C1, C10, C11, C12, C13, C14, C15, C16, C17, C18, C19, C20, C21, C22, C23, C24, C3, C4, C5, C6, C7, C8, C9, D1, D10, D11, D12, D13, D14, D15, D16, D17, D18, D19, D2, D20, D21, D22, D23, D24, D3, D4, D5, D6, D7, D8, D9, E1, E10, E11, E12, E13, E14, E15, E16, E17, E18, E19, E2, E20, E21, E22, E23, E24, E3, E4, E5, E6, E7, E8, E9, F1, F10, F11, F12, F13, F14, F15, F16, F17, F18, F19, F2, F20, F21, F22, F23, F24, F3, F4, F5, F6, F7, F8, F9, G1, G10, G11, G12, G13, G14, G15, G16, G17, G18, G19, G2, G20, G21, G22, G23, G24, G3, G4, G5, G6, G7, G8, G9, H1, H10, H11, H12, H13, H14, H15, H16, H17, H18, H19, H2, H20, H21, H22, H23, H24, H3, H4, H5, H6, H7, H8, H9, J1, J10, J11, J12, J13, J14, J15, J16, J17, J18, J19, J2, J20, J21, J22, J23, J24, J3, J4, J5, J6, J7, J8, J9, K1, K10, K11, K12, K13, K14, K15, K16, K17, K18, K19, K2, K20, K21, K22, K23, K24, K3, K4, K5, K6, K7, K8, K9, L1, L10, L11, L12, L13, L14, L15, L16, L17, L18, L19, L2, L20, L21, L22, L23, L24, L3, L4, L5, L6, L7, L8, L9, M1, M10, M11, M12, M18, M2, M3, M4, M5, M6, M7, M8, M9, N1, N10, N2, N3, N7, N8, N9, P1, P10, P13, P14, P15, P2, P3, P4, P5, P6, P7, P8, P9, R10, R11, R12, R2, R3, R4, R5, R6, R7, R8, R9, T1, T10, T11, T14, T15, T2, T8, T9, U1, U10, U11, U12, U13, U14, U2, U7, U8, U9, V1, V10, V11, V15, V7, V8, V9, W10, W11, W12, W13, W14, W16, W3, W6, W7, W8, W9, Y10, Y12, Y14, Y7, AA1, AA10, AA11, AA12, AA14, AA19, AA2, AA21, AA3, AA4, AA5, AA6, AA7, AA8, AA9, AB1, AB12, AB15, AB17, AB18, AB2, AB21, AB22, AB23, AB3, AB4, AB5, AB6, AC12, AC13, AC14, AC15, AC16, AC17, AC18, AC3, AC4, AC5, AC6, AD10, AD11, AD12, AD13, AD14, AD15, AD16, AD17, AD18, AD24, AD3, AD4, AD6, AD7, AD8, AD9		

Signal Name On WMP100	Signal Name On WMP150	Description	I/O	Ball Number
RESERVED	Do not connect. (Left opened)	B2, C2, N11, N12, N13, N14, N4, N5, N6, P11, P12, P16, P17, R16, T20, T3, T4, T5, T6, T7, V19, V5, W20, W4, W5, Y11, Y4, Y5, Y6, Y8, Y9, AB11, AB20, AC11		

5.3. Environmental Specifications

5.3.1. Status Classification

Sierra Wireless specifies following temperature range of WMP product.

The module is compliant with following operating class.

Table 92. Operating Class Temperature Range

Conditions	Temperature range
Operating / Class A	-20 °C to +55°C
Operating / Storage / Class B	-40 °C to +85°C

Class A:

The WMP module shall have full function during and after an external influence. The GSM performance shall meet the minimum ETSI requirements.

Class B:

Any functions can be out of specified tolerances. All the functions will be going back to normal tolerances automatically after that the external influence has been removed. Performance is allowed to go outside of the minimum ETSI requirements, but it must be possible to connect a call and send an SMS.

5.3.2. Case of Ground Vehicle Use

Table 93. Case of Ground Vehicle Use

Climatic Range[1]	Ground Vehicle Use
Temperature	-25 °C to +70°C
Relative Humidity	10 % to 95 %

(1): Refer to class 5K2 from IEC 60721-3-5 stand

Table 94. Environmental Resistance Stress Test

Environmental tests (ETSI EN 300 019-2)		Environmental classes (ETSI EN 300 019-1)		
Type of Test	**Standards**	**Storage** **(ETSI EN 300 019-1-1)** **Class 1.2**[2]	**Transportation** **(ETSI EN 300 019-1-2)** **Class 2.3**[3]	**Ground vehicle use** **Weather protected locations** **(ETSI EN 300 019-1-5)** **Class 5.1**[4]
Cold	**IEC 60068 - 2 - 1 : Ab/Ad**	– 25 °C, 72 h	– 40 °C, 72 h	– 25 °C, 16 h
Dry heat	**IEC 60068 - 2 - 2 : Bb/Bd**	+ 70 °C, 16 h	+ 70 °C, 72 h	+ 70 °C, 16 h
Change of temperature	**IEC 60068 - 2 - 14 : Na/Nb**	none	– 40 °C to + 30 °C 5 cycles t1 = 3 h 1 $K.min^{-1}$	– 25 °C to + 30 °C 5 cycles t1 = 3 h 1 $K.min^{-1}$
Damp heat	**IEC 60068-2-56 : Cb**	+ 30 °C, 93 % RH 96 h	+ 40 °C, 93 % RH 96 h	+ 40 °C, 93 % RH 96 h
Damp heat, cyclic	**IEC 60068-2-30 : Db Variant 2**	–	+ 40 °C 90 % to 100 % RH 2 cycles	+ 40°C 90 % to 100 % RH 2 cycles
Impacting water	**IEC 60068-2-18 Test Rb and guidance : water**	–	Test Rb Method 2.2 1 min. m^{-2}, 5 min minimum[5]	–

(2): This class is a combination of 1K4/1Z2/1Z3/1Z5/1B2/1C2/1S3/1M2 in IEC 60721-3-1.

(3): This class is a combination of 2K4/2B2/2C2/2S2/2M2 in IEC 60721-3-2.

(4): This class is a combination of 5K2/2B2/5C2/5F1/5S2/5M3 in IEC 60721-3-5.

(5): Taking into account the evolutions of CEI TR 60721-4-2:2003

Table 95. Mechanical Resistance Stress Tests

Environmental tests (ETSI EN 300 019-2)		Environmental classes (ETSI EN 300 019-1)		
Type of Test	**Standards**	**Storage** (ETSI EN 300 019-1-1) Class 1.2[6]	**Transportation** (ETSI EN 300 019-1-2) Class 2.3[7]	**Ground vehicle use** Weather protected locations (ETSI EN 300 019-1-5) Class 5.1[8]
Vibration (sinusoidal)	**IEC 60068-2-6 : Fc**	5 Hz - 62 Hz : 5 $mm.s^{-1}$ 62 Hz - 200 Hz : 2 $m.s^{-2}$ 3 axes 5 cycles per axe	–	–
Vibration (random)	**IEC 60068-2-64 : Fh**	–	5 - 20 Hz : 1.0 $m^2.s^{-3}$ 20 - 200 Hz : - 3 $dB.octave^{-1}$ 3 axes, 30 min per axe	5 - 20 Hz : 1.92 $m^2.s^{-3}$ 20 - 500 Hz : - 3 $dB.octave^{-1}$ 3 axes, 10 min per axe
Shock (half-sine)	**IEC 60068-2-27 : Ea**	–	–	1 000 $m.s^{-2}$ 6 ms 3 shocks 6 directions
Bump	**IEC 60068-2-29 : Eb**	–	180 $m.s^{-2}$ 6 ms 100 bumps 3 axes, 2 directions[9]	250 $m.s^{-2}$ 6 ms 500 bumps 3 axes, 2 directions
Free fall	**ISO 4180 – 2**	–	One fall on each side (see table 1)	–
Drop and topple	**IEC 60068-2-31 : Ec**	–	0.1 m One drop on relevant corner[5] One topple about each bottom edge[5]	–

Table 1

Mass [kg]	Free fall test height [m]
< 10	1.0
< 15	1.0
< 20	0.8
< 30	0.6
< 40	0.5
< 50	0.4
< 100	0.3

(6): This class is a combination of 1K4/1Z2/1Z3/1Z5/1B2/1C2/1S3/1M2 in IEC 60721-3-1.

(7): This class is a combination of 2K4/2B2/2C2/2S2/2M2 in IEC 60721-3-2.

(8): This class is a combination of 5K2/2B2/5C2/5F1/5S2/5M3 in IEC 60721-3-5.

(9): If mass lower than 50kg.

5.3.3. Case of Portable Use – Non Weather Protected Location

Table 96. Case of Portable Use without Weather Protected Location

Climatic Range[10]	Portable use
Temperature	-40 °C to +70°C
Relative Humidity	5 % to 100 %

(10): Refer to class 7K4 from IEC 60721-3-7 standard

Table 97. Environmental Resistance Stress Test

Environmental tests (ETSI EN 300 019-2)		Environmental classes (ETSI EN 300 019-1)		
Type of Test	**Standards**	**Storage** **(ETSI EN 300 019-1-1) Class 1.2(11)**	**Transportation** **(ETSI EN 300 019-1-2) Class 2.3(12)**	**Portable use Non weather protected locations (ETSI EN 300 019-1-7) Class 7.3E(13)**
Cold	**IEC 60068-2-1 : Ab/Ad**	– 25 °C, 72 h	– 40°C, 72 h	– 40°C, 16 h
Dry heat	**IEC 60068-2-2 : Bb/Bd**	+ 70 °C, 16 h	+ 70°C, 72 h	+ 70°C, 16 h
Change of temperature	**IEC 60068-2-14 : Na/Nb**	–	– 40°C to + 30 °C 5 cycles t_1 = 3 h 1 K.min^{-1}	– 25°C to + 30 °C 3 cycles t_1 = 3 h 1 K.min^{-1}
Damp heat	**IEC 60068-2-56 : Cb**	+ 30°C, 93 % RH 96 h	+ 40°C, 93% RH 96 h	+ 40°C, 93% RH 21 days
Damp heat, cyclic	**IEC 60068-2-30 : Db Variant 2**	none	+ 40°C, 90% to 100% RH 2 cycles	+ 40°C, 90% to 100% RH 6 cycles
Impacting water	**IEC 60068-2-18 Test Rb and guidance : water**	–	Test Rb Method 2.2 1 min. m^{-2}, 5 min minimum(14)	Test Rb Method 1.2 0,01 m^3.min^{-1}, 90 kPa 1 min.m^{-2}, 5 min minimum

(11): This class is a combination of 1K4/1Z2/1Z3/1Z5/1B2/1C2/1S3/1M2 in IEC 60721-3-1.

(12): This class is a combination of 2K4/2B2/2C2/2S2/2M2 in IEC 60721-3-2.

(13): This class is a combination of 7K4/7Z2/7Z6/7Z9/7B2/7C2/7S2/7M3 in IEC 60721-3-7.

(14): Taking into account the evolutions of CEI TR 60721-4-2:2003.

Table 98. Mechanical Resistance Stress Tests

Environmental tests (ETSI EN 300 019-2)		Environmental classes (ETSI EN 300 019-1)		
Type of Test	**Standards**	**Storage** **(ETSI EN 300 019-1-1) Class 1.2[15]**	**Transportation** **(ETSI EN 300 019-1-2) Class 2.3[16]**	**Portable use Non weather protected locations** **(ETSI EN 300 019-1-7) Class 7.3E[17]**
Vibration (random)	**IEC 60068-2-64 : Fh**	–	5 - 20 Hz : 1.0 $m^2.s^{-3}$ 20 - 200 Hz : -3 $dB.octave^{-1}$ 3 axes 30 min per axe	10 - 12 Hz : 2 $m^2.s^{-3}$ 12 - 150 Hz : -3 $dB.octave^{-1}$ 3 axes 30 min per axe
Shock (half-sine)	**IEC 60068-2-27 : Ea**	–	–	1 000 $m.s^{-2}$ 6 ms 3 shocks 6 directions
Bump	**IEC 60068-2-29 : Eb**	–	180 $m.s^{-2}$ 6 ms 100 bumps 3 axes, 2 directions[18]	250 $m.s^{-2}$ 6 ms 100 bumps 3 axes, 2 directions
Free fall	**ISO 4180 – 2**	–	One fall on each side (see table 2)	–
	IEC 60068-2-32	–	–	<1 kg, 1.0 m / <10 kg, 0.5 m < 50 kg, 0.25 m 2 falls in each specified attitude
Drop and topple	**IEC 60068-2-31 : Ec**	–	0.1 m One drop on relevant corner[5] One topple about each bottom edge[5]	0.1 m 4 edges and 4 corners

Table 2

Mass [kg]	Free fall test height [m]
< 10	1.0
< 15	1.0
< 20	0.8
< 30	0.6
< 40	0.5
< 50	0.4
< 100	0.3

(15): This class is a combination of 1K4/1Z2/1Z3/1Z5/1B2/1C2/1S3/1M2 in IEC 60721-3-1.

(16): This class is a combination of 2K4/2B2/2C2/2S2/2M2 in IEC 60721-3-2.

(17): This class is a combination of 7K4/7Z2/7Z6/7Z9/7B2/7C2/7S2/7M3 in IEC 60721-3-7.

(18): If mass lower than 50kg.

5.3.4. Case of Stationary Use – Weather Protected/Sheltered Location

Table 99. Case of Portable Use with Weather Protected Location

Climatic Range[19]	Stationary Use Weather Protected Location	Stationary Use Sheltered Location
Temperature	-40 °C to +40°C	-40 °C to +70°C
Relative Humidity	10 % to 100 %	10 % to 100 %

(19): Refer to class 3K7 and 3K7L from IEC 60721-3-3 standard

Table 100. Environmental Resistance Stress Test

Environmental tests (ETSI EN 300 019-2)		Environmental classes (ETSI EN 300 019-1)			
Type of Test	Standards	Storage (ETSI EN 300 019-1-1) Class 1.2(20)	Transportation (ETSI EN 300 019-1-2) Class 2.3(21)	Stationary use Weather protected locations (ETSI EN 300 019-1-3) Class 3.1[22]	Stationary use Sheltered locations (ETSI EN 300 019-1-3) Class 3.5[23]
Cold	IEC 60068 - 2 - 1 : Ab/Ad	– 25 °C, 72 h	– 40°C, 72 h	+ 5°C, 16 h	– 40 °C, 16 h
Dry heat	IEC 60068 - 2 - 2 : Bb/Bd	+ 70 °C, 16 h	+ 70°C, 72 h	+ 40°C, 16 h	+ 40°C, 16 h
Change of temperature	IEC 60068 - 2 - 14 : Na/Nb	–	– 40°C to + 30 °C 5 cycles t_1 = 3 h 1 K.min^{-1}	– 40 °C to ambient 2 cycles t_1 = 3 h 1 K.min^{-1}	– 40 °C to + 40 °C 2 cycles t_1 = 3 h 1 K.min^{-1}
Damp heat	IEC 60068-2-56 : Cb	+ 30°C, 93 % RH 96 h	+ 40°C, 93% RH 96 h	+ 30°C, 85% RH 96 h	+ 35°C, 93% RH 96 h
Damp heat, cyclic	IEC 60068-2-30 : Db Variant 1	–	+ 40°C 90% to 100% RH 2 cycles	–	+ 35 °C 90% to 100% RH 2 cycles
Impacting water	IEC 60068-2-18 Test Rb and guidance : water	–	Test Rb Method 2.2 1 min. m^{-2}, 5 min minimum(24)	–	–

(20): This class is a combination of 1K4/1Z2/1Z3/1Z5/1B2/1C2/1S3/1M2 in IEC 60721-3-1.

(21): This class is a combination of 2K4/2B2/2C2/2S2/2M2 in IEC 60721-3-1.

(22): This class is a combination of 3K3/3Z2/3Z4/3B1/3C2(3C1)/3S2/3M1 in IEC 60721-3-3.

(23): This class is a combination of 3K7 low /3Z2/3Z6/3Z7/3Z8/3B2/3C2(3C3)/3S3/3M5(3M3) in IEC 60721-3-3.

(24): Taking into account the evolutions of CEI TR 60721-4-2:2003.

Table 101. Mechanical Resistance Stress Tests

Environmental tests (ETSI EN 300 019-2)		Environmental classes (ETSI EN 300 019-1)			
Type of Test	**Standards**	**Storage (ETSI EN 300 019-1-1) Class 1.2[25]**	**Transportation (ETSI EN 300 019-1-2) Class 2.3[26]**	**Stationary use Weather protected locations (ETSI EN 300 019-1-3) Class 3.1[27]**	**Stationary use Sheltered locations (ETSI EN 300 019-1-3) Class 3.5[28]**
Vibration (sinusoidal)	**IEC 60068-2-6 : Fc**	5 Hz - 62 Hz : 5 $mm.s^{-1}$ 62 Hz - 200 Hz : 2 $m.s^{-2}$ 3 axes 5 cycles per axe	–	–	5 Hz - 62 Hz : 5 $mm.s^{-1}$ 62 Hz - 200 Hz : 2 $m.s^{-2}$ 3 axes 5 cycles per axe
Vibration (random)	**IEC 60068-2-64 : Fh**	–	5 - 20 Hz / 1.0 $m^2.s^{-3}$ 20 - 200 Hz / -3 $dB.octave^{-1}$ 3 axes 30 min per axe	–	5 - 10 Hz : 12 $dB.octave^{-1}$ 10 - 50 Hz : 0,04 $m^2.s^{-3}$ 50 - 100 Hz : -12 $dB.octave^{-1}$ 3 axes 30 min per axe
Shock (half-sine)	**IEC 60068-2-27 : Ea**	–	–	30 $m.s^{-2}$ 11 ms 3 shocks in each direction, 6 directions	30 $m.s^{-2}$ 11 ms 3 shocks in each direction, 6 directions
Bump	**IEC 60068-2-29 : Eb**	–	180 $m.s^{-2}$ 6 ms 100 bumps / 6 directions[29]	–	50 $m.s^{-2}$ 11 ms, Half sine 100 bumps / 6 directions
Free fall	**ISO 4180 – 2**	–	One fall on each side (see table 3)	–	–
Drop and topple	**IEC 60068-2-31 : Ec**	–	0.1 m One drop on relevant corner[5] One topple about each bottom edge[30]	–	–

Table 3

Mass [kg]	Free fall test height [m]
< 10	1.0
< 15	1.0
< 20	0.8
< 30	0.6
< 40	0.5
< 50	0.4
< 100	0.3

(25): This class is a combination of 1K4/1Z2/1Z3/1Z5/1B2/1C2/1S3/1M2 in IEC 60721-3-1.

(26): This class is a combination of 2K4/2B2/2C2/2S2/2M2 in IEC 60721-3-1.

(27): This class is a combination of 3K3/3Z2/3Z4/3B1/3C2(3C1)/3S2/3M1 in IEC 60721-3-3.

(28): This class is a combination of 3K7 low /3Z2/3Z6/3Z7/3Z8/3B2/3C2(3C3)/3S3/3M5(3M3) in IEC 60721-3-3.

(29): If mass lower than 50kg.

(30): Taking into account the evolutions of CEI TR 60721-4-2:2003.

5.4. MSL Level

The WMP modules are MSL 3 and 2, reflows are allowed on customer side including one for rework of the component.

If the product is double side, the module should be assembled on the side that will see only one reflow.

5.5. Mechanical Specifications

5.5.1. Physical Characteristics

The WMP modules have a complete self-contained shield. They differ from mechanical dimensions as described below.

Table 102. Mechanical Difference of WMP modules

Mechanical Difference	WMP50, WMP100, WMP100 Embedded SIM	WMP150, WMP150 Embedded SIM
Shield Type	Soldered can	Soldered belt and Clip-on cover
Dimension, Thickness	25x25x3.65 mm	25x25x3.78 mm
Weight	4.25 g	4.25 g

5.5.2. Mechanical Drawings for the WMP100 and WMP150

Refer to the following pages for the mechanical specifications of WMP100 and WMP150 modules.

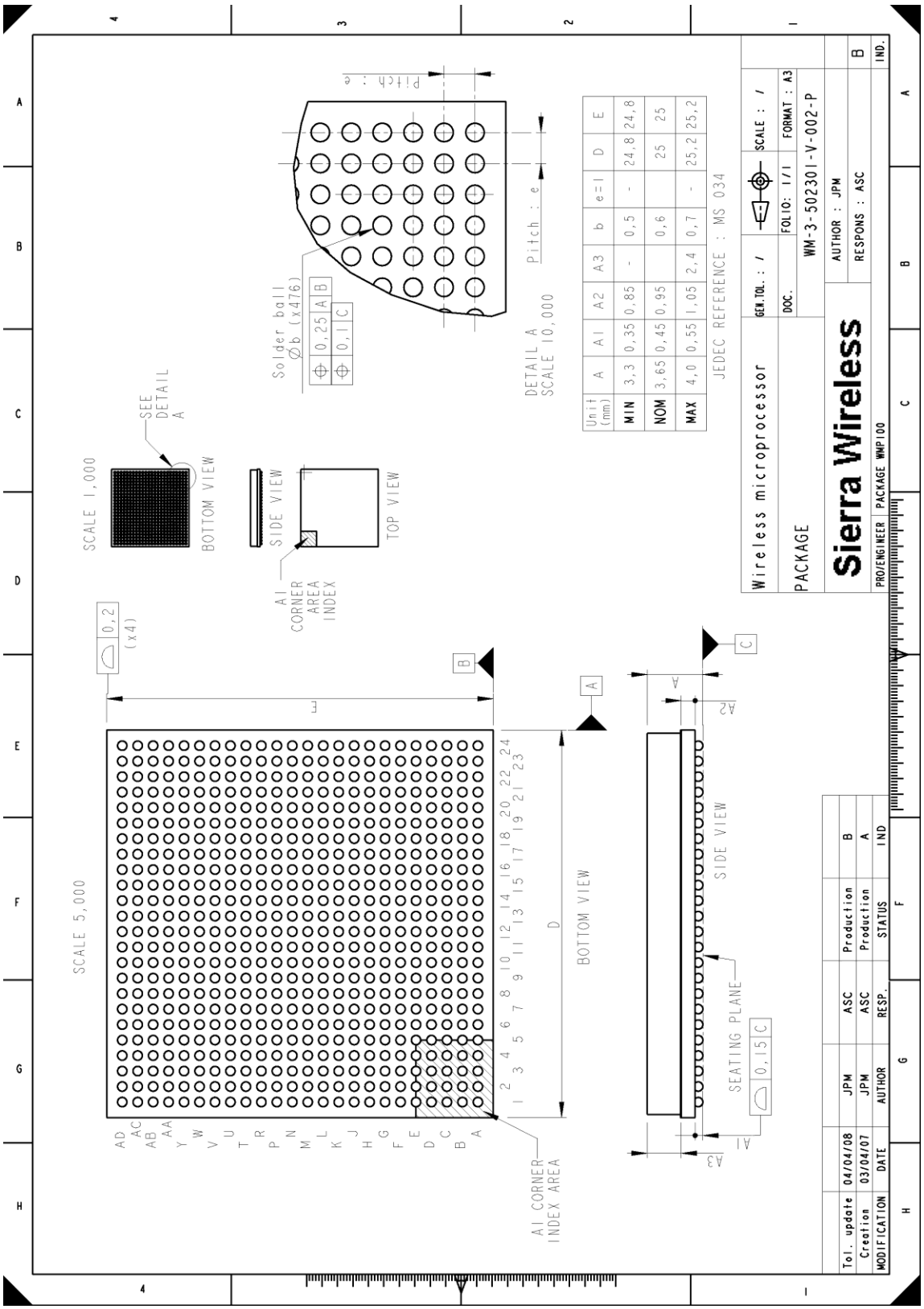


Figure 89. Mechanical Drawing of WMP100 (Bottom View)

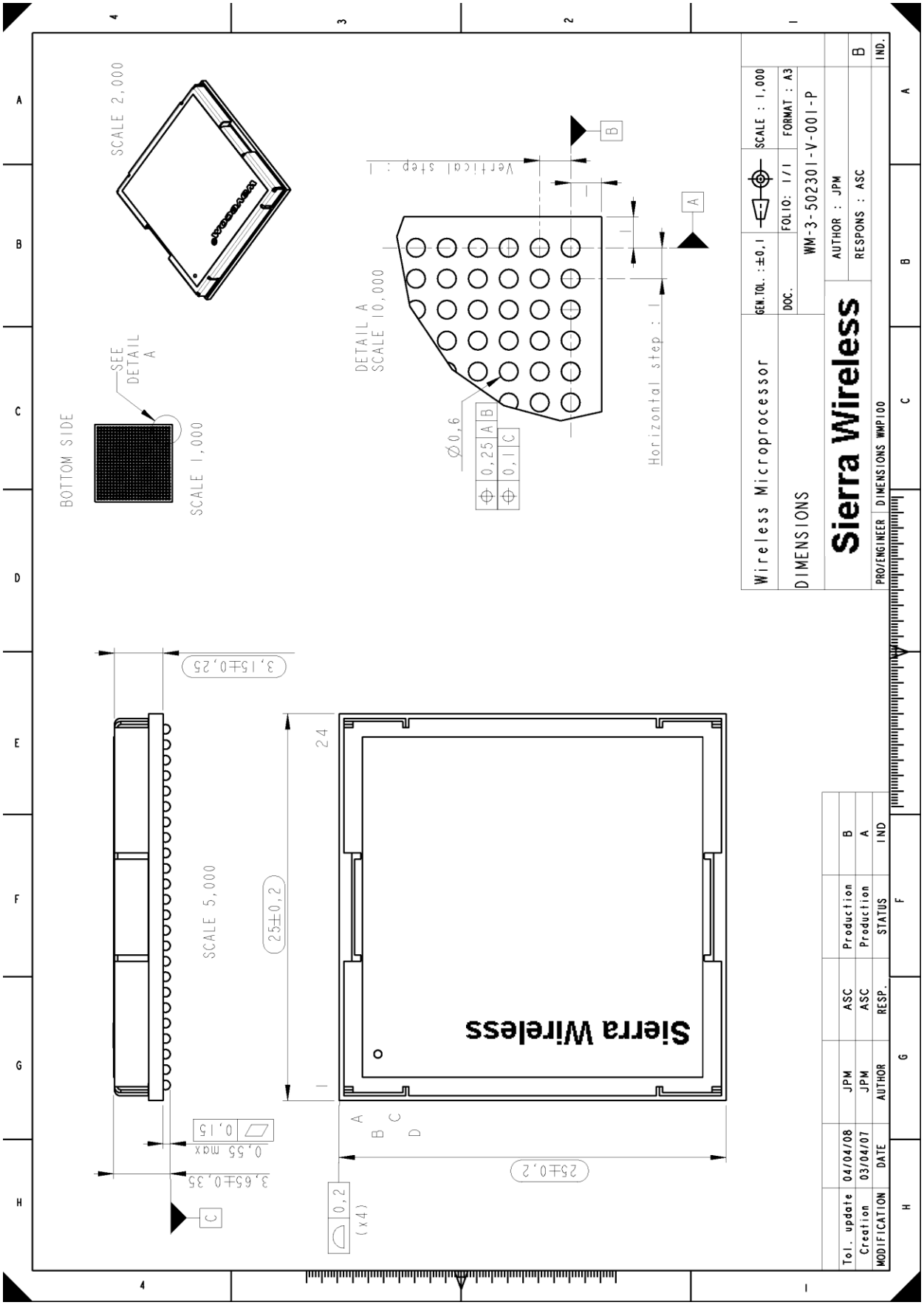
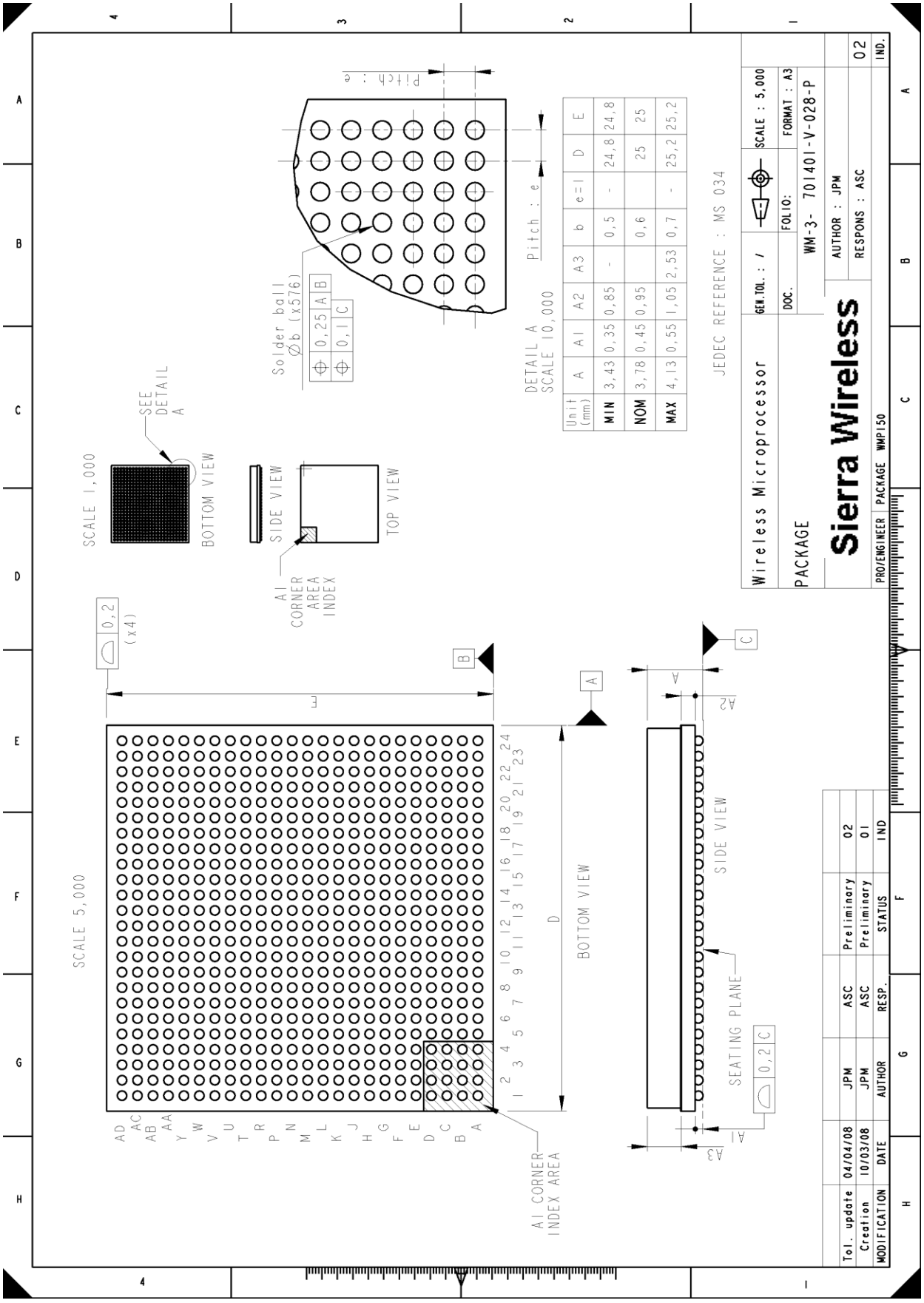


Figure 90. Mechanical Drawing of WMP100 (Top View)



Unit (mm)	A	A1	A2	A3	b	e=1	D	E
MIN	3,43	0,35	0,85	-	0,5	-	24,8	24,8
NOM	3,78	0,45	0,95		0,6		25	25
MAX	4,13	0,55	1,05	2,53	0,7	-	25,2	25,2

Figure 91. Mechanical Drawing of WMP150 (Bottom View)

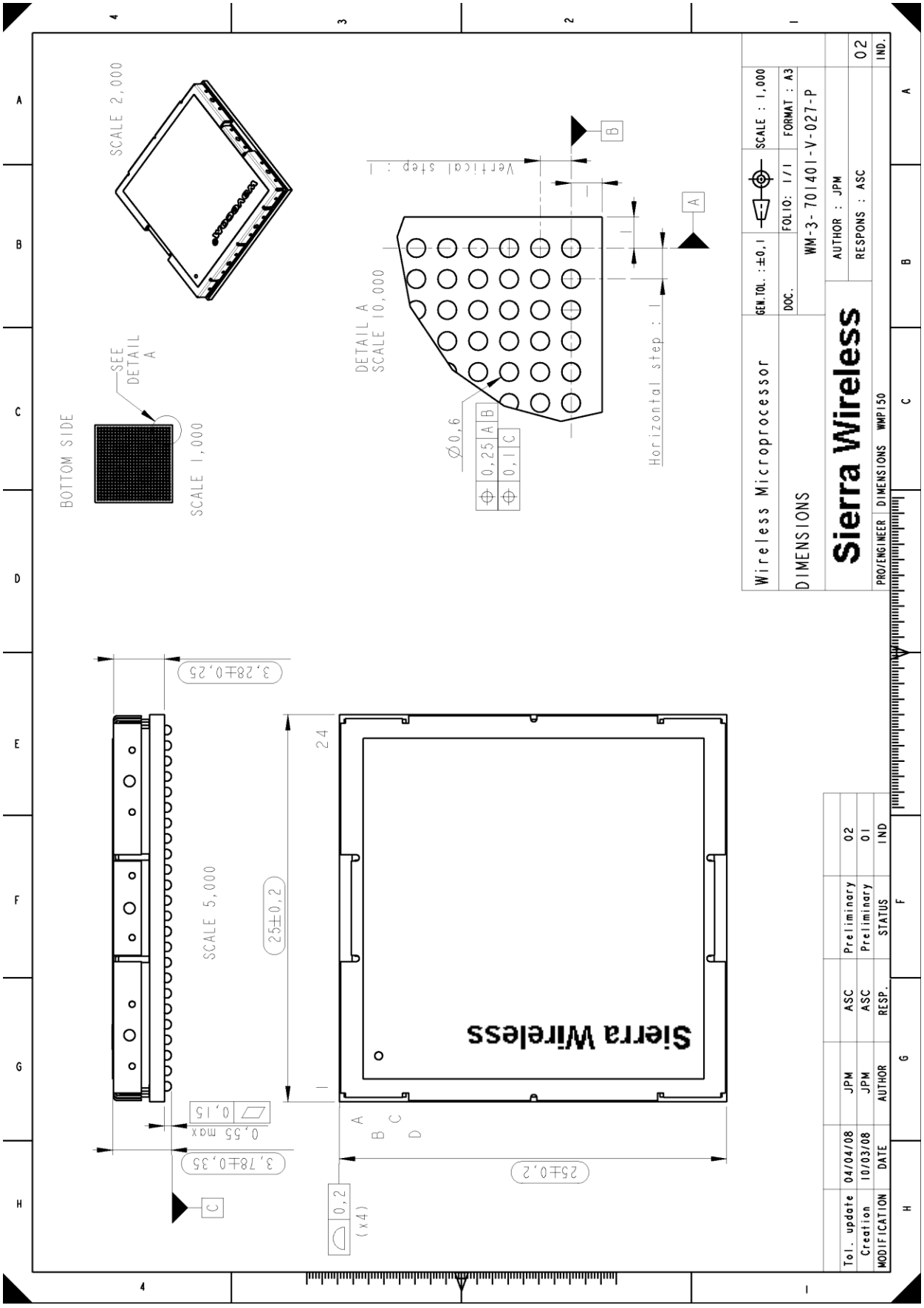


Figure 92. Mechanical Drawing of WMP150 (Top View)

5.5.3. Mechanical Constraints

Sierra Wireless recommends the customer to check on their own application if the WMP module can withstand their mechanical environment.

If needed, mechanical study should be done to reduce the warping of the mother board and the transmission of mechanical chocks. Underfill can also be envisaging.

Underfill process is described in the Manufacturing guidelines.

5.6. PCB Specifications

Due to the density of connections, the PCB stack should be 4 layers (track / distance 100 µm / 100 µm, with though-holes via Diam 0.25, pad 0.5 mm), but 6 layers may be necessary according to the functionality needed (track / distance 150 µm / 150 µm may be possible).

It is recommended to have a free-component area around the module of about 1 mm minimum, in order to facilitate the SMD assembly and rework.

5.7. Conformance with ATEX 94/9/CE Directive

To evaluate the conformity of a product using the WMP100 module with ATEX 94/9/CE directive, the integrator must take into account the following data from the WMP100 module:

- Sum of all capacitors: 78µF
- Sum of all inductors: 13µH
- Biggest single capacitor: 22µF ± 20%
- Biggest single inductor: 10µH ± 20%

6. Peripheral Devices Reference

6.1. SIM Card Reader

- ITT CANNON CCM03 series (see http://www.ittcannon.com)
- AMPHENOL C707 series (see http://www.amphenol.com)
- JAE (see http://www.jae.com)

Drawer type:

- MOLEX 99228-0002 (connector) / MOLEX 91236-0002 (holder) (see http://www.molex.com)

6.2. Microphone

Possible suppliers:

- HOSIDEN
- PANASONIC
- PEIKER

6.3. Speaker

Possible suppliers:

- SANYO
- HOSIDEN
- PRIMO
- PHILIPS

6.4. Antenna Cable

The following cable reference has been qualified for being mounted on WMP100/WMP150:

- RG178

6.5. GSM Antenna

GSM antennas and support for antenna adaptation can be obtained from manufacturers such as:

- ALLGON (http://www.allgon.com)
- IRSCHMANN (http://www.hirschmann.com/)

7. Noise and Design

7.1. EMC Recommendations

The EMC tests have to be performed as soon as possible on the application to detect any possible problem.

When designing, special attention should be paid to:

- Possible spurious emission radiated by the application to the RF receiver in the receiver band

Warning: *ESD protection is mandatory for all peripherals accessible from outside (SIM, serial link, etc.)*

- EMC protection on audio input/output (filters against 900MHz emissions)
- Biasing of the microphone inputs
- Length of the SIM interface lines (preferably <10cm)
- Ground plane: Sierra Wireless recommends having a common ground plane for analog / digital / RF grounds.
- Metallic case or plastic casing with conductive paint are recommended

Note: *The WMP modules do not include any protection against overvoltage.*

7.2. Power Supply

The power supply is one of the key issues in the design of a GSM terminal.

A weak power supply design could affect in particular:

- EMC performances.
- the emissions spectrum
- the phase error and frequency error

Warning: *Careful attention should be paid to:*

Quality of the power supply: low ripple, PFM or PSM systems should be avoided (PWM converter preferred).

Capacity to deliver high current peaks in a short time (pulsed radio emission).

8. Appendix

8.1. Template

This template may be used for consumption measurement, all modes and configurations are available. Three VBATT voltages are measured, 3.2V, 3.6V and 4.8V and the minimum/maximum RF transmission power configurations are set and measured.

Table 103. Power Consumption Template

Operating Mode	Parameter	$I_{Average}$ VBATT			I_{Peak}	Unit
ALARM Mode	-					µA
SLEEP Mode	-					mA
ACTIVE Mode	-					mA
SLEEP mode with GSM stack in Idle Mode	Paging 9/Rx burst occurrence ~2s					mA
	Paging 2/Rx burst occurrence ~0,5s					mA
ACTIVE mode with GSM stack in Idle Mode	Paging 9/Rx burst occurrence ~2s					mA
	Paging 2/Rx burst occurrence ~0,5s					mA
Peak current in GSM/GPRS Mode	850/900 MHz - PCL5 / gam.3 (TX power 33dBm) 1800/1900 MHz - PCL0 / gam.3 (TX power 30dBm)					mA
GSM Connected Mode (Voice)	850/900 MHz - PCL5 (TX power 33dBm)					mA
	850/900 MHz - PCL19 (TX power 5dBm)					mA
	1800/1900 MHz - PCL0 (TX power 30dBm)					mA
	1800/1900 MHz - PCL15 (TX power 0dBm)					mA
GPRS Transfer Mode class 10 (3Rx/2Tx)	850/900 MHz - gam.3 (TX power 33dBm)					mA
	1800/1900 MHz - gam.3 (TX power 30dBm)					mA

8.2. Standards and Recommendations

GSM ETSI, 3GPP, GCF-CC and NAPRD03 recommendations for Phase II.

Release 1999 of the 3GPP specifications references are applicable for the WMP module and can be found on the 3GPP web site http://www.3gpp.org.

Specifications used for conformance testing are the latest version of the references below.

Table 104. Applicable Standards and Requirements for the WMP Series Embedded Module

Document	Current Version	Title
GCF-CC	3.38.0	Global Certification Forum – Certification criteria
NAPRD.03	5.4	Overview of PCS Type certification review board (PTCRB) Mobile Equipment Type Certification and IMEI control
TS 51.010-1	9.2.0	3rd Generation Partnership Project; Technical Specification Group GSM/EDGE Radio Access Network; Digital cellular telecommunications system (Phase 2+); Mobile Station (MS) conformance specification; Part 1: Conformance specification
TS 51.011	9.2.0	Technical Specification Group Terminals; Specification of the Subscriber Identity Module - Mobile Equipment (SIM - ME) interface (Release 5)

The module connected to a development kit board application is certified to be in accordance with the following Rules and Regulations of the Federal Communications Commission (FCC).

Power listed on the Gant is conducted for Part 22 and conducted for Part 24.

This device contains EGSM/GPRS Class 10 functions in the 900 and 1800MHz Band, which are not operational in U.S. Territories.

This device can be used only for mobile and fixed applications. The antenna(s) used for this transmitter must be installed at a distance of minimum 20 cm from all persons and must not be co-located or operated with any other antenna or transmitter.

Caution: *Users and installers must be provided with antenna installation instructions and transmitter operating conditions for satisfying RF exposure compliance.*

Antennas used for this OEM module must not exceed 0.9 dBi gain for GSM 850 MHz and 7.1 dBi for GSM 1900 MHz for fixed operating configurations. For mobile operations the gain must not exceed 0.9 dBi for GSM 850 MHz and 3.1 dBi for GSM 1900 MHz. This device is approved as a module to be installed in other devices.

Installed in portable devices, the RF exposure condition requires a separate mandatory equipment authorization for the final device.

The license module will have an FCC ID label on the module itself. The FCC ID label must be visible through a window or it must be visible when an access panel, door or cover is easily removed.

If not, a second label must be placed on the outside of the device that contains the following text:

FCC ID: N7NWMP100

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions:

- This device may not cause harmful interference.
- This device must accept any interference received, including interference that may cause undesired operation.

The module's label will also have the CE mark with notified body number 0678. CE 0678

8.3. Safety Recommendations (for Information Only)

For the safe and efficient operation of your GSM application based on the WMP module, please read the following information carefully.

8.3.1. RF Safety

8.3.1.1. General Information

Your GSM terminal is based on the GSM standard for cellular technology. The GSM standard is spread all over the world. It covers Europe, Asia and some parts of America and Africa. This is the most used telecommunication standard.

Your GSM terminal is actually a low power radio transmitter and receiver. It sends out and receives radio frequency energy. When you use your GSM application, the cellular system which handles your calls controls both the radio frequency and the power level of your cellular modem.

8.3.1.2. Exposure to RF Energy

There has been some public concern about possible health effects of using GSM terminals. Although research on health effects from RF energy has focused on the current RF technology for many years, scientists have begun research regarding newer radio technologies, such as GSM. After existing research had been reviewed, and after compliance to all applicable safety standards had been tested, it has been concluded that the product was fitted for use.

If you are concerned about exposure to RF energy there are things you can do to minimize exposure. Obviously, limiting the duration of your calls will reduce your exposure to RF energy. In addition, you can reduce RF exposure by operating your cellular terminal efficiently by following the below guidelines.

8.3.1.3. Efficient Terminal Operation

For your GSM terminal to operate at the lowest power level, consistent with satisfactory call quality:

If your terminal has an extendible antenna, extend it fully. Some models allow you to place a call with the antenna retracted. However your GSM terminal operates more efficiently with the antenna fully extended.

Do not hold the antenna when the terminal is « IN USE ». Holding the antenna affects call quality and may cause the modem to operate at a higher power level than needed.

8.3.1.4. Antenna Care and Replacement

Do not use the GSM terminal with a damaged antenna. If a damaged antenna comes into contact with the skin, a minor burn may result. Replace a damaged antenna immediately. Consult your manual to see if you may change the antenna yourself. If so, use only a manufacturer-approved antenna. Otherwise, have your antenna repaired by a qualified technician.

Use only the supplied or approved antenna. Unauthorized antennas, modifications or attachments could damage the terminal and may contravene local RF emission regulations or invalidate type approval.

8.3.2. General Safety

8.3.2.1. Driving

Check the laws and the regulations regarding the use of cellular devices in the area where you have to drive as you always have to comply with them. When using your GSM terminal while driving, please:

- give full attention to driving,
- pull off the road and park before making or answering a call if driving conditions so require.

8.3.2.2. Electronic Devices

Most electronic equipment, for example in hospitals and motor vehicles is shielded from RF energy. However RF energy may affect some improperly shielded electronic equipment.

8.3.2.3. Vehicle Electronic Equipment

Check your vehicle manufacturer representative to determine if any on-board electronic equipment is adequately shielded from RF energy.

8.3.2.4. Medical Electronic Equipment

Consult the manufacturer of any personal medical devices (such as pacemakers, hearing aids, etc...) to determine if they are adequately shielded from external RF energy.

Turn your terminal **OFF** in health care facilities when any regulations posted in the area instruct you to do so. Hospitals or health care facilities may be using RF monitoring equipment.

8.3.2.5. Aircraft

Turn your terminal OFF before boarding any aircraft.

- Use it on the ground only with crew permission.
- Do not use it in the air.

To prevent possible interference with aircraft systems, Federal Aviation Administration (FAA) regulations require you to have permission from a crew member to use your terminal while the aircraft is on the ground. To prevent interference with cellular systems, local RF regulations prohibit using your modem while airborne.

8.3.2.6. Children

Do not allow children to play with your GSM terminal. It is not a toy. Children could hurt themselves or others (by poking themselves or others in the eye with the antenna, for example). Children could damage the modem, or make calls that increase your modem bills.

8.3.2.7. Blasting Areas

To avoid interfering with blasting operations, turn your unit OFF when in a « blasting area » or in areas posted: « turn off two-way radio ». Construction crews often use remote control RF devices to set off explosives.

Note: *This is not applicable for final products that are ATEX compliant. For final products that are ATEX compliant, the condition of use depends on specific ATEX requirements instead.*

8.3.2.8. Potentially Explosive Atmospheres

Turn your terminal **OFF** when in any area with a potentially explosive atmosphere. It is rare, but your application or its accessories could generate sparks. Sparks in such areas could cause an explosion or fire resulting in bodily injuries or even death.

Areas with a potentially explosive atmosphere are often, but not always, clearly marked. They include fuelling areas such as petrol stations; below decks on boats; fuel or chemical transfer or storage facilities; and areas where the air contains chemicals or particles, such as grain, dust, or metal powders.

Do not transport or store flammable gas, liquid, or explosives, in the compartment of your vehicle which contains your terminal or accessories.

Before using your terminal in a vehicle powered by liquefied petroleum gas (such as propane or butane) ensure that the vehicle complies with the relevant fire and safety regulations of the country in which the vehicle is to be used.

Note: *This is not applicable for final products that are ATEX compliant. For final products that are ATEX compliant, the condition of use depends on specific ATEX requirements instead.*

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