REV	DESCRIPTION	DATE	PREP	APPD
L	CO-21303	9/5/12	DF/SM	LT

EXAMPLES SHOWN IN ACTUAL SIZE

		DATE	VECTRON INTERNATIONAL MOUNT HOLLY SPRINGS, PA 17065			
PREPARED BY	Stan Carpenter	10/26/00	**Oscillator Specification, Hybrid Clock** Hi-Rel Standard			
QUALITY	SWP	11/1/00				
ENGINEERING	S. Carpenter	10/30/00	CODE IDENT NO	SIZE	DWG. NO.	REV
			00136	**A**	**OS-68338**	L
			UNSPECIFIED TOLERANCES: N/A			SHEET 1 0F 23

1. SCOPE

1.1 General. This specification defines the design, assembly and functional evaluation of high reliability, hybrid clock oscillators produced by Vectron International. Devices delivered to this specification represent the standardized Parts, Materials and Processes (PMP) Program developed, implemented and certified for advanced applications and extended environments.

1.2 Applications Overview. The designs represented by these products were primarily developed for the MIL-Aerospace community. The lesser Design Pedigrees and Screening Options imbedded within OS-68338 bridge the gap between Space and COTS hardware by providing custom hardware with measures of mechanical, assembly and reliability assurance needed for Military or Ruggedized COTS environments.

2. APPLICABLE DOCUMENTS

2.1 Specifications and Standards. The following specifications and standards form a part of this document to the extent specified herein. The issue currently in effect on the date of quotation will be the product baseline, unless otherwise specified. In the event of conflict between the texts of any references cited herein, the text of this document shall take precedence.

Military

MIL-PRF-55310	Oscillators, Crystal Controlled, General Specification For
MIL-PRF-38534	Hybrid Microcircuits, General Specification For

Standards

MIL-STD-202	Test Method Standard, Electronic and Electrical Component Parts
MIL-STD-883	Test Methods and Procedures for Microelectronics
MIL-STD-1686	Electrostatic Discharge Control Program for Protection of Electrical and Electronic Parts, Assemblies and Equipment

Other

HT-67849	Test Specification, OS-68338 Hybrids, Hi-Rel Standard
QSP-90100	Quality Systems Manual, Vectron International
VL-65339	Identification Common Documents, Materials and Processes, Hi-Rel XO
DOC203982	DPA Specification

3. GENERAL REQUIREMENTS

3.1 Classification. All devices delivered to this specification are of hybrid technology conforming to Type 1, Class 2 of MIL-PRF-55310. Primarily developed as a Class S equivalent specification, options are imbedded within it to also produce Class B, Engineering Model and Ruggedized COTS devices. Devices carry a Class 2 ESDS classification.

3.2 Item Identification. External packaging choices are of metal flatpacks, DIP's and ceramic J-lead 9x14mm and LCC's with either TTL or ACMOS logic output. Unique Model Number Series' are utilized to identify device package configurations and output logic as listed in Table 1.

3.3 Absolute Maximum Ratings.

a. Supply Voltage Range (V_{CC}):	-0.5Vdc to +7.0Vdc
b. Storage Temperature Range (T_{STG}):	-65°C to +125°C
c. Junction Temperature (T_J):	+175°C
d. Lead Temperature (soldering, 10 seconds):	+300°C
e. Output Source/Sink Current:	±70 mA

3.4 Design, Parts, Materials and Processes, Assembly, Inspection and Test.

3.4.1 Design. The ruggedized designs implemented for these devices are proven in military and space applications under extreme environments. Designs utilize 4-point crystal mounting in compliment with Established Reliability (MIL-ER) componentry. When specified, radiation hardening up to 100krad(Si) (RHA level R) can be included without altering the device's internal topography.

3.4.1.1 Design and Configuration Stability. Barring changes to improve performance by reselecting passive chip component values to offset component tolerances, there will not be fundamental changes to the design or assembly or parts, materials and processes after first product delivery of that item without written approval from the procuring activity.

3.4.1.2 Environmental Integrity. Designs have passed the environmental qualification levels of MIL-PRF-55310. These designs have also passed extended dynamic levels of at least:

Sine Vibration: MIL-STD-202, Method 204, Condition G (30g pk.)
Random Vibration: MIL-STD-202, Method 214, Condition II-J (43.92g rms)
Mechanical Shock: MIL-STD-202, Method 213, Condition F (1500g, 0.5ms)

3.4.2 Prohibited Parts, Materials and Processes. The items listed are prohibited for use in high reliability devices produced to this specification.

a. Gold metallization of package elements without a barrier metal.
b. Zinc chromate as a finish.
c. Cadmium, zinc, or pure tin external or internal to the device.
d. Plastic encapsulated semiconductor devices.
e. Ultrasonically cleaned electronic parts.
f. Heterojunction Bipolar Transistor (HBT) technology.
g. 'getter' materials

3.4.3 Assembly. Manufacturing utilizes standardized procedures, processes and verification methods to produce MIL-PRF-55310 Class S / MIL-PRF-38534 Class K equivalent devices. MIL-PRF-38534 Group B Option 1 in-line inspection is included on radiation hardened part numbers to further verify lot pedigree. Traceability of all components and production lots are

in accordance with MIL-PRF-38534, as a minimum. Tabulated records are provided as a part of the deliverable data package. Devices are handled in accordance with MIL-STD-1686 for Class 1 devices.

3.4.4 Inspection. The inspection requirements of MIL-PRF-55310 apply to all devices delivered to this document. Inspection conditions and standards are documented in accordance with the Quality Assurance, ISO-9001 and AS9100 derived, System of QSP-90100.

3.4.5 Test. The Screening test matrix of Table 5 is tailored for selectable-combination testing to eliminate costs associated with the development/maintenance of device-specific documentation packages while maintaining performance integrity.

3.4.6 Marking. Device marking shall be in accordance with the requirements of MIL-PRF-55310.

3.4.7 Ruggedized COTS Design Implementation. Design Pedigree "D" devices (see ¶ 5.2) use the same robust designs found in the other device pedigrees. They do not include the provisions of traceability or the Class-qualified componentry noted in paragraphs 3.4.3 and 4.1.

4. DETAIL REQUIREMENTS

4.1 Components

4.1.1 Crystals. Cultured quartz crystal resonators are used to provide the selected frequency for the devices. The optional use of Premium Q swept quartz can, because of its processing to remove impurities, be specified for better frequency aging characteristics. In accordance with MIL-PRF-55310, the manufacturer has a documented crystal element evaluation program.

4.1.2 Passive Components. Established Reliability (ER) failure level R minimum passive components are procured from QPL suppliers. Lot evaluations are in accordance with MIL-PRF-55310 or Enhanced Element Evaluation as specified in Table 7.

4.1.3 Class S Microcircuits. Microcircuits are procured from wafer lots that have passed MIL-PRF-55310 Lot Acceptance Tests for Class S devices. The prescribed die carries a Class 2 ESDS classification in accordance with MIL-PRF-38535. When optionally specified, further testing in accordance with MIL-PRF-55310 and MIL-PRF-38534 is performed for radiation hardness assurance and for Enhanced Element Evaluation as specified in Table 6. Those microcircuits, identified by a unique part number, are certified for 100krad(Si) total ionizing dose (TID), RHA level R (2X minimum margin). NSC, as the original 54ACT designer, rates the SEU LET at >40 MeV and SEL at >120MeV for the FACT™ family (AN-932). Vectron has conducted additional SEE testing in 2008 to verify this performance since our lot wafer testing does not include these parameters and determinations.

4.1.3.1 Class B Microcircuits. When specified, microcircuits assembled into OS-68338 Design Pedigree letters "B" and "C" devices (¶ 5.2a) are procured from wafer lots that have passed MIL-PRF-55310 element evaluations for Class B devices.

4.1.4 Packages. Packages are procured that meet the construction, lead materials and finishes as specified in MIL-PRF-55310. Package lots are upscreened in accordance with the requirements of MIL-PRF-38534 as applicable.

4.1.5 Traceability. Class S active device lots are homogenous and traceable to the manufacturer's individual wafer. Swept Quartz Crystals are traceable to the quartz bar and the processing details of the autoclave lot, as applicable. All other elements and materials are traceable to their manufacturer and incoming inspection lots.

4.1.6 Enhanced Element Evaluation. When Design Pedigree Option "E" is specified, active and passive devices with Enhanced Element Evaluation as listed in Table 6 and 7 shall be implemented for the highest reliability preference.

4.2 Mechanical.

4.2.1 Package Outline. Table 1 links each Hi-Rel Standard Model Number of this specification to a corresponding package style. Mechanical Outline information of each package style is found in the referenced Figure.

4.2.2 Thermal Characteristics. The worst case thermal characteristics of each package style are found in Table 4.

4.3 Electrical.

4.3.1 Input Power. Devices are designed for standard 5.0 volt dc operation, ±10%. Optional 3.3 Vdc (±10%) input performance for ACMOS output conditions. Current is measured, no load, at maximum rated operating voltage.

4.3.2 Temperature Range. Operating range is -55°C to +125°C.

4.3.3 Frequency Tolerance. Initial accuracy at +23°C is ±15 ppm maximum. Frequency-Temperature Stability is ±50 ppm maximum from +23°C reference. Frequency-Voltage Tolerance is ±4 ppm maximum.

4.3.4 Frequency Aging. Aging limits, and when tested in accordance with MIL-PRF-55310 Group B inspection, shall not exceed ±1.5 ppm the first 30 days, ±5 ppm Year 1 and ±2 ppm per year thereafter.

4.3.4.1 Frequency Aging Duration Option. By customer request, the Aging test may be terminated after 15 days if the measured aging rate is less than half of the specified aging rate. This is a common method of expediting 30-Day Aging without incurring risk to the hardware and used

quite successfully for numerous customers. It is based on the 'least squares fit' determinations of MIL-PRF-55310 paragraph 4.8.35. The 'half the time/half the spec' limit is generally conservative as roughly 2/3 of a unit's Aging deviation occurs within that period of time. Vectron's automated aging systems take about 6 data points per day, so a lot of data is available to do very accurate projections, much more data than what is required by MIL-PRF-55310. The delivered data would include the Aging plots projected to 30 days. If the units would not perform within that limit then they would continue to full 30 Day term. Please advise by purchase order text if this may be an acceptable option to exercise as it assists in Production Test planning.

4.3.5 Operating Characteristics. Symmetrical square wave limits are dependent on the device frequency and are in accordance with Tables 2 and 2A. Waveform measurement points and logic limits are in accordance with MIL-PRF-55310. Start-up time is 10.0 msec. maximum.

4.3.6 Output Load. Standard TTL (6 or 10) and ACMOS (10kΩ, 15pF) test loads are in accordance with MIL-PRF-55310.

5. QUALITY ASSURANCE PROVISIONS AND VERIFICATION

5.1 Verification and Test. Device lots shall be tested prior to delivery in accordance with the applicable Screening Option letter as stated by the 15th character of the part number. Table 5 tests are conducted in the order shown and annotated on the appropriate process travelers and data sheets of the governing test procedure. For devices that require Screening Options that include MIL-PRF-55310 Group A testing, the Post-Burn-In Electrical Test and the Group A Electrical Test are combined into one operation.

5.1.1 Screening Options. The Screening Options, by letter, are summarized as:

- A Modified MIL-PRF-38534 Class K
- B Modified MIL-PRF-55310 Class B Screening & Group A Quality Conformance Inspection (QCI)
- C Modified MIL-PRF-55310 Class S Screening & Group A QCI
- D Modified MIL-PRF-38534 Class K with Burn-in Delta Aging
- E Modified MIL-PRF-55310 Class B Screening, Groups A & B QCI
- F Modified MIL-PRF-55310 Class S Screening, Groups A & B QCI
- G Modified MIL-PRF-55310 Class B Screening & Post Burn-in Nominal Electricals
- X Engineering Model (EM)

5.2 Optional Design, Test and Data Parameters. The following is a list of design, assembly, inspection and test options that can be selected or added by purchase order request.

a. Design Pedigree (choose one as the 5th character in the part number):

(E) Enhanced Element Evaluation, 100krad Class S die, Premium Q Swept Quartz
(R) Hi-Rel design w/ 100krad Class S die, Premium Q Swept Quartz
(V) Hi-Rel design w/ 100krad Class S die, Cultured Quartz

(X) Hi-Rel design w/ Cultured Quartz, Class S die
(B) Hi-Rel design w/ Swept Quartz, Class B die
(C) Hi-Rel design w/ Cultured Quartz, Class B die
(D) Hi-Rel design w/ Cultured Quartz and commercial grade components

b. Input Voltage, **(A)** for 5.0V, **(B)** for 3.3V as the 14th character
c. Frequency-Temperature Slew Test
d. Radiographic Inspection
e. Group C Inspection: MIL-PRF-55310 (requires 8 pc. sample)
f. Group C Inspection: MIL-PRF-38534 (requires 8 pc. sample – 5 pc. Life, 3 pc. RGA)
g. Internal Water-Vapor Content (RGA) samples and test performance
h. MTBF Reliability Calculations
i. Worst Case/Derating Analysis: MIL-HDBK-1547 with Tj Max = +105°C; Derated Maximum Operating Temp = Tj Max - ΔTj
j. Deliverable Process Identification Documentation (PID)
k. Customer Source Inspection (pre-cap / final)
l. Destruct Physical Analysis (DPA): MIL-STD-1580 with exceptions as specified in Vectron DOC203982.

5.3 Test Conditions. Unless otherwise stated herein, inspections are performed in accordance with those specified in MIL-PRF-55310 and MIL-PRF-38534, in that order. Process travelers identify the applicable methods, conditions and procedures to be used. Examples of electrical test procedures that correspond to MIL-PRF-55310 requirements are shown in Table 3.

5.4 Special Tests and Descriptions.

5.4.1 Frequency-Temperature Slew. Frequency-Temperature Slew Test has been developed as an indicator of higher than normal internal water vapor content. The incremental temperature sweep from +125°C to -55°C and back to +125°C records output frequency fluctuations emulating the mass loading of moisture deposited on the crystal blank surface. Though not replacing a customer's internal water-vapor content (RGA) requirement, confidence is increased without destructively testing otherwise good devices.

5.4.2 Burn-in Delta Frequency Aging (in Option D). The frequency measurement for burn-in delta measurements is performed at the crystal's upper turning point temperature where its effects on repeatable frequency accuracy are maximized. Dependent on the crystal specified, this temperature is typically between +65°C and +85°C, ±0.2°C.

5.5 Deliverable Data. The manufacturer supplies the following data, as a minimum, with each lot of devices:

a. Completed assembly and screening lot travelers, including rework history.
b. Electrical test variables data, identified by unique serial number.
c. Frequency-Temperature Slew plots, Radiographic films, Group C data and RGA data as required by purchase order.

5.6 Discrepant Material. All MRB authority resides with the procuring activity.

5.7 Failure Analysis. Any catastrophic failure (no clocking, no current) at Post Burn-In or after will be evaluated for root cause. The customer will be notified after occurrence and upon completion of the evaluation.

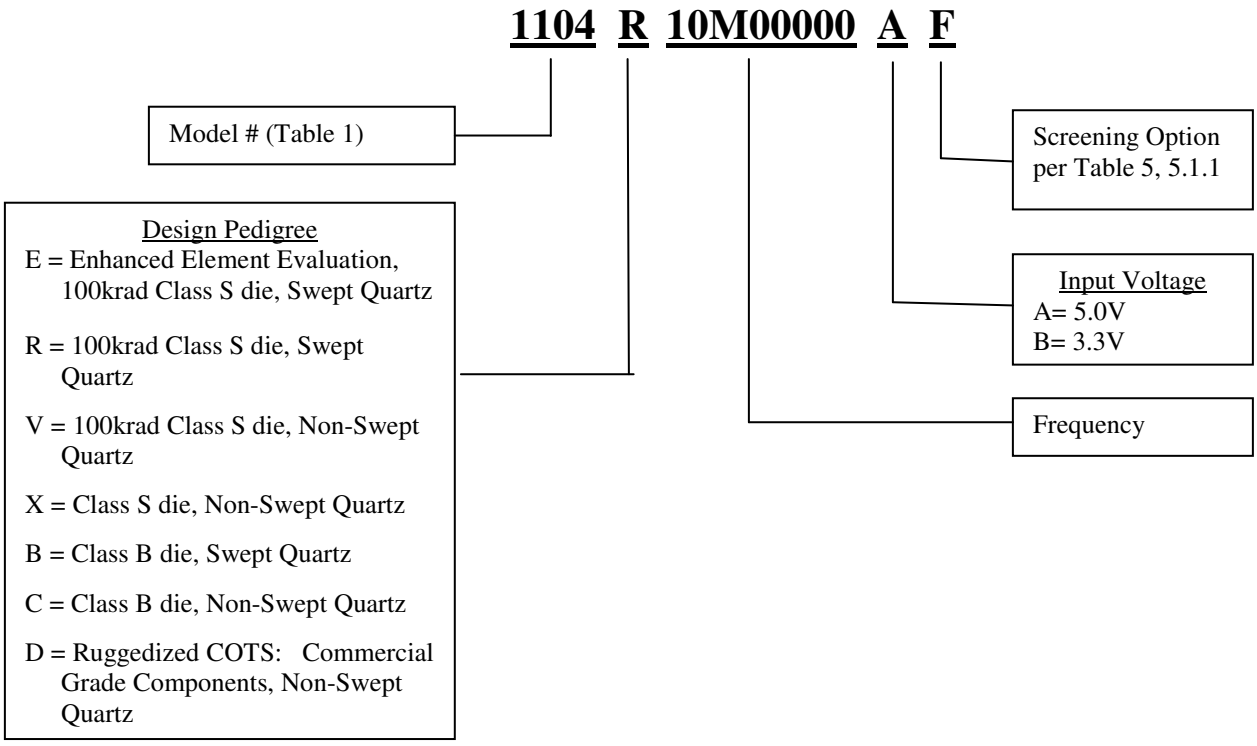
6. PREPARATION FOR DELIVERY

6.1 Packaging. Devices will be packaged in a manner that prevents handling and transit damage during shipping. Devices will be handled in accordance with MIL-STD-1686 for Class 1 devices.

7. ORDERING INFORMATION

7.1 Ordering Part Number. The ordering part number is made up of an alphanumeric series of 15 characters. Design-affected product options, identified by the parenthetic letter on the Optional Parameters list (¶ 5.2a and b), are included within the device part number.

The Part Number breakdown is described as:



7.1.1 Model Number. The device model number is the four (4) digit number assigned to a corresponding package and output combination per Table 1.

7.1.2 Design Pedigree. Class S variants correspond to either letter “E”, “R”, “V” or “X” and are described in paragraph 5.2a. Class B variants correspond to either letter “B” or “C” and are described in paragraph 5.2a. Ruggedized COTS, using commercial grade components, corresponds to letter “D”.

7.1.2.1 Input Voltage. Voltage is the 14th character, letters “A” representing 5.0V and “B” for 3.3V.

7.1.3 Output Frequency. The nominal output frequency is expressed in the format as specified in MIL-PRF-55310 utilizing eight (8) characters.

7.1.4 Screening Options. The 15th character is the Screening Option (letter A thru G or X) selected from Table 5.

7.2 Optional Design, Test and Data Parameters. Test and documentation requirements above that of the standard high reliability model shall be specified by separate purchase order line items (as listed in ¶ 5.2c thru k).

HI-REL STANDARD MODEL #	PACKAGE	OUTPUT, Square Wave	PIN I/O 1/				MECHANICAL OUTLINE
			Vcc	Out	Gnd/ Case	E/D 3/	
1101	12 Lead Flatpack	ACMOS	12	7	6	na	FIGURE 1
1102	14 Lead Flatpack	ACMOS	14	8	7	na	FIGURE 2
1103	16 Lead Flatpack	ACMOS	8	10	9	na	FIGURE 3
1104	20 Lead Flatpack	ACMOS	13, 20	11	10	na	FIGURE 6
1105	14 Pin DIP	ACMOS	14	8	7	na	FIGURE 7
1115	4 pin ½ DIP	ACMOS	8	5	4	na	FIGURE 5
1116	J-lead SMT	ACMOS	4	3	2	1	FIGURE 8
1118 2/	4 pad 5 x 7mm	ACMOS	4	3	2	1	FIGURE 9
1107	12 Lead Flatpack	TTL	12	7	6	na	FIGURE 1
1108	14 Lead Flatpack	TTL	14	8	7	na	FIGURE 2
1109	16 Lead Flatpack	TTL	8	10	9	na	FIGURE 3
1110	20 Lead Flatpack	TTL	13, 20	11	10	na	FIGURE 6
1111	14 Pin DIP	TTL	14	8	7	na	FIGURE 7
1117	J-lead SMT	TTL	4	3	2	1	FIGURE 8

1/. All unassigned pins have no internal connections or ties.
2/. See Appendix A.
3/. A logic "1" (>+2.0V) or open on pin 1 will enable the output. A logic "0" (<+0.8V) will disable the output.

TABLE 1 - Item Identification and Package Outline

Frequency Range @ 5V Operation: 0.35 MHz to 100.0 MHz 1/					
Frequency Range @ 3.3V Operation: 0.35 MHz to 100.0 MHz					
Temperature Range: -55°C to +125°C					
Frequency Tolerance, Initial Accuracy @ +23°C: ±15 ppm max.					
Frequency-Temperature Stability from +23°C ref.: ±50 ppm max.					
Frequency-Voltage Tolerance: ±4 ppm max. (Vcc ±10%)					
Frequency Aging: ±1.5 ppm max. 1st 30 days, ±5 ppm max. Year 1, ±2 ppm max. Year 2+					
Start-up Time: 10.0 ms max.					
Frequency Range (MHz)	Current (mA) (max. no load) 5.5V	3.63V	Rise / Fall Times (ns max.)	Duty Cycle (%)	Fan-out (if TTL) 3/
0.35 - 4.0	10	6	6	45 to 55	10
4.0 – 12.0	15	8	5	45 to 55	10
>12.0 – 24.0	15	10	5	40 to 60	10
>24.0 – 40.0	20	15	5	40 to 60	6
>40.0 – 65.0	35	20	5	40 to 60	6
>65.0 – 85.0	45	25	3	40 to 60	6
>85.0 – 100	55	30	3	40 to 60	6

1/. Exception: Frequency Range @ 5V Operation for model 1117 (TTL) series is limited to 85 MHz.

2/. Waveform measurement points and logic limits are in accordance with MIL-PRF-55310.

3/. For +3.3V TTL option, R_L=160Ω for 10 TTL loads and R_L=270Ω for 6 TTL loads.

TABLE 2 - Electrical Performance Characteristics

OPERATION LISTING	REQUIREMENTS AND CONDITIONS	VECTRON TEST PROCEDURE
@ all Electrical tests		
Input Current (no load)	MIL-PRF-55310, Para 4.8.5.1	GR-51681
Initial Accuracy @ Ref. Temp.	MIL-PRF-55310, Para 4.8.6	GR-51596
Output Logic Voltage Levels	MIL-PRF-55310, Para 4.8.21.3	GR-51597
Rise and Fall Times	MIL-PRF-55310, Para 4.8.22	GR-51599
Duty Cycle	MIL-PRF-55310, Para 4.8.23	GR-51601
@ Post Burn-In Electrical only		
Overvoltage Survivability	MIL-PRF-55310, Para 4.8.4	GR-37269
Initial Freq. – Temp. Accuracy	MIL-PRF-55310, Para 4.8.10.1	GR-51602
Freq. – Voltage Tolerance	MIL-PRF-55310, Para 4.8.14	GR-51602
Start-up Time (fast/slow start)	MIL-PRF-55310, Para 4.8.29	GR-61352

TABLE 3 - Electrical Test Parameters

Model #	Typical Thermal Resistance Junction to Case θ_{jc} (°C / W)	Δ Junction Temp. T_j (°C @ max. Icc)	Typical Weight (Grams)
1101 / 1107	17.32	5.24	3.0
1102 / 1108	17.32	5.24	3.3
1103 / 1109	17.20	5.20	1.4
1104 / 1110	16.97	5.13	2.9
1105 / 1111	19.57	5.92	3.9
1115	20.22	6.12	2.2
1116 / 1117	17.91	5.42	1.2
1118	3.77	1.14	0.2

Maximum operating power = 302.5 mW per Table 2.

TABLE 4 - Typical Thermal Characteristics and Weight

	Vcc=+5.0V		Vcc=+3.3V	
Frequency	1 sigma (ps)	pk-pk (ps)	1 sigma (ps)	pk-pk (ps)
1 MHz	8.5	60	20	150
40 MHz	5	40	8	70
80 MHz	5	40	6	45

TABLE 4a – Typical Jitter Performance

OPN. NO.	OPERATION LISTING	REQUIREMENTS AND CONDITIONS	Option A	Option B	Option C	Option D	Option E	Option F	Option G	Option X
	SCREENING	MIL Class Similarity	K 100%	B- 100%	S- 100%	K+ 100%	B 100%	S 100%	 100%	EM 100%
1	Non-Destruct Bond Pull 9/	MIL-STD-883, Meth 2023	Completed During Assembly							
2	Internal Visual	MIL-STD-883, Meth 2017 Class K, Meth 2032 Class K								
3	Stabilization (Vacuum) Bake	MIL-STD-883, Meth 1008, Cond C, 150°C, 48 hours min.								
4	Thermal Shock	MIL-STD-883, Meth 1011, Cond A	NR	NR	X	NR	NR	X	NR	NR
5	Temperature Cycle	MIL-STD-883, Meth 1010, Cond. B, 10 cycles min.	X	X	X	X	X	X	X	NR
6	Constant Acceleration	MIL-STD-883, Meth 2001, Cond A, Y1 plane only, 5000 g's	X	X	X	X	X	X	X	NR
7	Particle Impact Noise Detection	MIL-STD-883, Meth 2020, Cond B	X	X	X	X	X	X	NR	X
8	Electrical Testing, Pre Burn-In	Perform tests in Table 3. Nominal Vcc, nominal temperature	X	X	X	X, 3/	X	X	X	X
9	Freq-Temp Slew Test	Operating temp. range, frequency plotted at 1.0°C steps	AR	AR	AR	AR	AR	AR	NR	NR
10	1st Burn-In	MIL-STD-883, Meth 1015, Condition B	X 160 hrs.	X 160 hrs.	X 240 hrs.	X 160 hrs.	X 160 hrs.	X 240 hrs.	X 160 hrs.	NR
11	Electrical Testing, Intermediate	Perform tests in Table 3. Nominal Vcc, nominal temperature	X	NR	NR	X, 4/	NR	NR	NR	NR
12	2nd Burn-In	MIL-STD-883, Meth 1015, Condition B	X 160 hrs.	NR	NR	X 160 hrs.	NR	NR	NR	NR
13	Electrical Testing, Post Burn-In (Group A)	Perform tests in Table 3. Nominal Vcc & extremes, nominal temperature & extremes	X	X	X	X, 5/	X	X	X nom. Vcc	NR
14	Seal: Fine Leak	MIL-STD-883, Meth 1014, Cond A2 5 x 10^{-8} atm cc/sec max	X	X	X	X	X	X	X	X
15	Seal: Gross Leak	MIL-STD-202, Meth 112, Cond D	X	X	X	X	X	X	X	X
16	Radiographic Inspection	MIL-STD-883, Meth 2012	X	AR	AR	X	AR	X	NR	NR
17	Solderability	MIL-STD-883, Meth 2003	6/	6/	6/	6/	6/	6/	6/	NR
18	External Visual & Mechanical	MIL-STD-883, Meth 2009	X 7/	X 7/	X 7/	X 7/	X 7/	X 7/	X 7/	X 7/
19	Aging, 30 Day 8/ (M55310 Group B)	MIL-PRF-55310, para. 4.8.35.1	NR	NR	NR	NR	13 pcs.	X	NR	NR

LEGEND: X = Required, NR = Not Required, AR = As Required

TABLE 5 - Test Matrix

3/ includes frequency recorded at the crystal Upper Turning Point (UTP) temperature. 4/ Δ_F @ UTP = ± 7.5 ppm maximum.
5/ Δ_F @ UTP = ± 2.5 ppm maximum. 6/ Performed at package LAT. Include LAT data sheet
7/ When specified, RGA samples will be removed from the lot after completion of this operation. Use of Screening failures require customer concurrence.
8/ By customer request, the Aging test may be terminated after 15 days if the measured aging rate is less than one-half the specified aging rate, as described in paragraph 4.3.4.1 herein. See the customer PO. 9/. Not performed on Option B, E and X units.

Subgroup	Class	Test	Mil-STD-883		Quantity	Mil-PRF-38534 Reference
	K		Method	Condition	(accept number)	Paragraph
1	X	Element Electrical A. May perform at wafer level B. All failures shall be removed from the lot C. Perform at room ambient			100%	C.3.3.1
2	X	Element Visual	2010		100%	C.3.3.2
3	X	Internal Visual	2010		10(0) or 22(0)	C.3.3.3 C.3.3.4.2
4	X	Temperature Cycling	1010	C	10(0) 22(0)	C.3.3.3
	X	Mechanical Shock or Constant Acceleration	2002 2001	B, Y1 direction 3,000 G, Y1 direction		
	X	Interim Electrical				C.3.3.4.3
	X	Burn-In	1015	240 hours minimum at +125°C		
	X	Post Burn-In Electrical				C.3.3.4.3
	X	Steady State Life	1005			
	X	Final Electrical				C.3.3.4.3
5	X	Wire Bond Evaluation	2011		10(0) wires or 20(1) wires	C.3.3.3 C.3.3.5
6	X	SEM	2018		See method 2018	C.3.3.6

Notes:
Subgroups 3, 4, & 5 shall be performed on a sample of 10 die if the wafer lot is from a QPL/QML line. If the die are from commercial wafer lots, then the sample size shall be 22 die.

TABLE 6 - MICROCIRCUIT ENHANCED ELEMENT EVALUATION

Parts Type	Test	Requirement Paragraph	Sample size	Allowable Reject(s)
Ceramic Capacitors				
M55681 FRL S or M123 (chips)	N/A	N/A	N/A	N/A
Resistors				
M55342 FRL R or S	N/A	N/A	N/A	N/A
Inductors				
Custom	Group A	Mil-Std-981	Mil-Std-981	Mil-Std-981
	Group B	Mil-Std-981	Mil-Std-981	Mil-Std-981

TABLE 7: PASSIVE COMPONENT ENHANCED ELEMENT EVALUATION

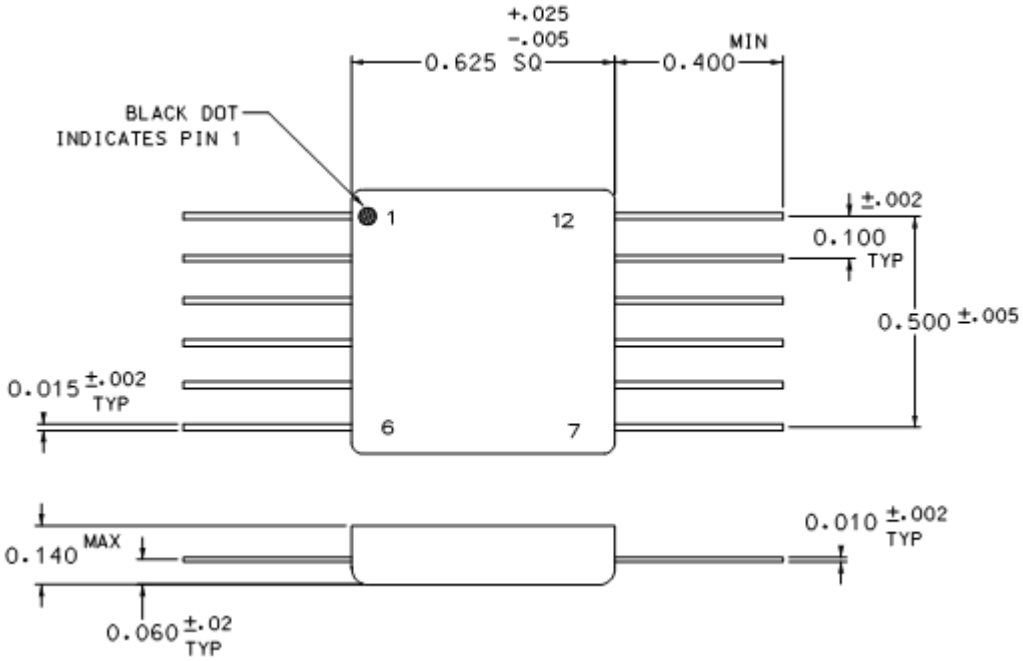


FIGURE 1
Models 1101 & 1107 Package Outline

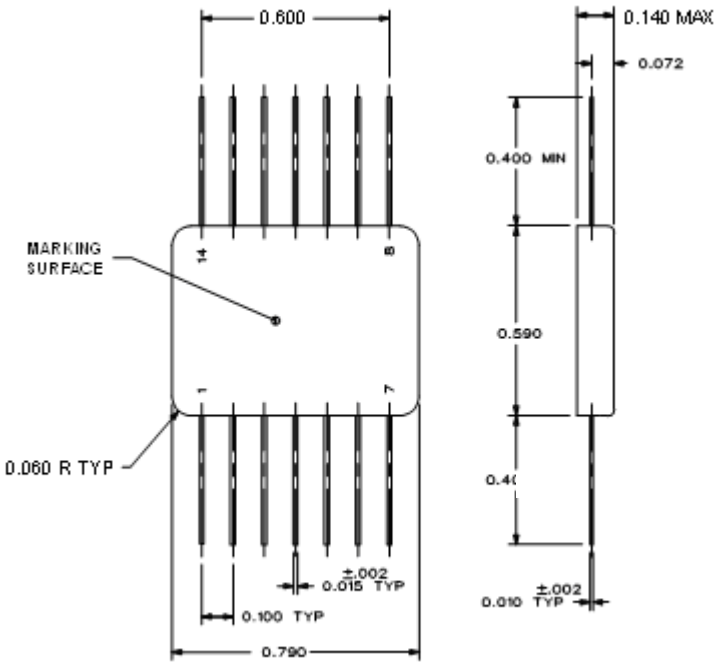


FIGURE 2
Models 1102 & 1108 Package Outline
Tolerances: Unspecified = ±0.010”

SIZE	CODE IDENT NO.	THIRD ANGLE PROJECTION	UNSPECIFIED TOLERANCES	DWG NO.	REV.	SHEET
A	**00136**		**N/A**	**OS-68338**	**L**	**15**

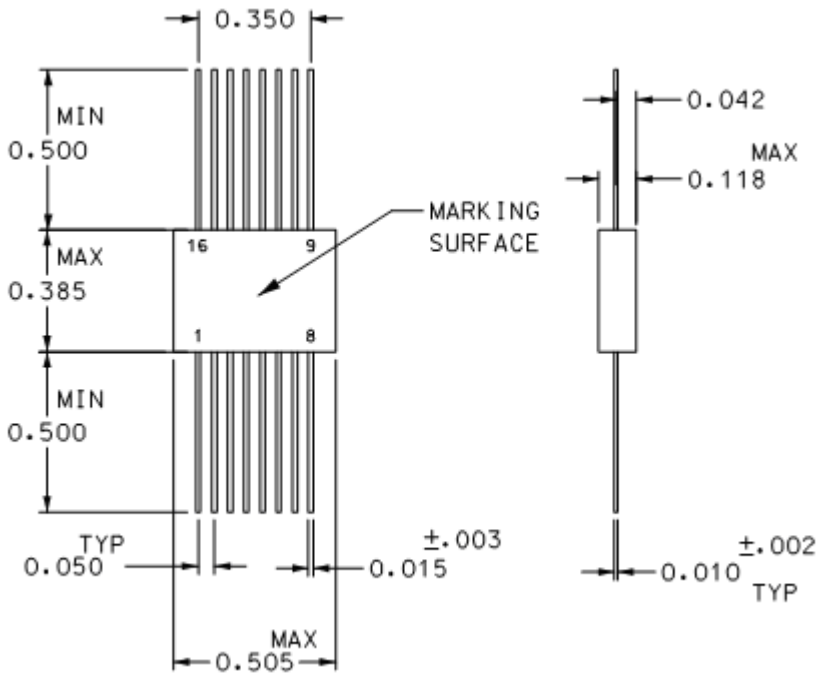


FIGURE 3
Models 1103 & 1109 Package Outline

Deleted Models 1106/1112 and 1113/1114

FIGURE 4
Models 1106 & 1112 Package Outline
Models 1113 & 1114 - same package minus the leads

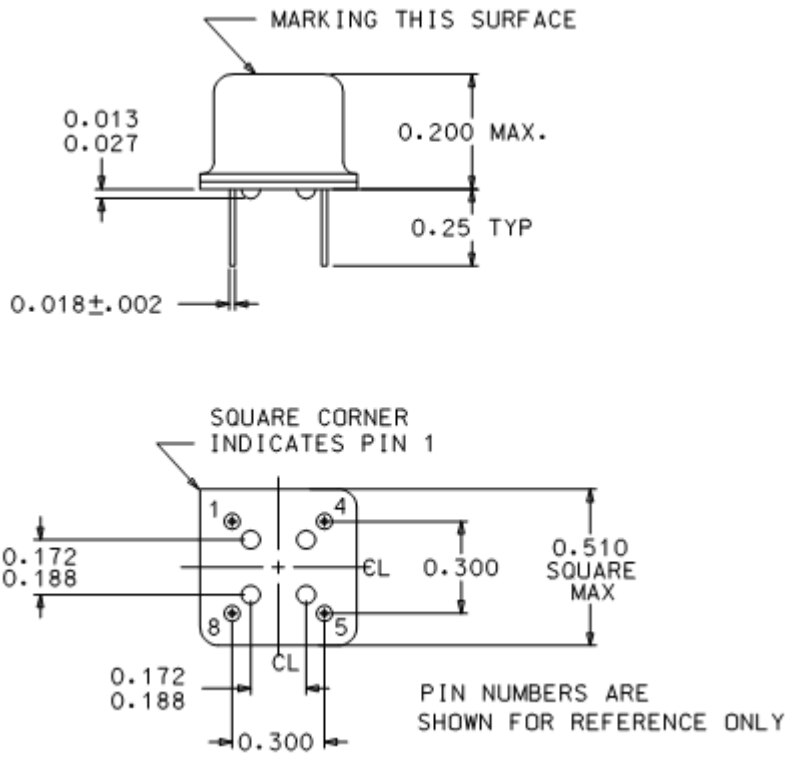


FIGURE 5
Model 1115 Package Outline

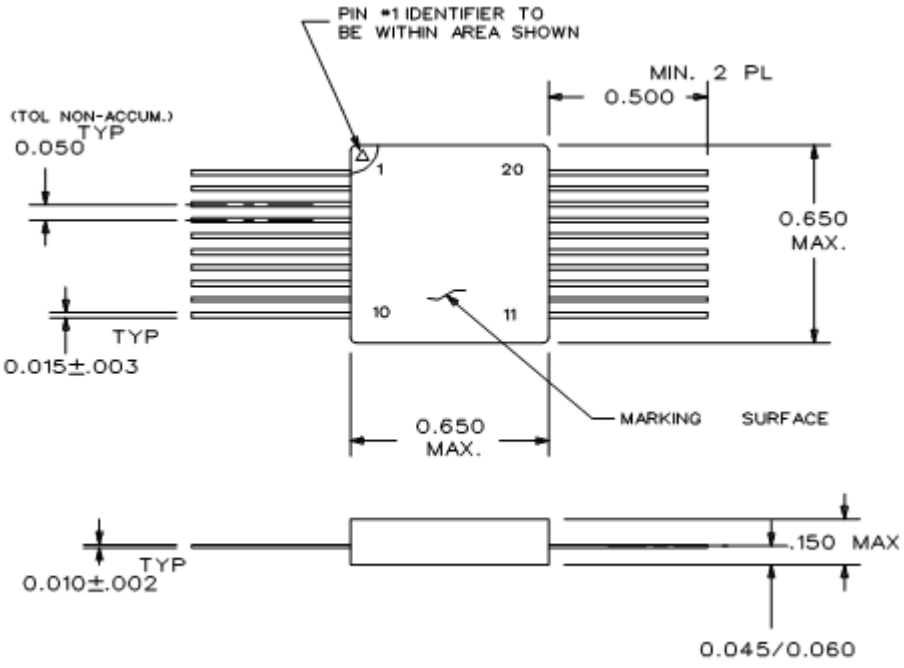


FIGURE 6
Model 1104 & 1110 Package Outline

SIZE	CODE IDENT NO.	THIRD ANGLE PROJECTION	UNSPECIFIED TOLERANCES	DWG NO.	REV.	SHEET
A	**00136**		**N/A**	**OS-68338**	**L**	**17**

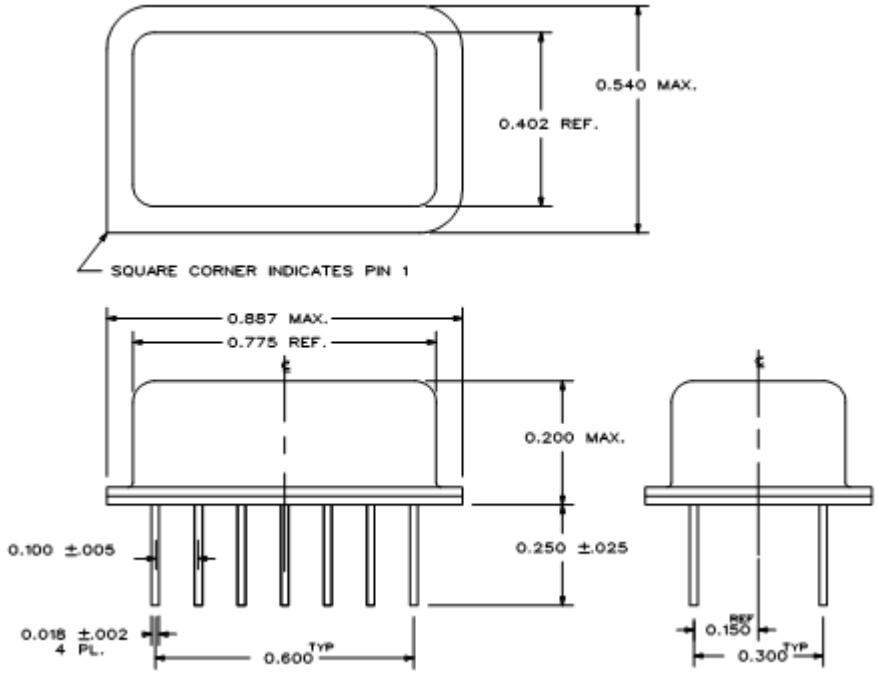


FIGURE 7
Model 1105 & 1111 Package Outline

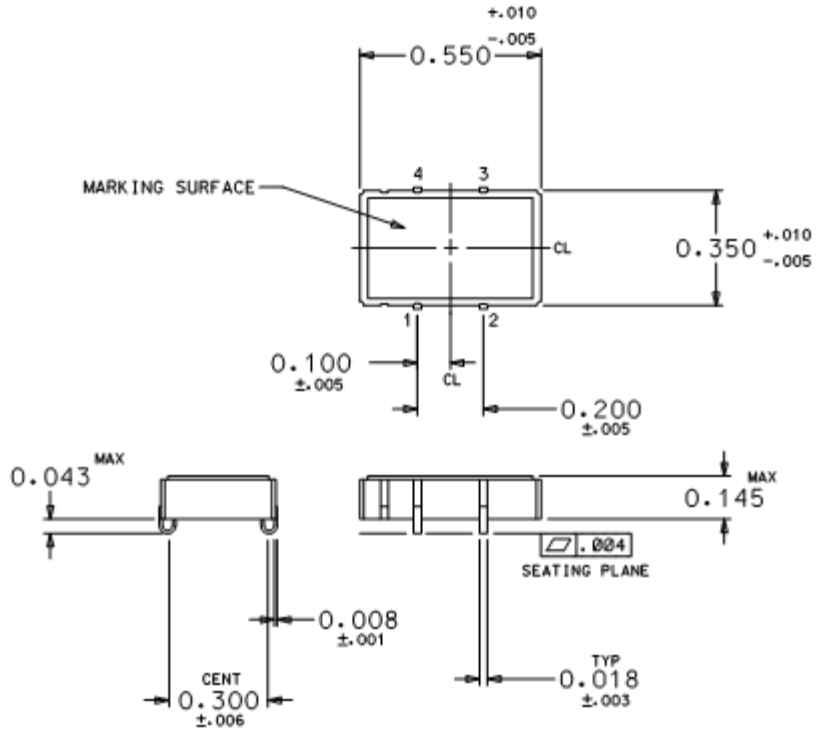


FIGURE 8
Model 1116 & 1117 Package Outline

SIZE	CODE IDENT NO.	THIRD ANGLE PROJECTION	UNSPECIFIED TOLERANCES	DWG NO.	REV.	SHEET
A	**00136**		**N/A**	**OS-68338**	**L**	**18**

APPENDIX A

4 Pad 5 x 7mm ACMOS Hybrid, Model Number 1118 Series

A.1 Scope. The Model 1118 Series uses a fundamentally different design approach versus the other models offered by the OS-68338 Specification. Some of that text does not fit this design, so for that reason the Model 1118 Series is specified here in Appendix A. Where not superseded by this Appendix the original text still applies.

A.2 Design. The Model 1118 Series uses an AT-strip crystal mounted at two adjacent points. Due to the crystal's smaller mass this 2-point design has proven its ruggedness by passing the same environmental qualification exposures of the other OS-68338 Models (¶ 3.4.1.2).

Frequency Range Operation: 0.7 MHz to 70 MHz					
Temperature Range: -55°C to +125°C					
Frequency Tolerance, Initial Accuracy @ +23°C: ±15 ppm max.					
Frequency-Temperature Stability from +23°C ref.: ±75 ppm max.					
Frequency-Voltage Tolerance: ±4 ppm max. (Vcc ±10%)					
Frequency Aging: ±1.5 ppm 1st 30 days, ±5 ppm max. Year 1, ±2 ppm max. Year 2+					
Start-up Time: 10.0 ms max.					
Frequency Range (MHz)	Current (mA) (max. no load) 5.5V	3.63V	Rise / Fall Times (ns max.)	Duty Cycle (%)	
0.7 - 4.0	10	6	6	45 to 55	
4.0 – 12.0	15	8	5	45 to 55	
>12.0 – 24.0	15	10	5	45 to 55	
>24.0 – 40.0	20	15	5	40 to 60	
>40.0 – 70.0	35	20	5	40 to 60	

Note: Waveform measurement points and logic limits are in accordance with MIL-PRF-55310.

TABLE 2A - Electrical Performance Characteristics, Model 1118 Series

A.3 Marking. Device marking, due to size, will be limited to the Vectron logo (VI), date code, Pin 1 / ESD ID and the fully traceable Work Order – unique serial number combination, i.e. 370002-20. Individual device packaging will include the full part number.

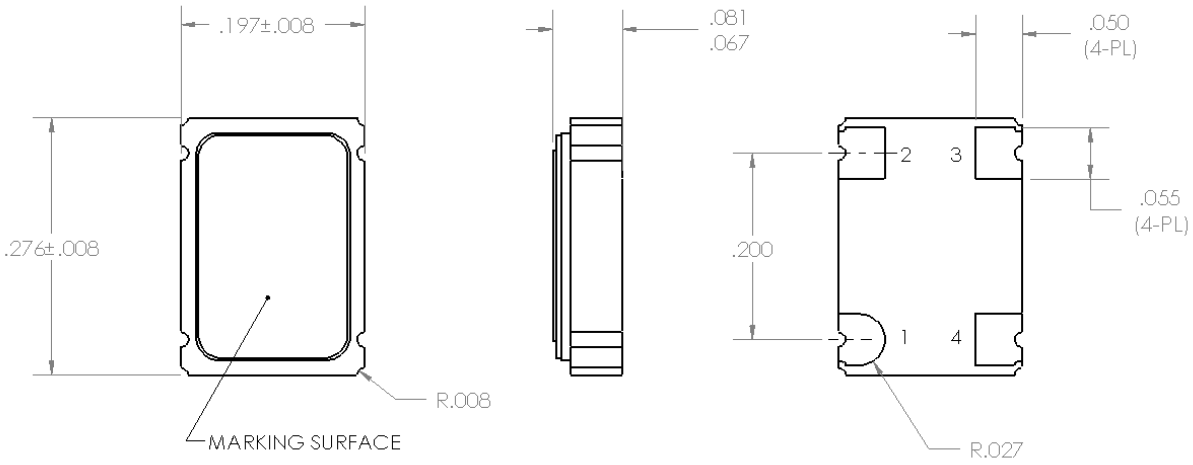


FIGURE 9
Model 1118 Package Outline

DOCUMENT CHANGE RECORD

Revision	Change
F	**ECO 04-2126** Add Application Overview: ¶ 1.2 Add new para. for Ruggedized COTS: ¶ 3.4.7 Add Design Pedigree 'D': ¶ 5.2, 7.1 Add references to Ruggedized COTS: ¶ 3.1, 7.1.2 Add Screening Option 'G': ¶ 5.1.1, 7.1.4 Table 1: change all HCMOS or ACMOS, replace MIL package references with applicable added Figures Table 4: add Screening Options 'G' and 'EM' Add Figures 6 thru 8
G	**ECO 05-0727** Add ¶ 3.4.1.2 Environmental Integrity ¶ 4.1.3: add SEU / SEL statement ¶ 4.3.1: change 3.3Vdc tolerance from ±5% to ±10% ¶ 4.3.4: revised Aging from ±5 ppm / year max. to ±5 ppm max. Year 1, ±2 ppm max. Year 2+ ¶ 5.2: add (V) Hi-Rel design w/ 100krad Class S die, Cultured Quartz ¶ 7.1 Design Pedigree: add V=100krad Class S die, Cultured Quartz Table 1: add 1118 Model Number info Table 2, Current column: split into 5.5V and 3.6V columns and revised limits downward Table 2, Rise/Fall Times column: revise limits downward for ≤12 MHz and >65.0 to 80 MHz ranges Add new Table 4 Thermal Characteristics, renumber Test Matrix to Table 5 Table 5 Test Matrix, Option X column: correct Opn. No. 5, 6 and 17 from "X" to "N/R" Add Appendix A for 5 x 7 requirements
H	**ECO 06-2510** ¶ 2.1: add VL-65339 Add ¶ 3.3e, Output Source/Sink Current Add ¶ 3.4.2g, 'getter' materials Add ¶ 4.3.4.1 Frequency Aging Duration Option ¶ 5.1.1: S/O 'G', clarify description ¶ 5.2e & 5.2f: clarify Group C sample sizes Table 1: 1106 & 1112 package name to 20 Lead Ceramic Table 2: add Frequency Ranges of both voltages; >65.0MHz – 85.0; >85.0 -100, 'n/a' under 3.63V column Table 5: add Note 8 Figure 2: add Unspecified Tolerance dimension
I	**ECO 07-0692** • Table 5: Corrected Operation 2 reference to "Cond. K". • Table 5: Changed Table 5 OPN 10 and 12 to note Method 1015 Condition B. • Added new sentence to end of Par 5.1 describing that Post BI and Group A are combined into one electrical test. • Added "n/a" to Table 2 for the 85.00-100.00 "Fan-out" column. • Removed photo from cover page (to reduce file size).

J	**ECO 08-0145** Paragraph 4.1.5: added "Class S" & "SWEPT Quartz" Table 2: replaced "n/a" with "30", at row “85.00-100.00”, column “3.63 V” Figure 3: changed ".057" to ".042", the dimension at back-to-leads
K	**CO-14428** Sheet1: Inserted picture on cover sheet. ¶ 4.1.2: Added “minimum” and “Lot evaluations are in accordance with MIL-PRF-55310 or Enhanced Element Evaluation as specified in Table 7.” ¶ 4.1.3: Added “and for Enhanced Element Evaluation as specified in Table 6.” Added: “Vectron has conducted additional SEE testing in 2008 to verify this performance since our lot wafer testing does not include these parameters and determinations.” ¶ 4.1.6: Added new paragraph. ¶ 4.3.4: Added “When screening Option F is selected, aging is… compliance to the aging limit.” ¶ 5.1.1: Added “Modified” to options F and G. ¶ 5.2, 7.1 and 7.1.2: Added Option (E) for Enhanced Element Evaluation Table 1: Added Footnote 2 for Model 1118 Table 2: Added Footnote 1 Changed Frequency Range Maximum @ 3.3V Operation from “85.0 MHz” to “100.0 MHz” Table 5: Added Footnote 9 for Option F. “PDA is not applicable” Tables 6 and 7: New Figures 3, 6 and 9: Redrawn ¶ A.3: Deleted. Renumbered paragraphs. Table 2A: Added “Frequency Range: 0.7 MHz to 54 MHz” Changed Duty Cycle at >12.0-24.0 From “40 to 60” To “45 to 55”

L	**CO-21303** Sheet 1: Revised picture on cover sheet to delete 1106/1113 and 1112/1114 and added 1118. Added "EXAMPLES SHOWN IN ACTUAL SIZE" ¶ 2.1: Added "DOC203982 DPA Specification" ¶ 3.4.4: Added "and AS9100" ¶ 4.3.4: Changed maximum 30 day aging limit from ±1.0 ppm to ±1.5 ppm. ¶ 4.3.4: Deleted "When screening Option F is… to the aging limit" ¶ 5.2.i: Added "MIL-HDBK-1547 with Tj Max = +105°C; Derated Maximum Operating Temp = Tj Max - ΔTj" ¶ 5.2: Added option item "l" to the list. ¶ 7.1: Added "non-swept" to descriptions ¶ 7.1.4 Corrected error. From Table 4 to Table 5 Table 1: Added Note 3 Table 1: Deleted Models 1106, 1113, 1112 and 1114 Table 2: Changed maximum 30 day aging limit from ±1.0 ppm to ±1.5 ppm. Table 2: Added Note 3 Table 4: Added Typical Weight information. Table 4: Deleted Models 1106, 1113, 1112 and 1114 Added Table 4a "Typical Jitter Performance". Table 5: Replaced note 9 with "Not performed on Option B, E and X units" and moved note "9/" from op. 19 to op. 1. Figure 4: Deleted Models 1106, 1113, 1112 and 1114 Table 2A: Changed maximum frequency range from 54Mhz to 70MHz Table 2A: Deleted "2./" Table 2A: Changed maximum 30 day aging limit from ±1.0 ppm to ±1.5 ppm.