Product Specification

Product Name: VGM128064B0B02

Product Code: M00482

Customer
Approved by Customer
Approved Date:

Designed By	Checked By	Approved By	
		R&D	QA
2011.3.10	2011.3.10	2011.3.10	2011.3.10

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REVISION RECORD

REV.	REVISION DESCRIPTION	REV. DATE	REMARK
A01	Initial release.	2011.3.8	

1 Overview

VGM128064B0B02 is a monochrome OLED display module with 128×64 dot matrix. The characteristics of this display module are high brightness, self-emission, high contrast ratio, slim/thin outline, wide viewing angle, wide temperature range, and low power consumption.

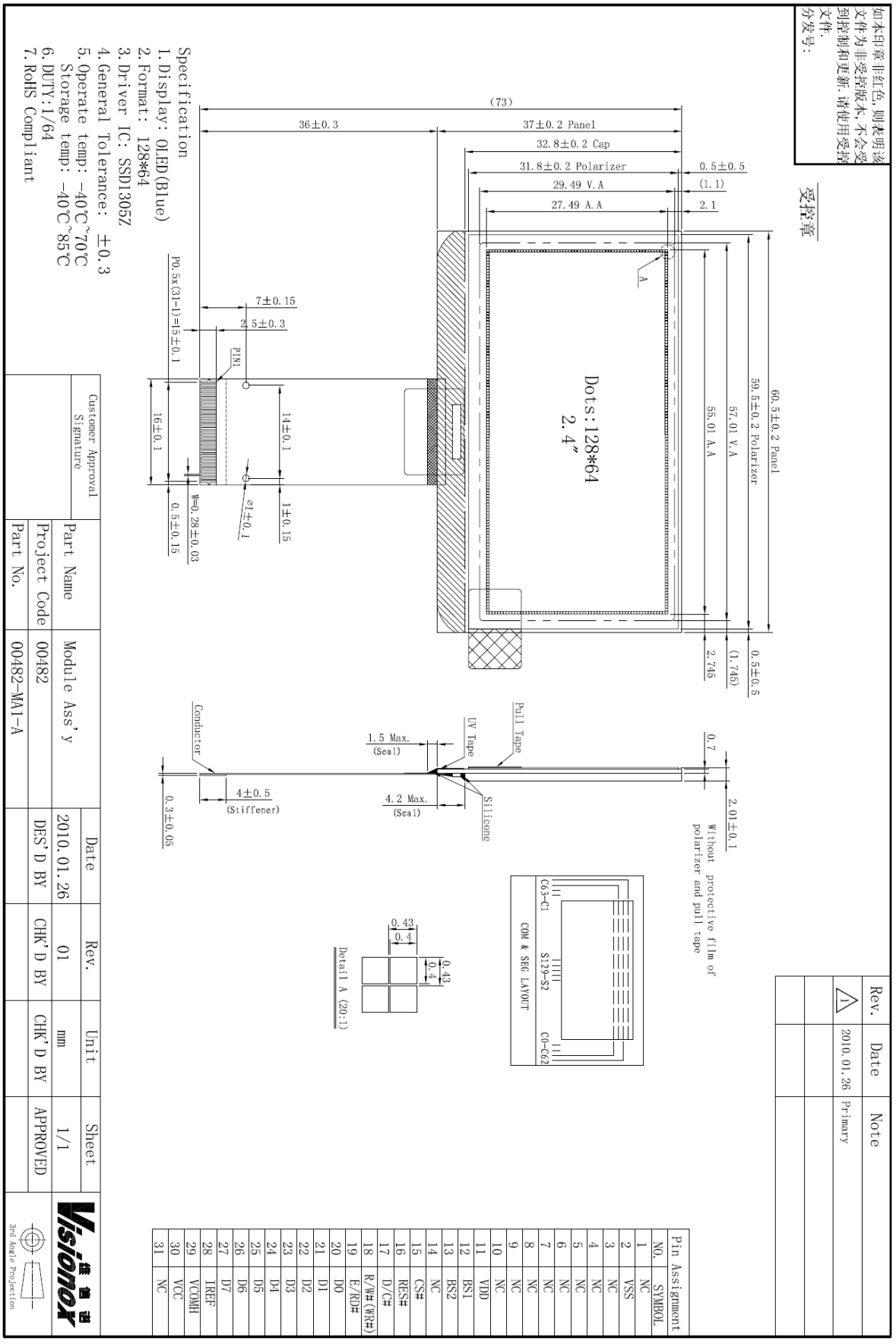
2 Features

- Display Color: Blue
- Dot Matrix: 128×64
- Driver IC: SSD1305Z
- Interface:8-bit 8080,8-bit 6800, SPI, I^2C
- Wide range of operating temperature: -40℃ to 70℃

3 Mechanical Data

NO.	ITEM	SPECIFICATION	UNIT
1	Dot Matrix	128(W)×64(H)	-
2	Dot Size	0.4(W)×0.4(H)	mm^2
3	Dot Pitch	0.43(W)×0.43(H)	mm^2
4	Aperture Rate	86	%
5	Active Area	55.01(W)×27.49(H)	mm^2
6	Panel Size	60.5(W)×37(H)×1.8(T)	mm^3
7	Module Size	60.5(W)×73(H)×2.01(T)	mm^3
8	Diagonal A/A Size	2.4	inch
9	Module Weight	9.1±10%	gram

4 Mechanical Drawing

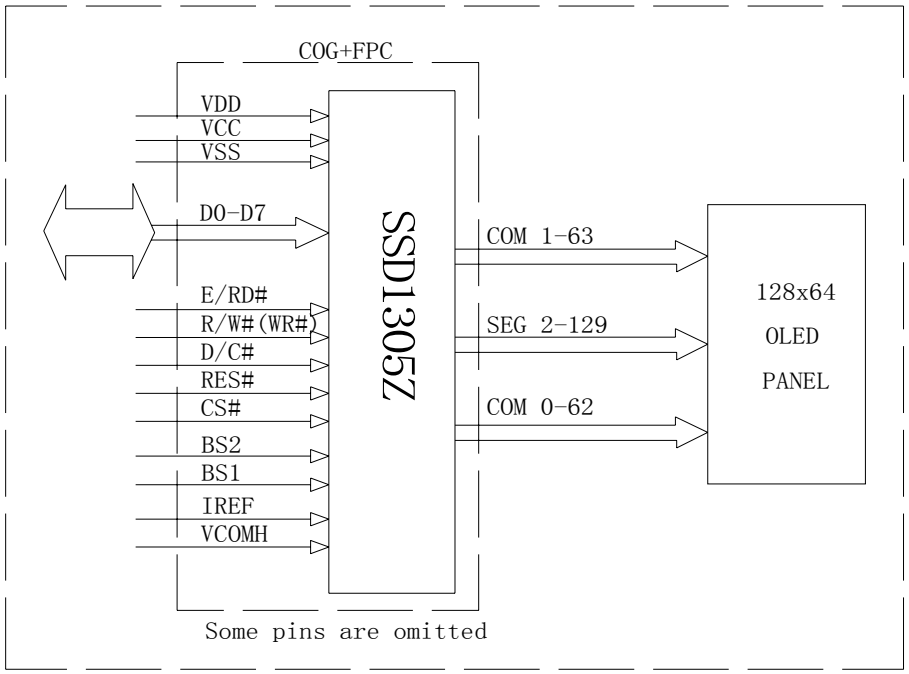


5 Module Interface

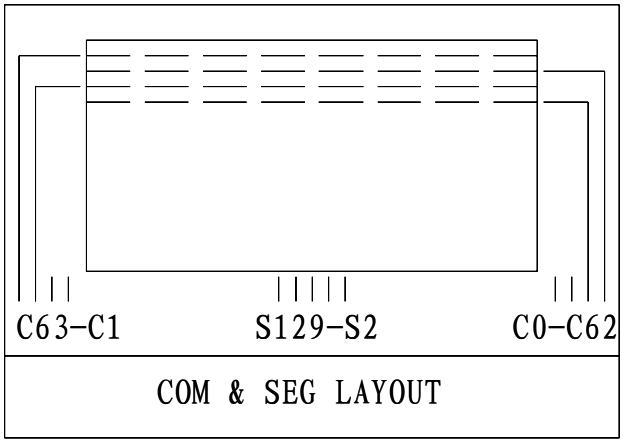
<table>
<tr><th>PIN NO.</th><th>PIN NAME</th><th>DESCRIPTION</th></tr>
<tr><td>1</td><td>NC</td><td>No Connection.</td></tr>
<tr><td>2</td><td>VSS</td><td>Ground.</td></tr>
<tr><td>3~10</td><td>NC</td><td>No Connection.</td></tr>
<tr><td>11</td><td>VDD</td><td>Power supply pin for core logic operation.</td></tr>
<tr><td>12</td><td>BS1</td><td rowspan="2">MCU bus interface selection pins.
<table>
<tr><th>Pin Name</th><th>I²C Interface</th><th>6800-parallel interface (8 bit)</th><th>8080-parallel interface (8 bit)</th><th>Serial interface</th></tr>
<tr><td>BS1</td><td>1</td><td>0</td><td>1</td><td>0</td></tr>
<tr><td>BS2</td><td>0</td><td>1</td><td>1</td><td>0</td></tr>
</table></td></tr>
<tr><td>13</td><td>BS2</td></tr>
<tr><td>14</td><td>NC</td><td>No Connection.</td></tr>
<tr><td>15</td><td>CS#</td><td>This pin is the chip select input.(active LOW)</td></tr>
<tr><td>16</td><td>RES#</td><td>Reset, active low.</td></tr>
<tr><td>17</td><td>D/C#</td><td>This is Data/Command control pin.When it is pulled HIGH(i.e.connect to VDDIO),the data at D[]7:0] is treated as data.When it is pulled LOW,the data at D[7:0] will be transferred to the command register.
In IIC mode ,this pin acts as SA0 for slave address selection.</td></tr>
<tr><td>18</td><td>R/W#(WR#)</td><td>This is read / write control input pin connecting to the MCU interface.
When interfacing to a 6800-series microprocessor, this pin will be used as Read/Write (R/W#) selection input. Read mode will be carried out when this pin is pulled HIGH (i.e. connect to VDDIO) and write mode when LOW.
When 8080 interface mode is selected, this pin will be the Write (WR#) input. Data write operation is initiated when this pin is pulled LOW and the chip is selected.
When serial interface is selected, this pin must be connected to VSS.</td></tr>
<tr><td>19</td><td>E/RD#</td><td>When interfacing to a 6800-series microprocessor, this pin will be used as the Enable (E) signal. Read/write operation is initiated when this pin is pulled HIGH (i.e. connect to VDDIO) and the chip is selected.
When connecting to an 8080-microprocessor, this pin receives the Read (RD#) signal. Read operation is initiated when this pin is pulled LOW and the chip is selected.
When serial interface is selected, this pin must be connected to VSS.</td></tr>
<tr><td>20~27</td><td>D0~D7</td><td>These are 8-bit bi-directional data bus to be connected to the microprocessor’s data bus.
When serial interface mode is selected, D0 will be the serial clock input: SCLK; D1 will be the serial data input: SDIN and D2 should be left opened.
When I2C mode is selected, D2, D1 should be tied together and serve as SDAout, SDAin in application and D0 is the serial clock input, SCL.</td></tr>
<tr><td>28</td><td>IREF</td><td>This is a segment current reference pin. A resistor should be connected between this pin and VSS. Set the current at 10uA.</td></tr>
<tr><td>29</td><td>VCOMH</td><td>The pin for COM signal deselected voltage level. A capacitor should be connected between this pin and VSS.</td></tr>
<tr><td>30</td><td>VCC</td><td>Power supply for panel driving voltage.This is also the most positive power voltage supply pin.</td></tr>
<tr><td>31</td><td>NC</td><td>No Connection.</td></tr>
</table>

6 Function Block Diagram

6.1 Function Block Diagram



6.2 Panel Layout Diagram



7 Absolute Maximum Ratings

ITEM	SYMBOL	MIN	MAX	UNIT	REMARK
Logic supply voltage	VDD	-0.3	4.0	V	IC maximum rating
OLED Operating voltage	VCC	0	16	V	IC maximum rating
Operating Temp.	Top	-40	70	℃	-
Storage Temp	Tstg	-40	85	℃	-

Note (1): All of the voltages are on the basis of "VSS = 0V".

Note (2): Permanent breakage of module may occur if the module is used beyond the maximum rating. The module can be normal operated under the conditions according to Section 8 "Electrical Characteristics". Malfunctioning of the module may occur and the reliability of the module may deteriorate if the module is used beyond the conditions.

8 Electrical Characteristics

8.1 DC Electrical Characteristics

ITEM	SYMBOL	TEST CONDITION	MIN	TYPE	MAX	UNIT
Logic Supply Voltage	VDD	22±3°C, 55±15%R.H	2.4	3.0	3.5	V
OLED Driver Supply Voltage	VCC	22±3°C, 55±15%R.H	14.5	15	15.5	V
High-level Input Voltage	V_{IH}	-	0.8×VDD	-	-	V
Low-level Input Voltage	V_{IL}	-	-	-	0.2×VDD	V
High-level Output Voltage	V_{OH}	-	0.9×VDD	-	-	V
Low-level Output Voltage	V_{OL}	-	-	-	0.1×VDD	V

Note : The V_{CC} input must be kept in a stable value; ripple and noise are not allowed.

8.2 Electro-optical Characteristics

ITEM	SYMBOL	TEST CONDITION	MIN	TYPE	MAX	UNIT
Normal Mode Brightness	L_{br}	All pixels ON(1)	40	60	-	cd/m^2
ICC Sleep mode Current	ICC,SLEEP	VDD=2.4V~3.5V, VCC=7~15V Display OFF, No panel attached	-	-	10	uA
IDD Sleep mode Current	IDD,SLEEP	VDD=2.4V~3.5V, VCC=7V~15V Display OFF, No panel attached	-	-	10	uA
Normal Mode Power Consumption	Pt	All pixels ON(1)	-	525	630	mW
C.I.E(Blue)	(x)	x,y(CIE1931)	0.12	0.16	0.20	-
	(y)		0.23	0.27	0.31	-
Dark Room Contrast	CR	-	≥2000:1	-	-	-
Response Time	-	-	-	10	-	μs
View Angle	-	-	≥160	-	-	Degree

Note(1): Normal Mode test conditions are as follows:

- Driving voltage : 15V
- Contrast setting : 0X80
- Frame rate : 105Hz
- Duty setting : 1/64

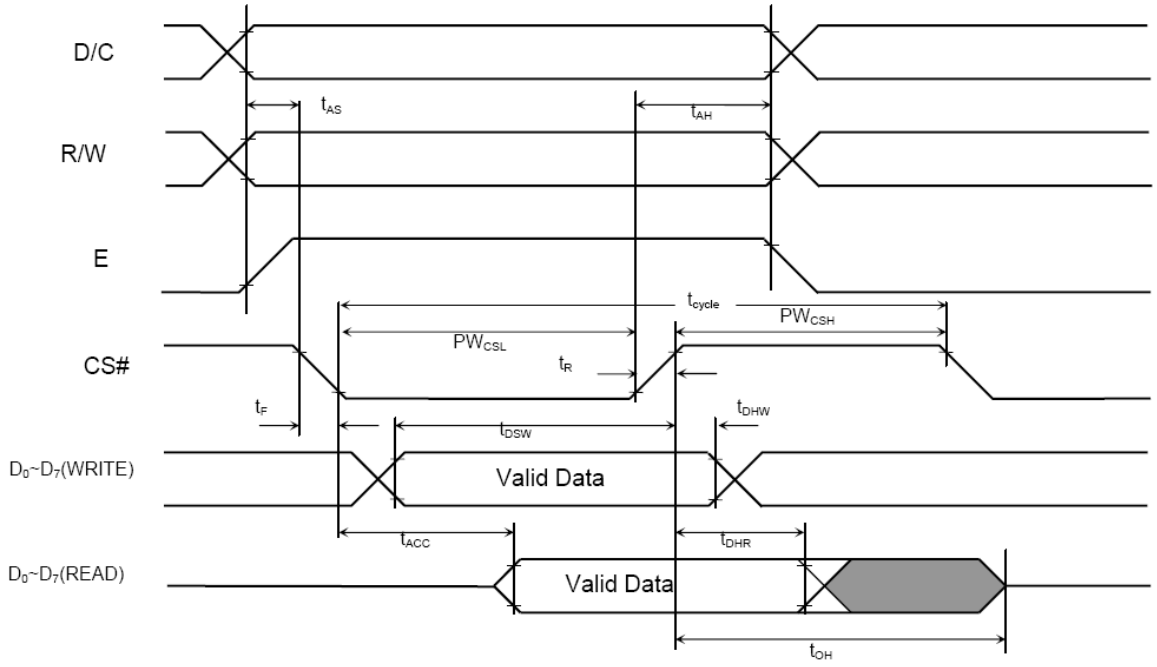
8.3 AC Electrical Characteristics

(1)6800-Series MPU Parallel Interface Timing Characteristics

(VDD - VSS = 2.4V to 3.5V, TA = 25°C)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	300	-	-	ns
t_{AS}	Address Setup Time	0	-	-	ns
t_{AH}	Address Hold Time	0	-	-	ns
t_{DSW}	Write Data Setup Time	40	-	-	ns
t_{DHW}	Write Data Hold Time	7	-	-	ns
t_{DHR}	Read Data Hold Time	20	-	-	ns
t_{OH}	Output Disable Time	-	-	70	ns
t_{ACC}	Access Time	-	-	140	ns
PW_{CSL}	Chip Select Low Pulse Width (read) Chip Select Low Pulse Width (write)	120 60	-	-	ns
PW_{CSH}	Chip Select High Pulse Width (read) Chip Select High Pulse Width (write)	60 60	-	-	ns
t_R	Rise Time	-	-	40	ns
t_F	Fall Time	-	-	40	ns

6800-series MCU parallel interface characteristics

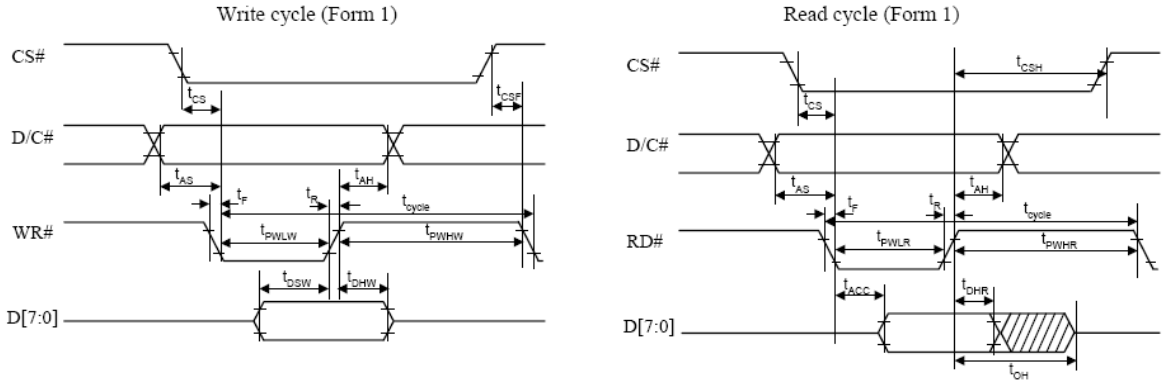


(2)8080-Series MPU Parallel Interface Timing Characteristics

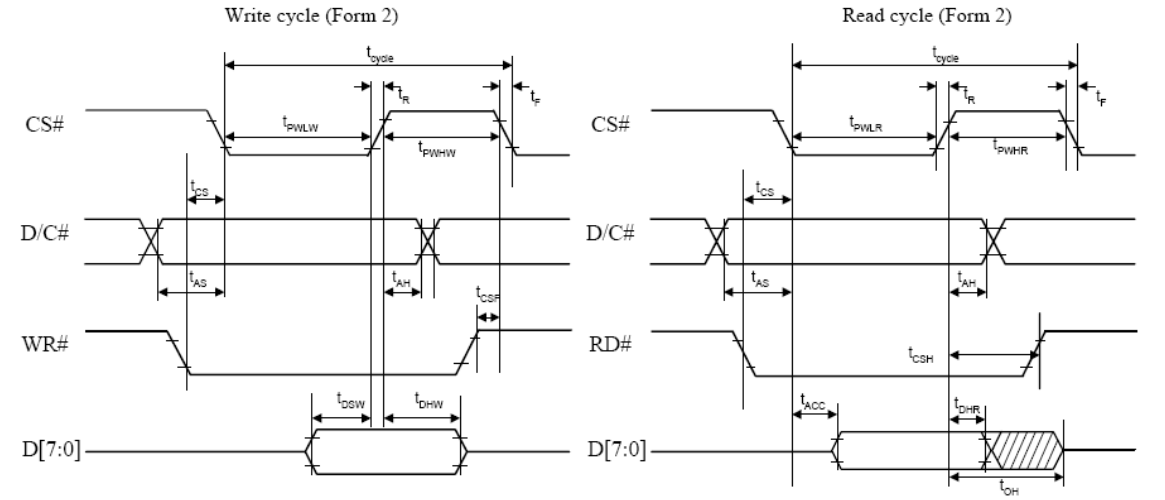
(VDD - VSS = 2.4V to 3.5V, TA = 25°C)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	300	-	-	ns
t_{AS}	Address Setup Time	10	-	-	ns
t_{AH}	Address Hold Time	0	-	-	ns
t_{DSW}	Write Data Setup Time	40	-	-	ns
t_{DHW}	Write Data Hold Time	7	-	-	ns
t_{DHR}	Read Data Hold Time	20	-	-	ns
t_{OH}	Output Disable Time	-	-	70	ns
t_{ACC}	Access Time	-	-	140	ns
t_{PWLR}	Read Low Time	120	-	-	ns
t_{PWLW}	Write Low Time	60	-	-	ns
t_{PWHR}	Read High Time	60	-	-	ns
t_{PWHW}	Write High Time	60	-	-	ns
t_R	Rise Time	-	-	40	ns
t_F	Fall Time	-	-	40	ns
t_{CS}	Chip select setup time	0	-	-	ns
t_{CSH}	Chip select hold time to read signal	0	-	-	ns
t_{CSF}	Chip select hold time	20	-	-	ns

8080-series parallel interface characteristics (Form 1)



8080-series parallel interface characteristics (Form 2)

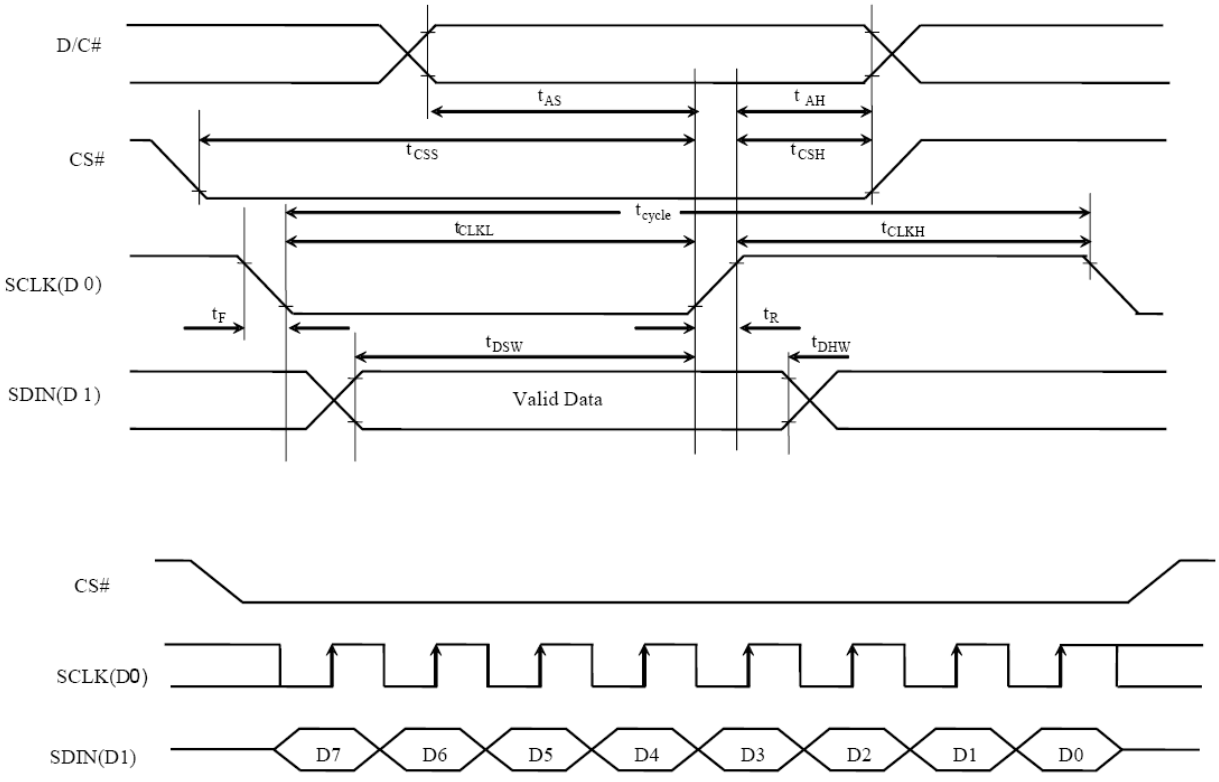


(3)Serial Interface Timing Characteristics

(VDD - VSS = 2.4V to 3.5V, TA = 25°C)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	250	-	-	ns
t_{AS}	Address Setup Time	150	-	-	ns
t_{AH}	Address Hold Time	150	-	-	ns
t_{CSS}	Chip Select Setup Time	120	-	-	ns
t_{CSH}	Chip Select Hold Time	60	-	-	ns
t_{DSW}	Write Data Setup Time	50	-	-	ns
t_{DHW}	Write Data Hold Time	15	-	-	ns
t_{CLKL}	Clock Low Time	100	-	-	ns
t_{CLKH}	Clock High Time	100	-	-	ns
t_R	Rise Time	-	-	40	ns
t_F	Fall Time	-	-	40	ns

Serial interface characteristics

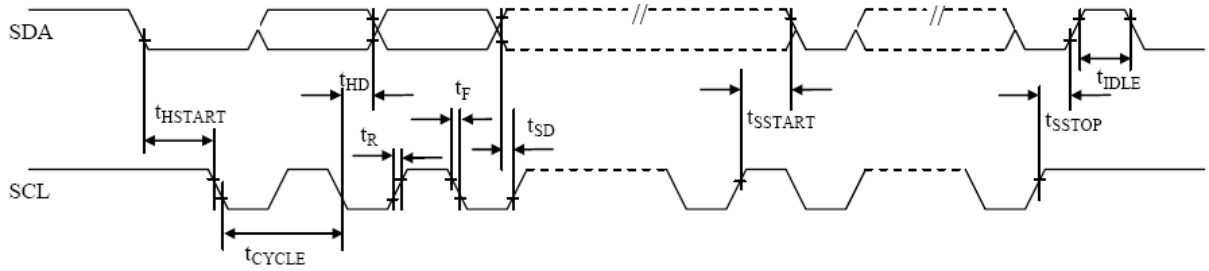


(4) I²C interface Timing Characteristics

(VDD - VSS = 2.4V to 3.5V, TA = 25°C)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	2.5	-	-	us
t_{HSTART}	Start condition Hold Time	0.6	-	-	us
t_{HD}	Data Hold Time (for "SDA_{OUT}" pin)	0	-	-	ns
	Data Hold Time (for "SDA_{IN}" pin)	300	-	-	ns
t_{SD}	Data Setup Time	100	-	-	ns
t_{SSTART}	Start condition Setup Time (Only relevant for a repeated Start condition)	0.6	-	-	us
t_{SSTOP}	Stop condition Setup Time	0.6	-	-	us
t_R	Rise Time for data and clock pin	-	-	300	ns
t_F	Fall Time for data and clock pin	-	-	300	ns
t_{IDLE}	Idle Time before a new transmission can start	1.3	-	-	us

I²C interface Timing characteristics

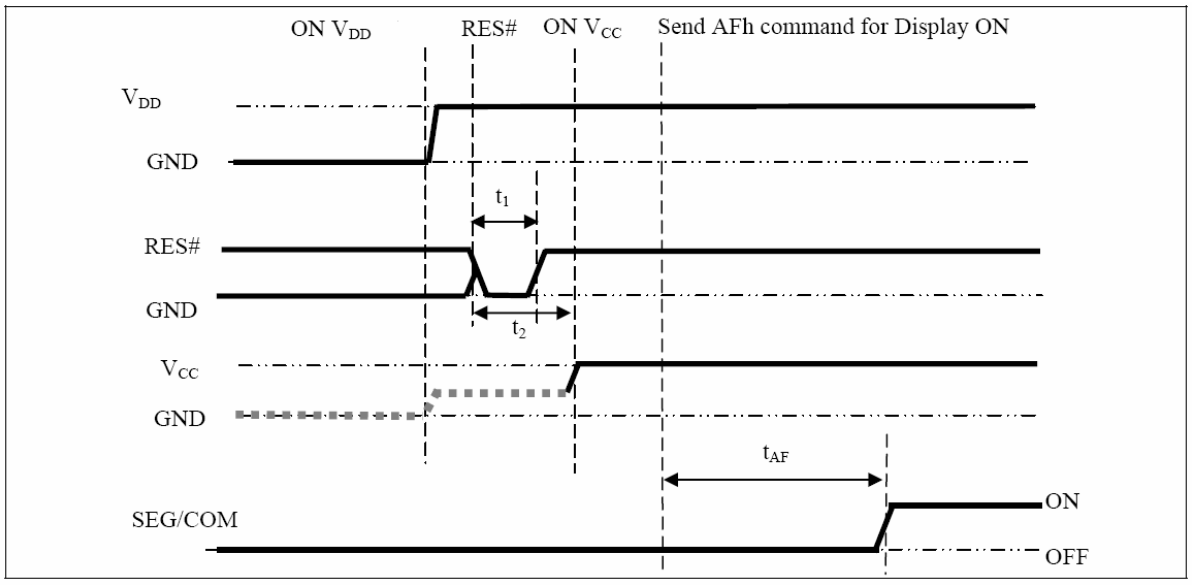


9 Functional Specification and Application Circuit

9.1 Power ON and Power OFF Sequence

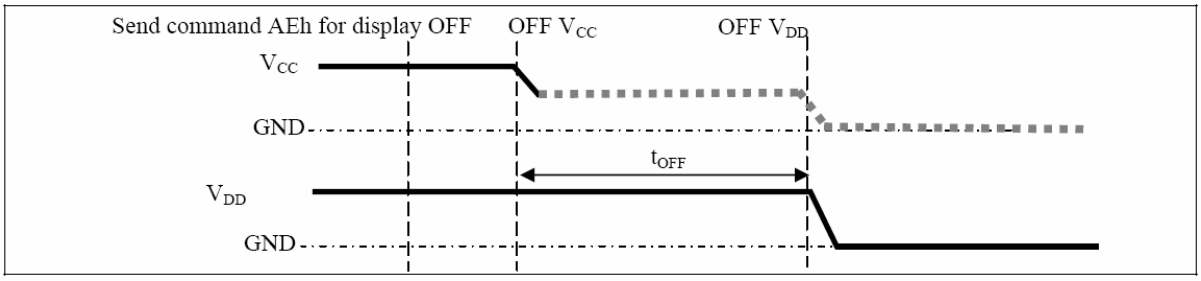
Power ON Sequence:

1. Power ON VDD
2. After VDD, become stable, set RES# pin LOW (logic low) for at least 3us (t1)(4) and then HIGH (logic high).
3. After set RES# pin LOW (logic low), wait for at least 3us (t2). Then Power ON VCC(1).
4. After VCC become stable, send command AFh for display ON. SEG/COM will be ON after 100ms(tAF).



Power OFF Sequence:

1. Send command AEh for display OFF.
2. Power OFF VCC(1),(2),(3).
3. Wait for tOFF. Power OFF VDD (where Minimum tOFF=0ms(5), Typical tOFF=100ms)



Note:

(1)Since an ESD protection circuit is connected between VDDand VCC, VCC becomes lower than VDD whenever VDDis ON and VCC is OFF as shown in the dotted line of VCC in above figures.

(2) VCC should be kept float (disable) when it is OFF.

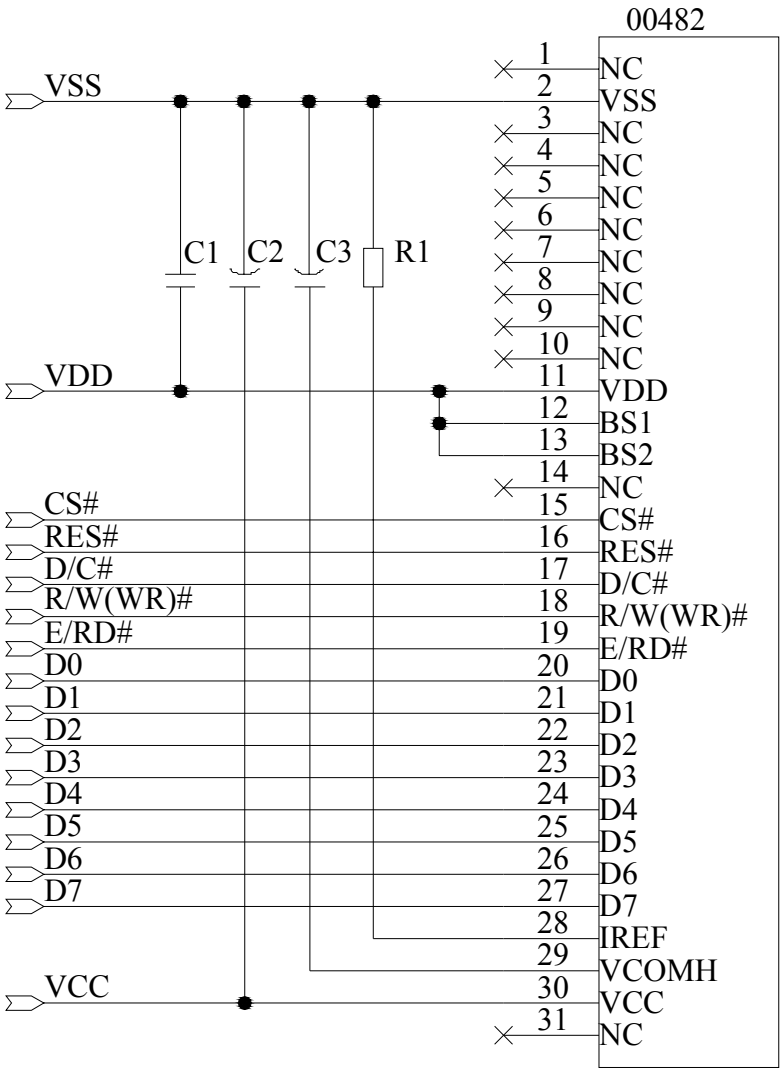
(3) Power Pins(VDD, VCC) can never be pulled to ground under any circumstance.

(4) The register values are reset after t1.

(5) VDD should not be Power OFF before VCC Power OFF

9.2 Application Circuit

(1).The configuration for 8-bit 8080-parallel interface mode, external VCC is shown in the following diagram.



Pin connected to MCU interface: D[0:7], E/RD#, R/W(WR)#, D/C#, CS#, RES#

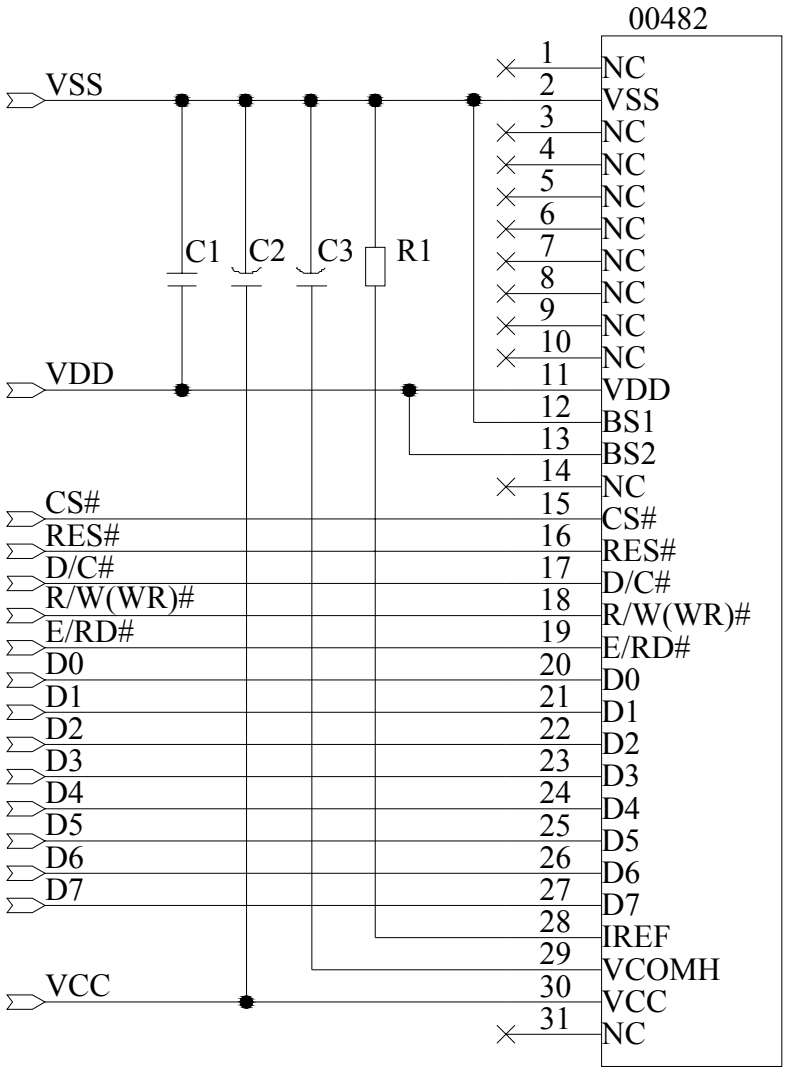
Component:

C1: 0.1uF-0603-X7R±10%.ROHS

C2, C3: 4.7μF/25V.ROHS (Tantalum Capacitors)

R1: 910K ohm 0603 1/10W +/-5%.ROHS

(2).The configuration for 8-bit 6800-parallel interface mode, external VCC is shown in the following diagram.



Pin connected to MCU interface: D[0:7], E/RD#, R/W(WR)#, D/C#, CS#, RES#

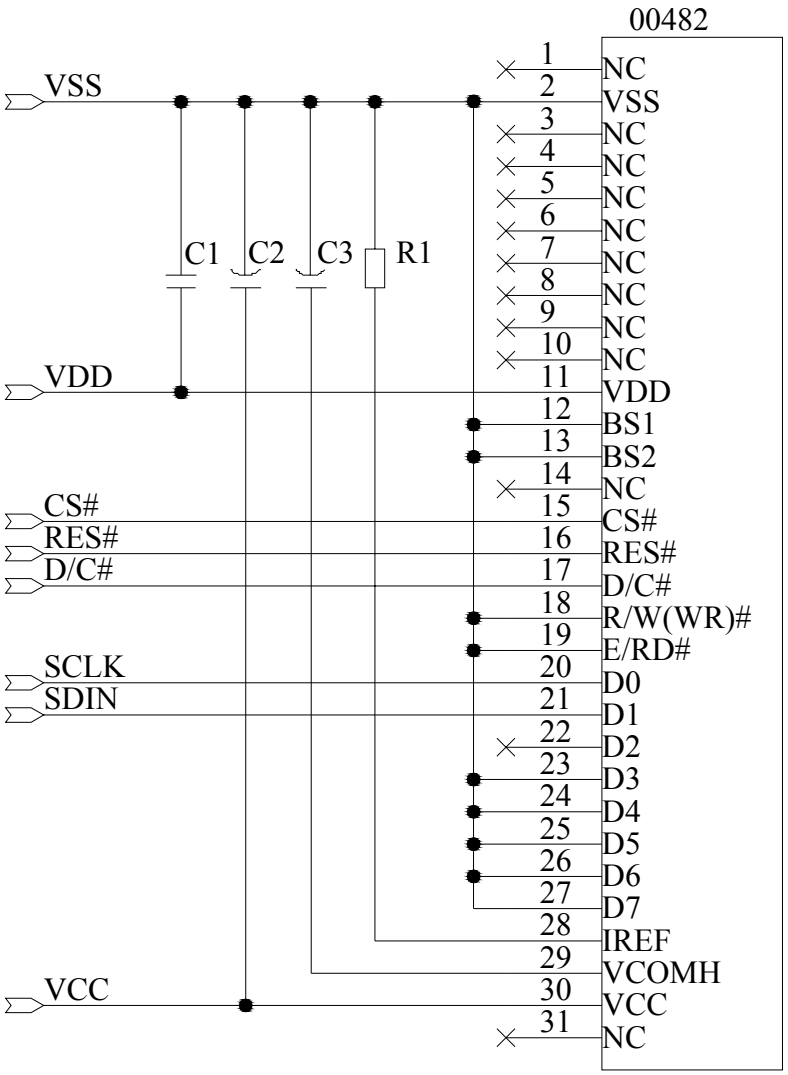
Component:

C1: 0.1uF-0603-X7R±10%.ROHS

C2, C3: 4.7μF/25V.ROHS (Tantalum Capacitors)

R1: 910K ohm 0603 1/10W +/-5%.ROHS

(3).The configuration for SPI interface mode,
external VCC is shown in the following diagram.



Pin connected to MCU interface:SCLK,SDIN, D/C#, CS#, RES#

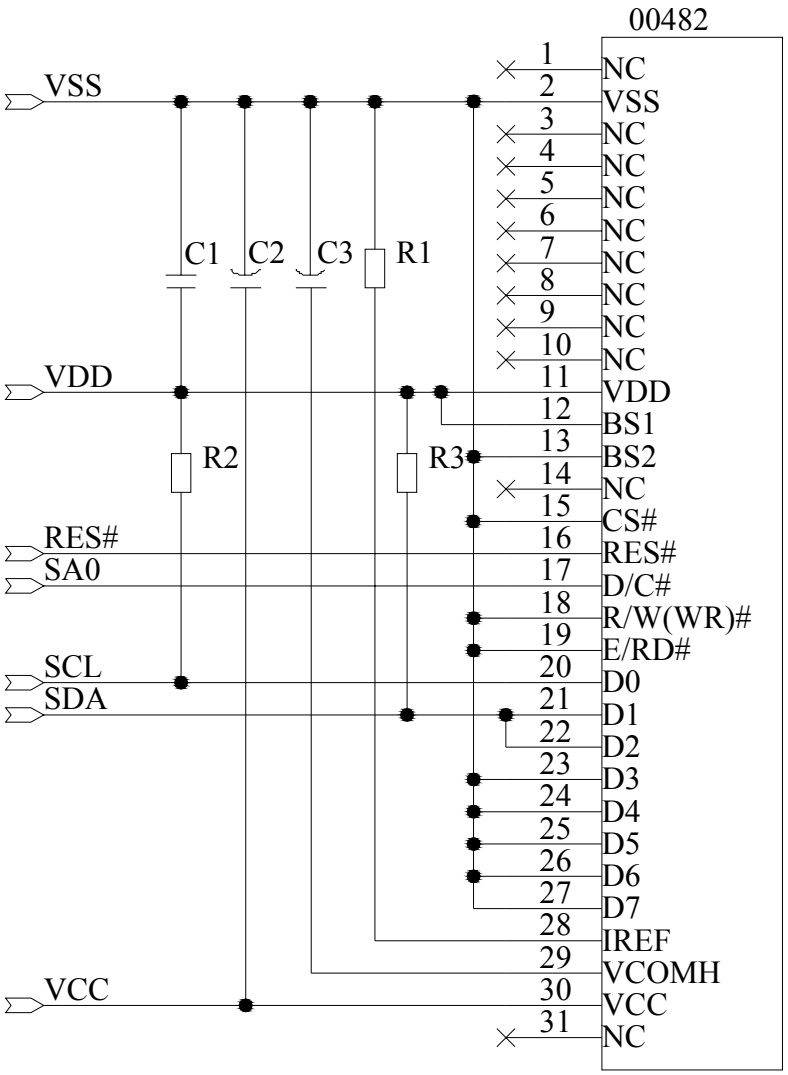
Component:

C1: 0.1uF-0603-X7R±10%.ROHS

C2, C3: 4.7μF/25V.ROHS (Tantalum Capacitors)

R1: 910K ohm 0603 1/10W +/-5%.ROHS

(4).The configuration for I²C interface mode,
external VCC is shown in the following diagram.



Pin connected to MCU interface: SCL,SDA,SA0, RES#

Component:

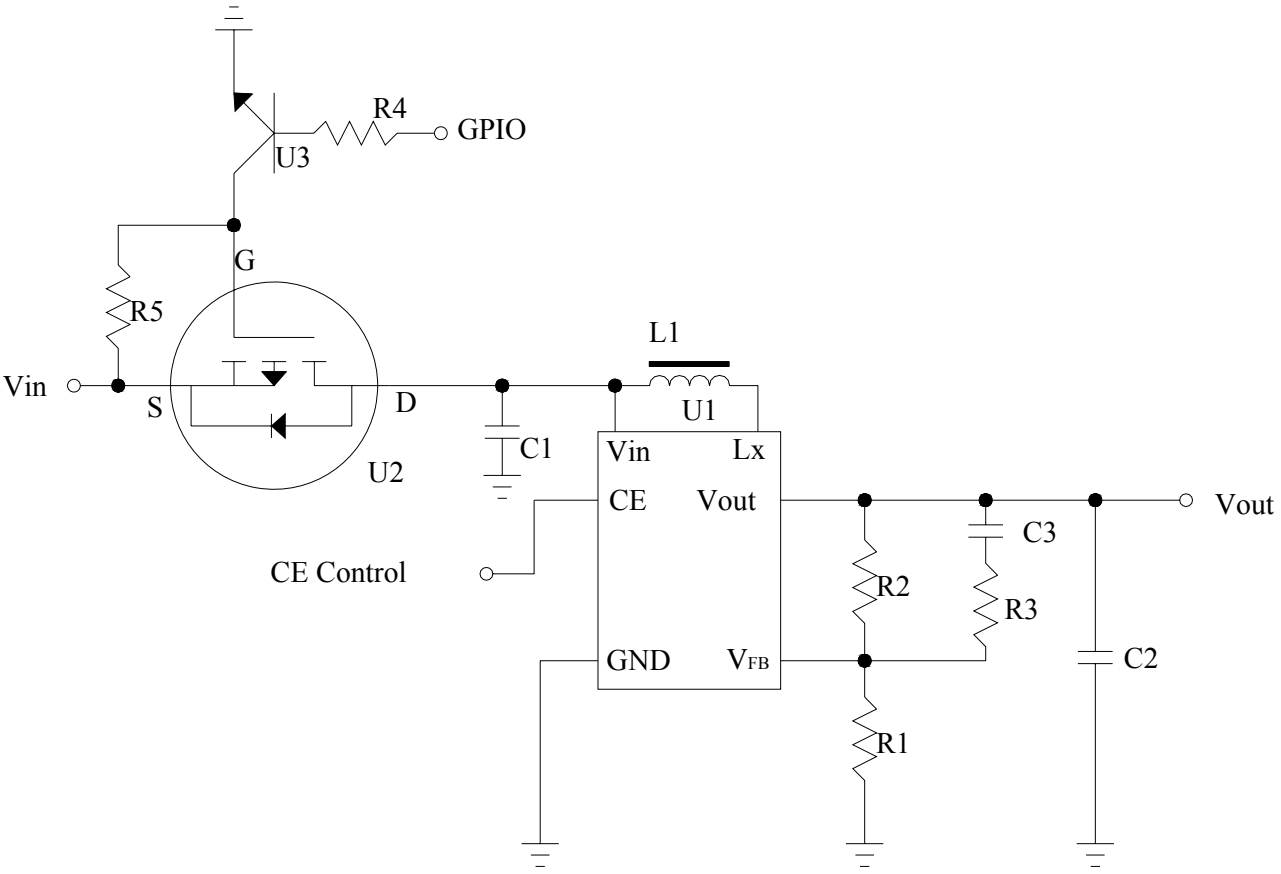
C1: 0.1uF-0603-X7R±10%.ROHS

C2, C3: 4.7μF/25V.ROHS (Tantalum Capacitors)

R1: 910K ohm 0603 1/10W +/-5%.ROHS

R2,R3: 10K ohm 0603 1/10W +/-5%.ROHS

9.3 External DC-DC application circuit



Recommend component

The C1	: 1 uF-0603-X7R±10%.ROHS
The C2	: 1 uF-0603-X7R±10%.ROHS
The C3	: 220pF-0603-X7R±10%.ROHS
The R1	: 0603 1/10W +/-5% 10Kohm.ROHS
The R2	: 0603 1/10W +/-5% 140 Kohm.ROHS
The R3	: 0603 1/10W +/-5% 2Kohm.ROHS
The R4	: 0603 1/10W +/-5% 1Kohm.ROHS
The R5	: 0603 1/10W +/-5% 10Kohm.ROHS
The L1	: 22uH
The U1	: R1200
The U2	: FDN338N
The U3	: 8050

9.4 Display Control Instruction

Refer to SSD1305 IC Specification.

9.5 Recommended Software Initialization

```
void Init_SSD1305()
{
    Write_Command(0xae);        //Display off
    Write_Command(0xa1);        //segment remap
    Write_Command(0xda);        //common pads hardware: alternative
    Write_Command(0x12);
    Write_Command(0xc8);        //common output scan direction:com63~com0
    Write_Command(0xa8);        //multiplex ration mode:63
    Write_Command(0x3f);
    Write_Command(0xd5);        //display divide ratio/osc. freq. mode
    Write_Command(0x50);        //Osc. Freq:320kHz,DivideRation:1
    Write_Command(0x81);        //contrast control
    Write_Command(0x80);        // mode:64
    Write_Command(0xd9);        //set pre-charge period
    Write_Command(0xf1);        //set period 1:1;period 2:15
    Write_Command(0x20);        //Set Memory Addressing Mode
    Write_Command(0x02);        //page addressing mode
    Write_Command(0xdb);        //VCOM deselect level mode
    Write_Command(0x3c);        //set Vvcomh=0.83*Vcc
    Write_Command(0xad);        //master configuration
    Write_Command(0x8e);        //external VCC supply
    Write_Command(0xa4);        //out follows RAM content
    Write_Command(0xa6);        //set normal display
    Write_Command(0xaf);        //Display on

}
```

10 Package Specification

Controlled Seal

Packing Process(1) ~ (9)

(1) TRAY Type:00482-MT1-A
Add EPE in every contained tray

(2)

(3) order①、②、①、②
fix trays with tape
240 pcs of 1 small carton
1 tray contain 12 pcs
20 contained trays, 1 empty tray

(4) package with plastic bags
add five desiccants
create a power vacuum

(5)

(6)

(7)

small carton package

(8)

2 small cartons in 1 big carton

(9) 40 contained trays, 2 empty trays,
Package quantity products:
480 pcs of 1 big carton

Package finished

NOTE:1、The inner carton and master carton must be sealed with adhesive tape.

2、Fill up the gap with EPE.

3、If the customer has special needs with the RoHS making, the inner carton and master carton need adhesive new RoHS marking at ⓒ.