Product Specification

Product Name: VGM128128A1F02

Product Code: M0009B

Customer
Approved by Customer
Approved Date:

Designed By	Checked By	Approved By	
		R&D	QA
2012.11.8	2012.11.8	2012.11.8	2012.11.8

CONTENT

REVISION RECORD

REV.	REVISION DESCRIPTION	REV. DATE	REMARK
Y01	Initial release.	2010-07-14	
Y02	Update Mechanical Data Update the Module Interface Update the Function Block Diagram Update the Electro-optical Characteristics Update the Application Circuit Update the Reliability Test	2011-1-12	Page 4 Page 6 Page 7 Page 9 Page 15~19 Page 24
A01	Update the Serial Interface Timing Characteristics(3-wire SPI) Update the Power ON and Power OFF Sequence Update the Application Circuit(The double byte command 0xAB) Update the External DC-DC application circuit Update the Recommended Software Initialization(0xCF command) Update the Package Specification	2011-08-23	Page 13 Page 14 Page 15 Page 20 Page 21 Page 23
A02	Update the Recommended Software Initialization Update the Package Specification	2012-02-13	Page 21~22 Page 23
A03	Update the Features Update the Electro-optical Characteristics Update the Application Circuit	2012-05-19	Page 4 Page 9 Page 15
A04	Update the Application Circuit(4-Wire SPI)	2012-7-30	Page 19
B01	Update the Electro-optical Characteristics Update the Recommended Software Initialization Update the Lifetime	2012-11-08	Page 9 Page 21~25 Page 27

1 Overview

VGM128128A1F02 is a full color OLED display module with 128(RGB) ×128 dot matrix. The characteristics of this display module are high brightness, self-emission, high contrast ratio, slim/thin outline, wide viewing angle, wide temperature range, and low power consumption.

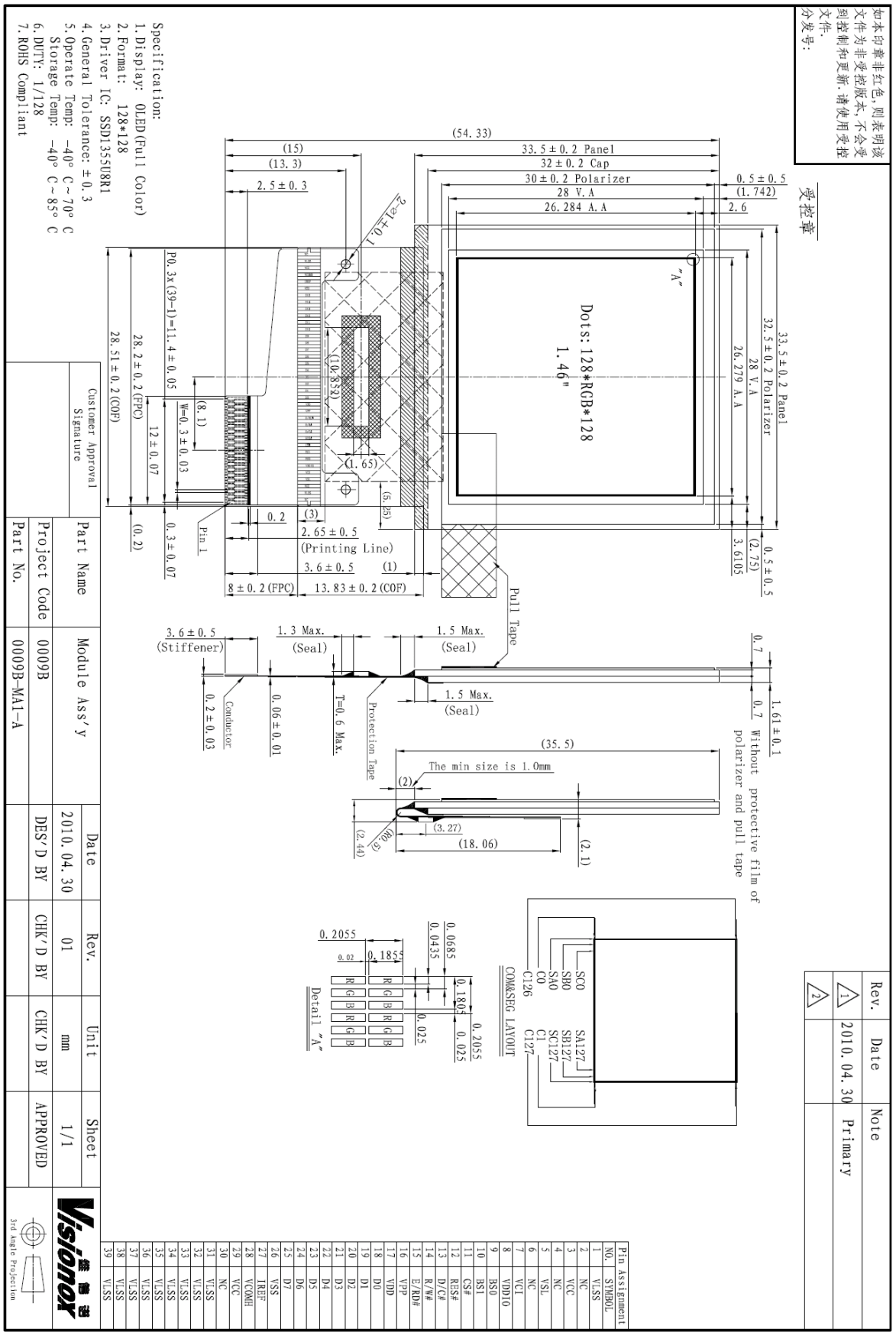
2 Features

- Display Color: Full Color
- Dot Matrix:128(RGB)×128
- Driver IC: SSD1355U8R1
- Interface:8-bit 8080, 8-bit 6800, 3/4SPI
- Wide range of operating temperature: -40℃ to 70℃

3 Mechanical Data

NO.	ITEM	SPECIFICATION	UNIT
1	Dot Matrix	128(W)(RGB)×128(H)	-
2	Dot Size	0.0435(W)×0.1855(H)	mm^2
3	Dot Pitch	0.0685(W)×0.2055(H)	mm^2
4	Aperture Rate	57	%
5	Active Area	26.279(W)×26.284 (H)	mm^2
6	Panel Size	33.5(W)×33.5(H) ×1.4(T)	mm^3
7	Module Size	33.5(W)×54.33(H) ×1.61(T)	mm^3
8	Diagonal A/A Size	1.46	inch
9	Module Weight	3.9±10%	gram

4 Mechanical Drawing



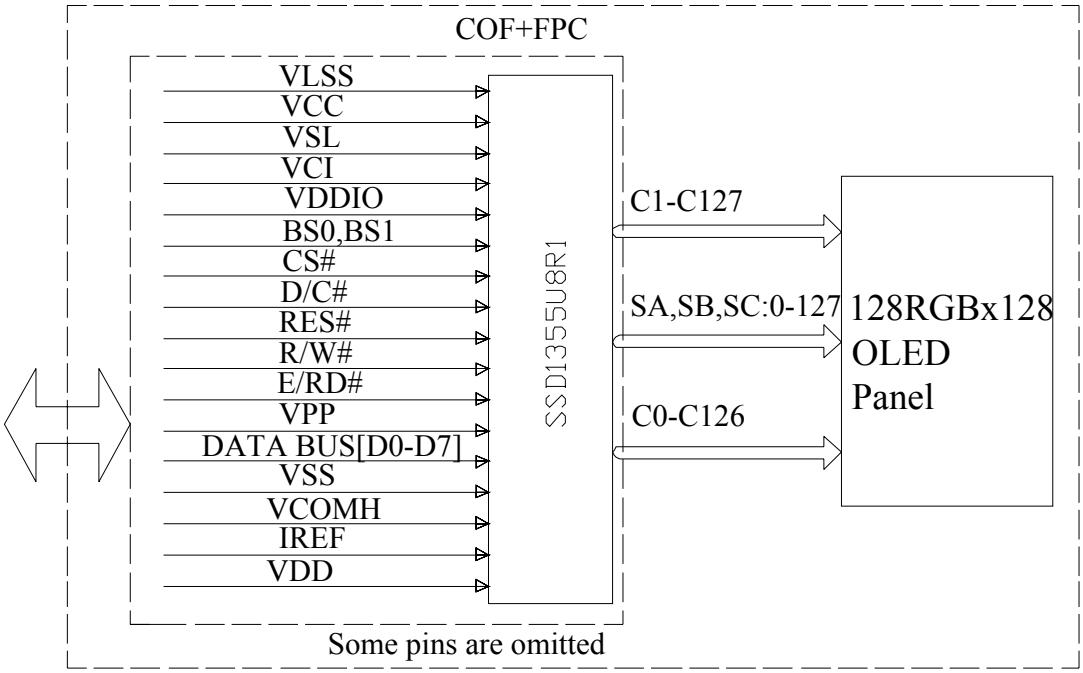
Pin Assignment		
NO.	SYMBOL	
1	VLSS	
2	NC	
3	VCC	
4	NC	
5	VSL	
6	NC	
7	VCI	
8	VDDIO	
9	BS0	
10	BS1	
11	CS#	
12	RES#	
13	D/C#	
14	R/W#	
15	E/RD#	
16	VPP	
17	VDD	
18	D0	
19	D1	
20	D2	
21	D3	
22	D4	
23	D5	
24	D6	
25	D7	
26	VSS	
27	IREF	
28	VCOMH	
29	VCC	
30	NC	
31	VLSS	
32	VLSS	
33	VLSS	
34	VLSS	
35	VLSS	
36	VLSS	
37	VLSS	
38	VLSS	
39	VLSS	

5 Module Interface

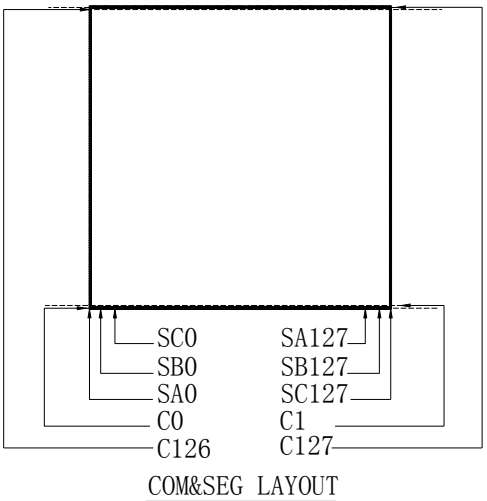
<table>
<tr><th>PIN NO.</th><th>PIN NAME</th><th>DESCRIPTION</th></tr>
<tr><td>1</td><td>VLSS</td><td>Analog system ground pin</td></tr>
<tr><td>2</td><td>NC</td><td>No Connection.</td></tr>
<tr><td>3</td><td>VCC</td><td>Power supply for panel driving voltage. This is also the most positive power voltage supply pin. It is supplied by external high voltage source.</td></tr>
<tr><td>4</td><td>NC</td><td>No Connection.</td></tr>
<tr><td>5</td><td>VSL</td><td>This is segment voltage reference pin.
When externa VSL is not used,this pin should be left open.
When external VSL is used,connect with resistor and diode to ground</td></tr>
<tr><td>6</td><td>NC</td><td>No Connection.</td></tr>
<tr><td>7</td><td>VCI</td><td>Low voltage power supply
VCI must always be equal to or higher than VDD and VDDIO.</td></tr>
<tr><td>8</td><td>VDDIO</td><td>Power supply for interface logic level. It should match with the MCU interface voltage level and must be connected to external source.</td></tr>
<tr><td>9</td><td>BS0</td><td rowspan="2">BS3 and BS2 are command programmable (by command 36H). BS1 and BS0 are pin select
<table><tr><td>BS[3:0]</td><td>Interface</td></tr><tr><td>0000</td><td>4 line SPI</td></tr><tr><td>0001</td><td>3 line SPI</td></tr><tr><td>0011</td><td>8-bit 6800 parallel</td></tr><tr><td>0010</td><td>8-bit 8080 parallel</td></tr></table></td></tr>
<tr><td>10</td><td>BS1</td></tr>
<tr><td>11</td><td>CS#</td><td>This pin is the chip select input connecting to the MCU.
The chip is enabled for MCU communication only when CS# is pulled LOW.</td></tr>
<tr><td>12</td><td>RES#</td><td>This pin is reset signal input.
When the pin is pulled LOW, initialization of the chip is executed.
Keep this pin pull HIGH during normal operation.</td></tr>
<tr><td>13</td><td>D/C#</td><td>This pin is Data/Command control pin connecting to the MCU.</td></tr>
<tr><td>14</td><td>R/W#</td><td>This pin is read / write control input pin connecting to the MCU interface.
When 6800 interface mode is selected, this pin will be used as Read/Write (R/W#) selection input. Read mode will be carried out when this pin is pulled HIGH and write mode when LOW.
When 8080 interface mode is selected, this pin will be the Write (WR#) input. Data write operation is initiated when this pin is pulled LOW and the chip is selected.</td></tr>
<tr><td>15</td><td>E/RD#</td><td>This pin is MCU interface input.
When 6800 interface mode is selected, this pin will be used as the Enable (E) signal. Read/write operation is initiated when this pin is pulled HIGH and the chip is selected.
When 8080 interface mode is selected, this pin receives the Read (RD#) signal. Read operation is initiated when this pin is pulled LOW and the chip is selected.
When serial interface is selected, this pin E(RD#) must be connected to VSS.</td></tr>
<tr><td>16</td><td>VPP</td><td>Power supply for programming OTP.</td></tr>
<tr><td>17</td><td>VDD</td><td>Power supply pin for core logic operation.</td></tr>
<tr><td>18~25</td><td>D0-D7</td><td>These pins are bi-directional data bus connecting to the MCU data bus.</td></tr>
<tr><td>26</td><td>VSS</td><td>Ground pin</td></tr>
<tr><td>27</td><td>IREF</td><td>A resistor should be connented between this pin and VSS.</td></tr>
<tr><td>28</td><td>VCOMH</td><td>A capacitor should be connected between this pin and VSS.</td></tr>
<tr><td>29</td><td>VCC</td><td>Power supply for panel driving voltage. This is also the most positive power voltage supply pin. It is supplied by external high voltage source.</td></tr>
<tr><td>30</td><td>NC</td><td>No Connection.</td></tr>
<tr><td>31~39</td><td>VLSS</td><td>Analog system ground pin</td></tr>
</table>

6 Function Block Diagram

6.1 Function Block Diagram



6.2 Panel Layout Diagram



7 Absolute Maximum Ratings

ITEM	SYMBOL	MIN	MAX	UNIT	REMARK
Logic supply voltage	VDD	-0.5	2.75	V	IC maximum rating
Low voltage power supply	VCI	-0.3	4.0	V	IC maximum rating
Power supply for interface logic level.	VDDIO	-0.5	VCI	V	IC maximum rating
OLED Operating voltage	VCC	0	22	V	IC maximum rating
Operating Temp.	Top	-40	70	℃	-
Storage Temp	Tstg	-40	85	℃	-

Note (1): All of the voltages are on the basis of "VSS = 0V".

Note (2): Permanent breakage of module may occur if the module is used beyond the maximum rating. The module can be normal operated under the conditions according to Section 8 "Electrical Characteristics". Malfunctioning of the module may occur and the reliability of the module may deteriorate if the module is used beyond the conditions.

8 Electrical Characteristics

8.1 DC Electrical Characteristics

ITEM	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNIT
Logic Supply Voltage	VDD	22±3°C, 55±15%R.H	2.4	-	2.6	V
OLED Driver Supply Voltage	VCC	22±3°C, 55±15%R.H	16	16.5	17	V
Low Voltage power supply	VCI	-	2.4	-	3.5	V
Power Supply for I/O pins	VDDIO	-	1.6	-	VCI	V
High-level Input Voltage	V_{IH}	-	0.8×VDDIO	-	VDDIO	V
Low-level Input Voltage	V_{IL}	-	0	-	0.2×VDDIO	V
High-level Output Voltage	V_{OH}	-	0.9×VDDIO	-	VDDIO	V
Low-level Output Voltage	V_{OL}	-	0	-	0.1×VDDIO	V

Note : The VCC input must be kept in a stable value; ripple and noise are not allowed.

8.2 Electro-optical Characteristics

ITEM	SYMBOL	TEST CONDITION		MIN	TYP	MAX	UNIT
Normal Mode Brightness(White)	L_{br}	All pixels ON(1)		60	80	-	cd/m^2
Sleep mode Current	ISLP_VDD	VCI = VDDIO =2.8V, VCC = OFF VDD(external) = 2.5V, Display OFF, No panel attached		-	-	20	uA
	ISLP_VDDIO	VCI = VDDIO =2.8V, VCC = OFF Display OFF, No panel attached	External VDD = 2.5V	-	-	20	uA
			Internal VDD	-	-	20	uA
	ISLP_VCI	VCI = VDDIO =2.8V, VCC = OFF Display OFF, No panel attached	External VDD = 2.5V	-	-	20	uA
			Enable Internal VDD during Sleep mode	-	-	140	uA
			Disable Internal VDD during Sleep mode	-	-	20	uA
Normal Mode Power Consumption	Pt	All pixels ON(1)		-	676.5	825	mW
C.I.E(White)	(x)	x,y(CIE1931)		0.26	0.30	0.34	-
	(y)			0.29	0.33	0.37	-
C.I.E(Red)	(x)	x,y(CIE1931)		0.61	0.65	0.69	-
	(y)			0.30	0.34	0.38	-
C.I.E(Green)	(x)	x,y(CIE1931)		0.25	0.29	0.33	-
	(y)			0.54	0.58	0.62	-
C.I.E(Blue)	(x)	x,y(CIE1931)		0.10	0.14	0.18	-
	(y)			0.13	0.17	0.21	-
Dark Room Contrast	CR	-		≥2000:1	-	-	-
Response Time	-	-		---	10	-	μ s
View Angle	-	-		≥160	-	-	Degree

Note(1): Normal Mode test conditions are as follows:

- Driving voltage : 16.5V
- Red contrast setting : 0xc8
- Green contrast setting : 0x55
- Blue contrast setting : 0x99
- Frame rate : 105Hz
- Duty setting : 1/128

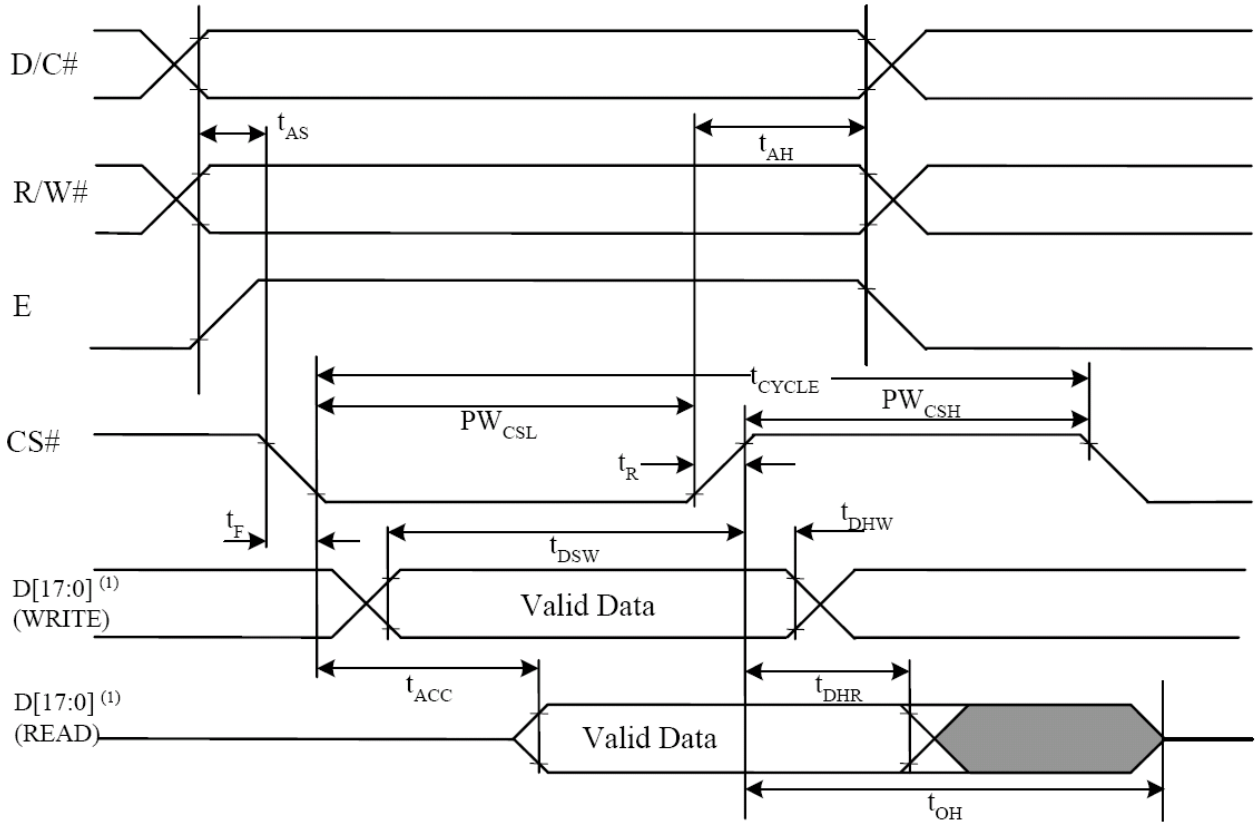
8.3 AC Electrical Characteristics

(1)6800-Series MPU Parallel InterfaceTiming Characteristics

(V_{DD} - V_{SS} = 2.4 to 2.6V, V_{DDIO}=1.6V, V_{CI} = 2.8V, T_A = 25°C)

Symbol	Parameter	Min	Typ	Max	Unit
t_{CYCLE}	Clock Cycle Time	300	-	-	ns
t_{AS}	Address Setup Time	10	-	-	ns
t_{AH}	Address Hold Time	0	-	-	ns
t_{DSW}	Write Data Setup Time	40	-	-	ns
t_{DHW}	Write Data Hold Time	7	-	-	ns
t_{DHR}	Read Data Hold Time	20	-	-	ns
t_{OH}	Output Disable Time	-	-	70	ns
t_{ACC}	Access Time	-	-	140	ns
PW_{CSL}	Chip Select Low Pulse Width (read) Chip Select Low Pulse Width (write)	120 60	-	-	ns
PW_{CSH}	Chip Select High Pulse Width (read) Chip Select High Pulse Width (write)	60 60	-	-	ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns

6800-series MCU parallel interface characteristics

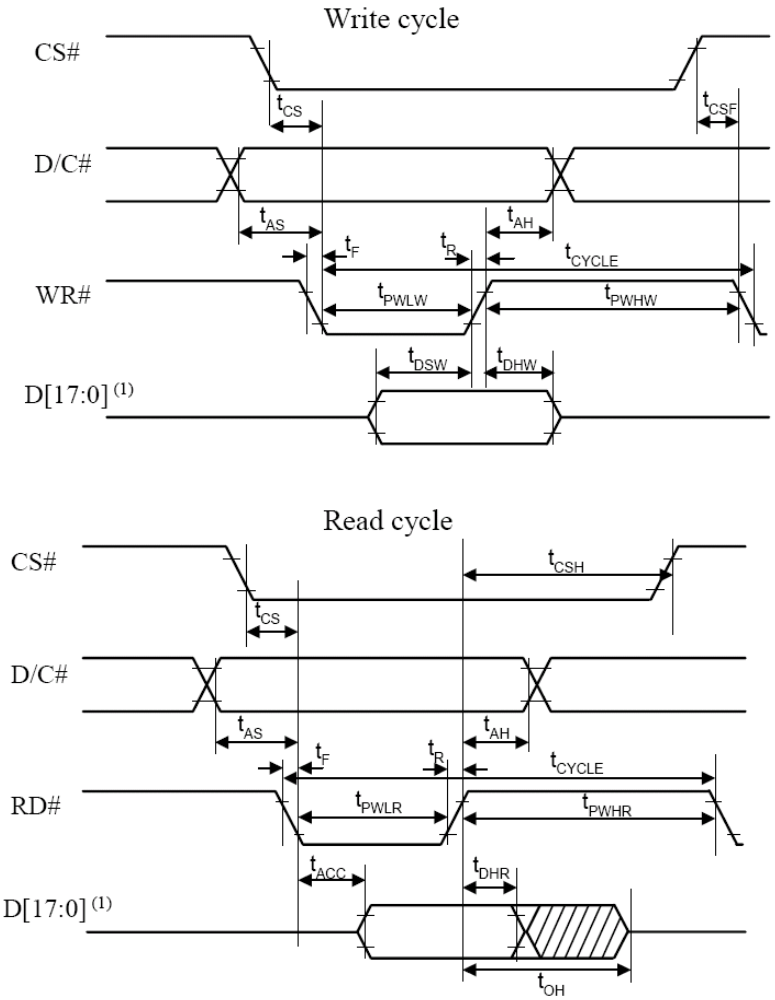


(2)8080-Series MPU Parallel Interface Timing Characteristics

(V_{DD} - V_{SS} = 2.4 to 2.6V, V_{DDIO}=1.6V, V_{CI} = 2.8V, T_A = 25°C)

Symbol	Parameter	Min	Typ	Max	Unit
t_{CYCLE}	Clock Cycle Time	300	-	-	ns
t_{AS}	Address Setup Time	10	-	-	ns
t_{AH}	Address Hold Time	0	-	-	ns
t_{DSW}	Write Data Setup Time	40	-	-	ns
t_{DHW}	Write Data Hold Time	7	-	-	ns
t_{DHR}	Read Data Hold Time	20	-	-	ns
t_{OH}	Output Disable Time	-	-	70	ns
t_{ACC}	Access Time	-	-	140	ns
t_{PWLR}	Read Low Time	150	-	-	ns
t_{PWLW}	Write Low Time	60	-	-	ns
t_{PWHR}	Read High Time	60	-	-	ns
t_{PWHW}	Write High Time	60	-	-	ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns
t_{CS}	Chip select setup time	0	-	-	ns
t_{CSH}	Chip select hold time to read signal	0	-	-	ns
t_{CSF}	Chip select hold time	20	-	-	ns

8800-series MCU parallel interface characteristics

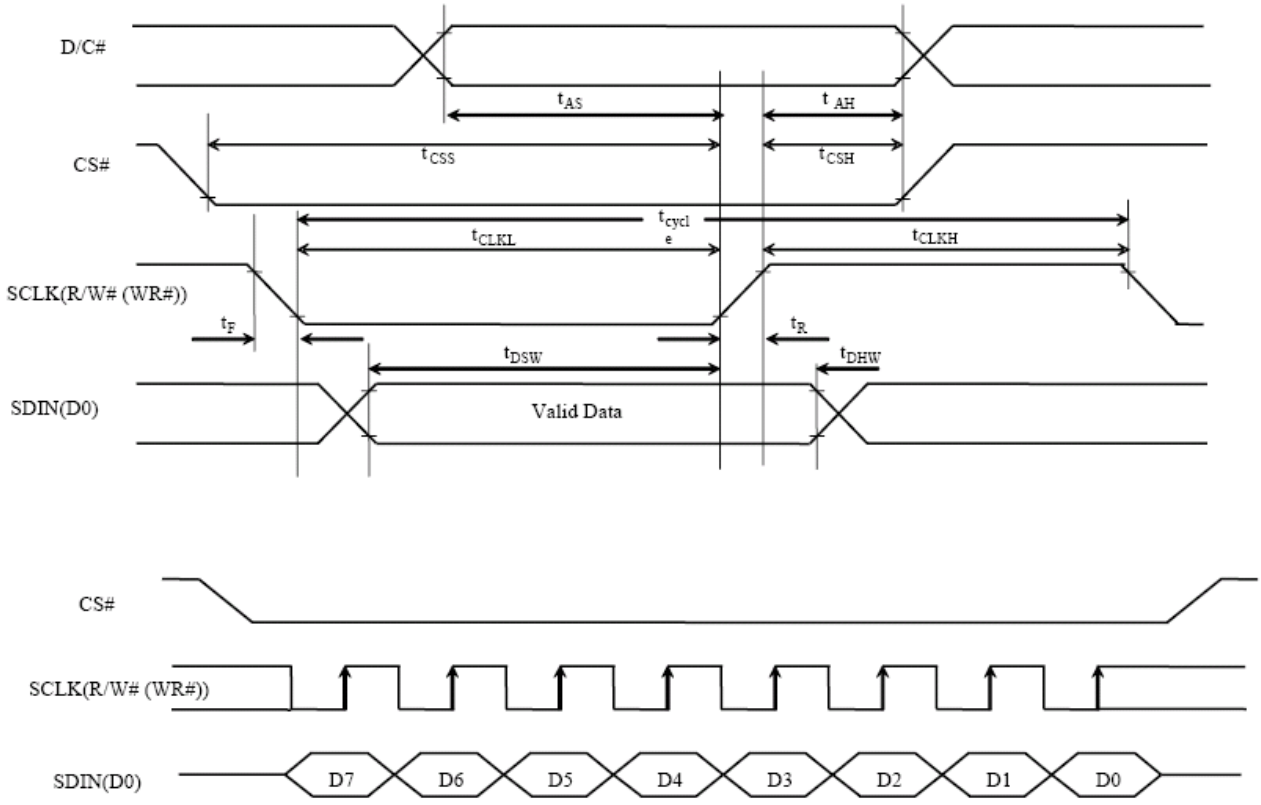


(3)Serial Interface Timing Characteristics(4-wire SPI)

(V_{DD} - V_{SS} = 2.4 to 2.6V, V_{DDIO}=1.6V, V_{CI} = 2.8V, T_A = 25°C)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	50	-	-	ns
t_{AS}	Address Setup Time	15	-	-	ns
t_{AH}	Address Hold Time	15	-	-	ns
t_{CSS}	Chip Select Setup Time	20	-	-	ns
t_{CSH}	Chip Select Hold Time	10	-	-	ns
t_{DSW}	Write Data Setup Time	15	-	-	ns
t_{DHW}	Write Data Hold Time	15	-	-	ns
t_{CLKL}	Clock Low Time	20	-	-	ns
t_{CLKH}	Clock High Time	20	-	-	ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns

Serial interface characteristics(4-wire SPI)

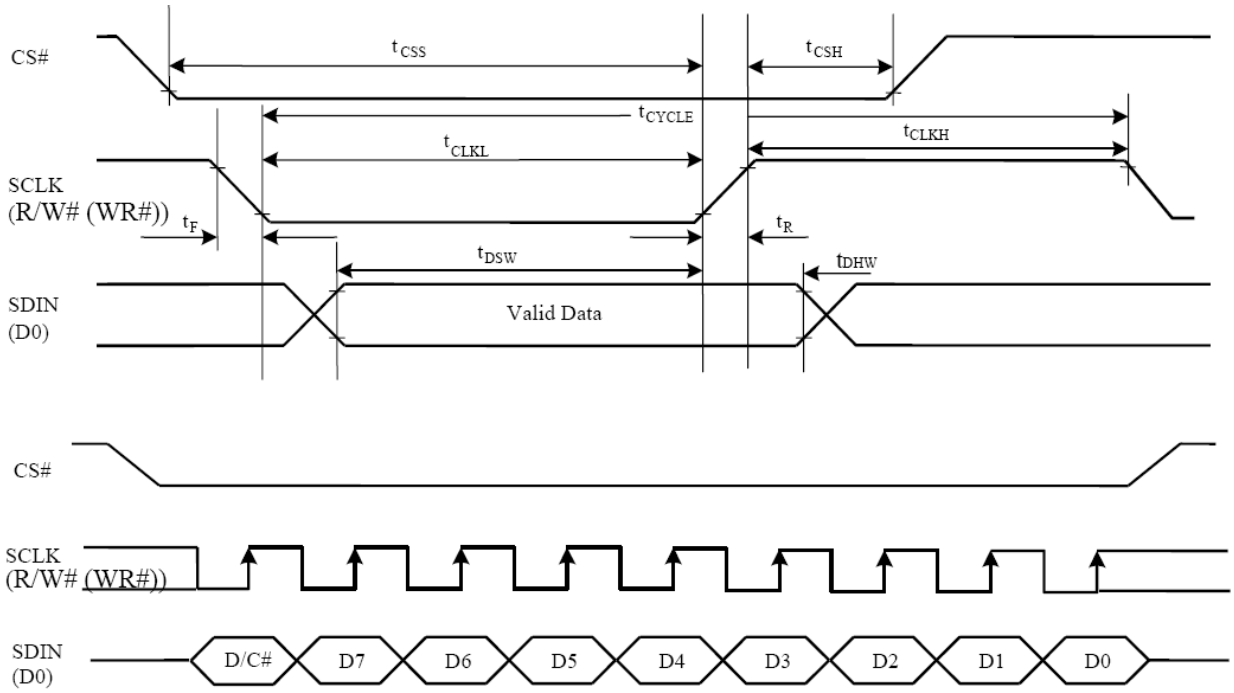


(4)Serial Interface Timing Characteristics(3-wire SPI)

(V_{DD} - V_{SS} = 2.4 to 2.6V, V_{DDIO}=1.6V, V_{CI} = 2.8V, T_A = 25°C)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	50	-	-	ns
t_{CSS}	Chip Select Setup Time	20	-	-	ns
t_{CSH}	Chip Select Hold Time	10	-	-	ns
t_{DSW}	Write Data Setup Time	15	-	-	ns
t_{DHW}	Write Data Hold Time	15	-	-	ns
t_{CLKL}	Clock Low Time	20	-	-	ns
t_{CLKH}	Clock High Time	20	-	-	ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns

Serial interface characteristics(3-wire SPI)



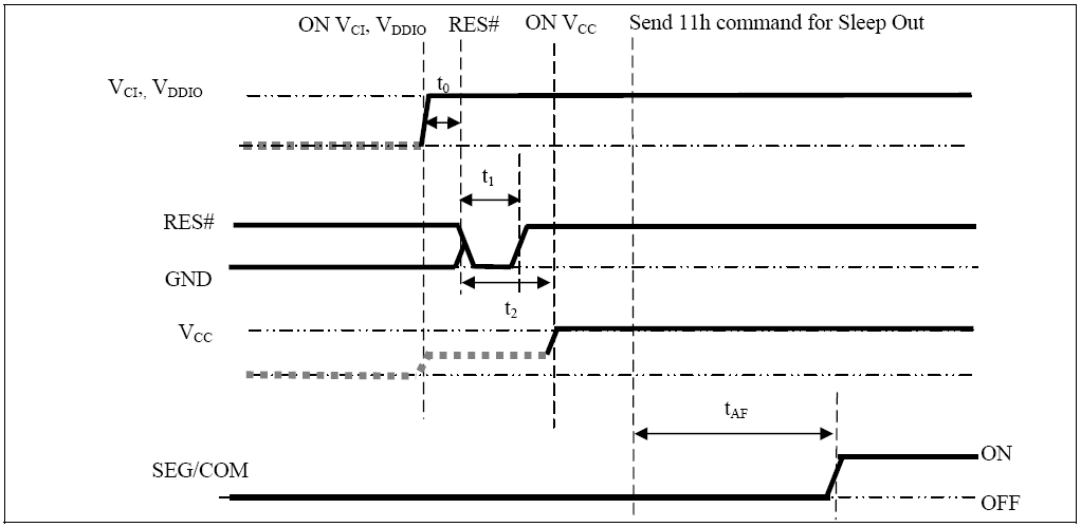
9 Functional Specification and Application Circuit

9.1 Power ON and Power OFF Sequence

The following figures illustrate the recommended power ON and power OFF sequence of SSD1355 (assume VCI and VDDIO are at the same voltage level and internal VDD is used).

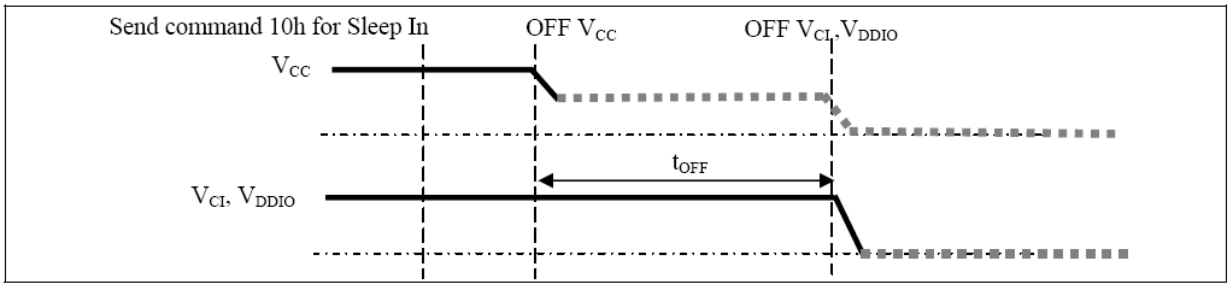
Power ON Sequence:

1. Power ON VCI, VDDIO.
2. After VCI, VDDIO become stable, set wait time at least 1ms (t0) for internal VDD become stable.Then set RES# pin LOW (LOGIC LOW) for at least 2us (t1)[4] and then HIGH (logic high).
3. After set RES# pin LOW (logic low), wait for at least 2us (t_2). Then Power ON VCC. [1]
4. After VCC become stable, send command 11h for Sleep Out. SEG/COM will be ON after 200ms(t_{AF}).



Power OFF Sequence:

1. Send command 10h for Sleep In
2. Power OFF VCC.[1], [2] , [3]
4. Wait for t_{OFF}. Power OFF VCI, VDDIO. (where Minimum t_{OFF}=0ms[5], Typical t_{OFF}=100ms)



Note:

(1) Since an ESD protection circuit is connected between VCI,VDDIO and VCC, VCC becomes lower than VCI whenever VCI, VDDIO is ON and Vcc is OFF as shown in the dotted line of VCC in above figures.

(2).VCC should be kept float (disble) when it is OFF.

(3). Power Pins (VDD , VCC) can never be pulled to ground under any circumstance.

(4). The register values are reset after t_1.

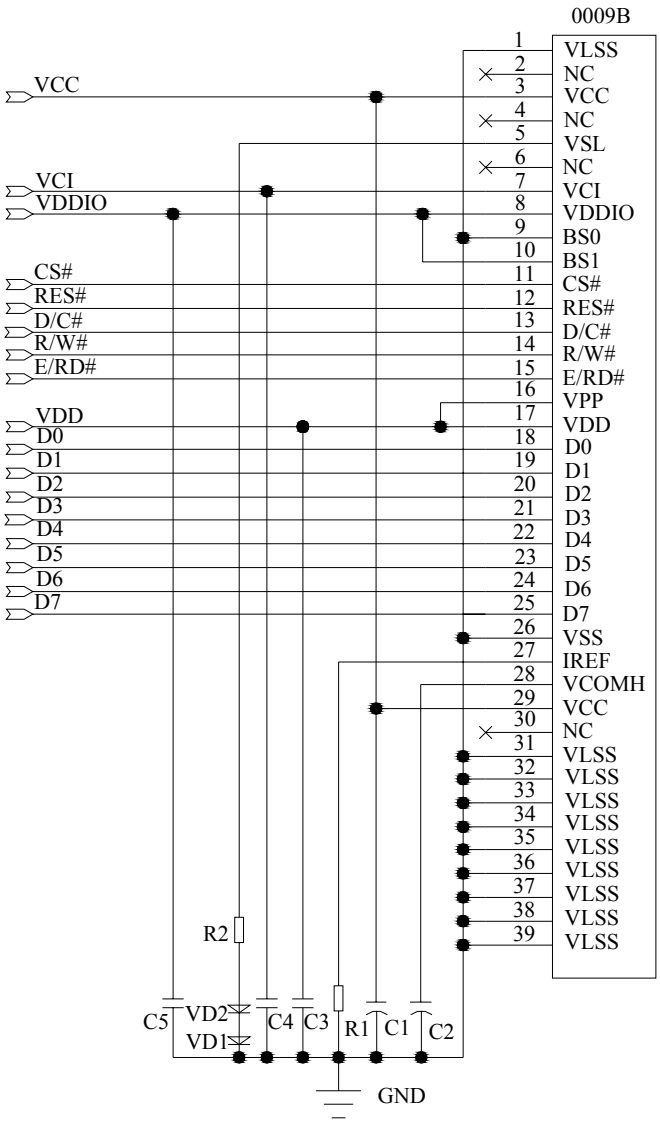
(5). VCI, VDDIO should not be Power OFF before VCC Power OFF.

9.2 Application Circuit

The double byte command for 0XB3 is used to enable or disable the VDD regulator. No matter VDD is supplied by external source or internal regulated ; VCI must always be set equivalent to or higher than VDD.

(A) 、VDD can be supplied externally (with the range of 2.4V to 2.6V, VCI must always be set equivalent to or higher than VDD.) when A[0] is set to 0b.

(1). The configuration for 8-bit 8080-parallel interface mode.



Write_c(0x36) //memory access control
Write_d(0x00)
Write_d(0x01)

Pin connected to MCU interface: D[7:0], E/RD#, R/W#, D/C#, RES#, CS#

Recommended components

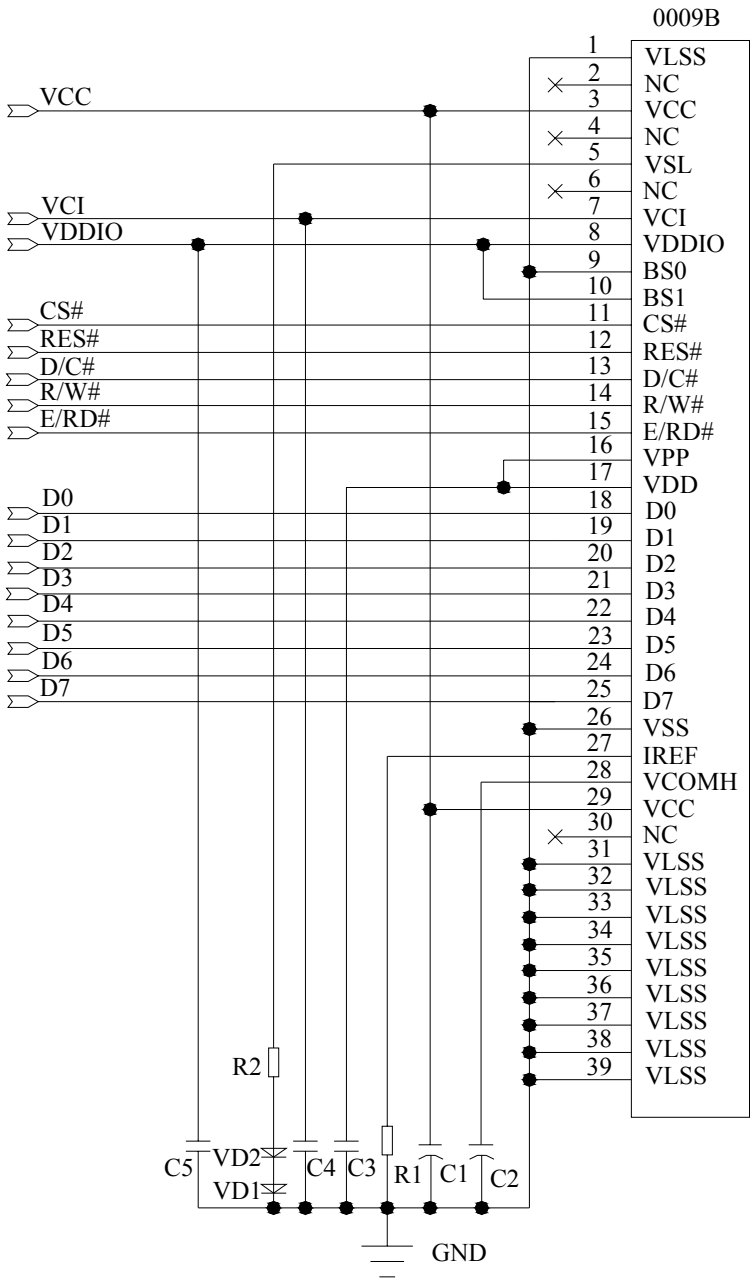
C1, C2,: 4.7μF/25V.ROHS (Tantalum Capacitors) C3,C4,C5: 0.1uF-0603-X7R±10%.ROHS

R1: 0603 1/10W +/-5% 1.2M ohm.ROHS R2: 0603 1/10W +/-5% 51 ohm.ROHS

VD1,VD2:LL4148

(B)、VDD can be supplied regulated internally from VCI when A[0] is set to 1b.
(VCI must be > 2.6V)

(1). The configuration for 8-bit 8080-parallel interface mode.



Write_c(0x36) //memory access control
Write_d(0x00)
Write_d(0x01)

Pin connected to MCU interface: D[7:0], E/RD#, R/W#, D/C#, RES#, CS#

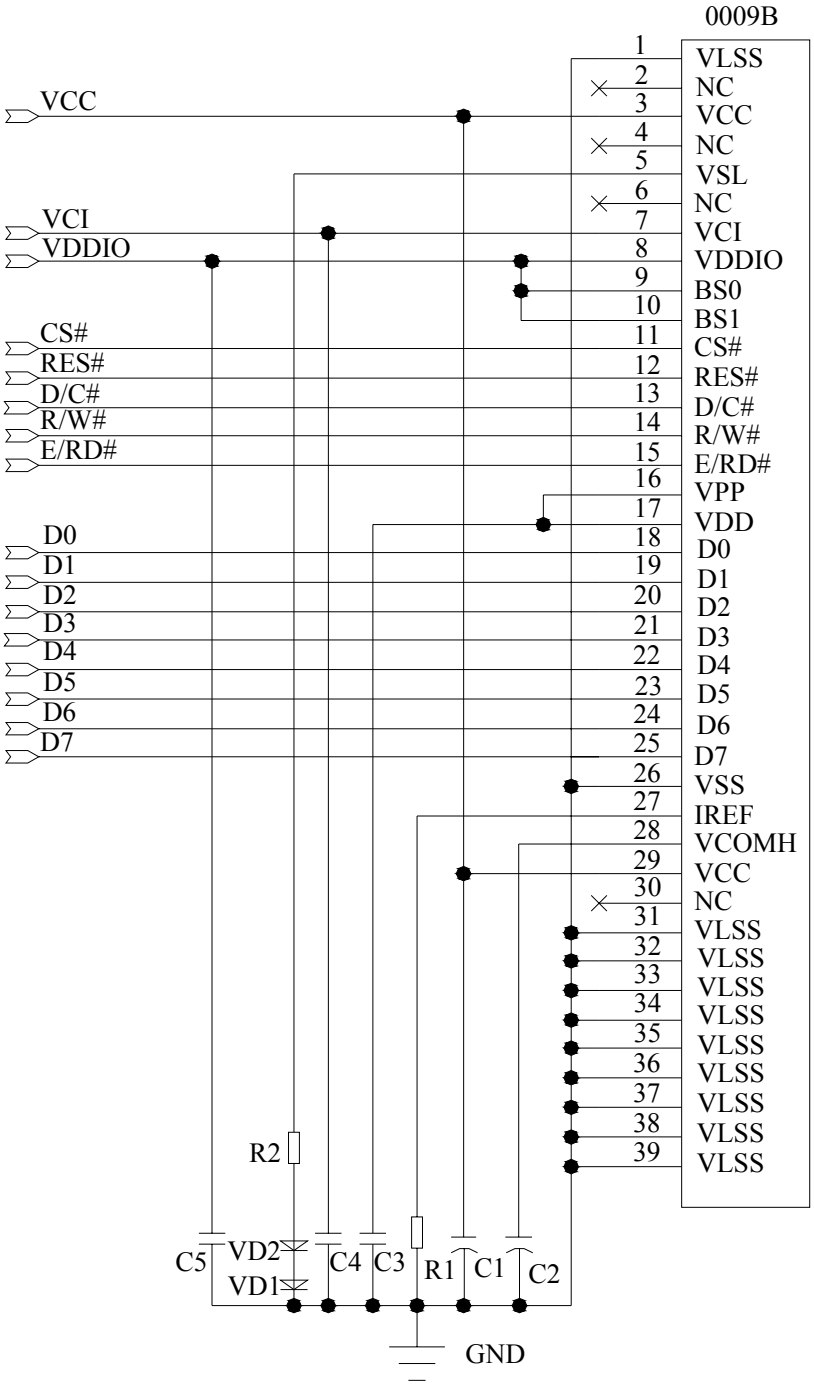
Recommended components

C1, C2,: 4.7μF/25V.ROHS (Tantalum Capacitors) C3,C4,C5: 1uF-0603-X7R±10%.ROHS

R1: 0603 1/10W +/-5% 1.2M ohm.ROHS R2: 0603 1/10W +/-5% 51 ohm.ROHS

VD1,VD2:LL4148

(2). The configuration for 8-bit 6800-parallel interface mode.



Write_c(0x36) //memory access control
Write_d(0x00)
Write_d(0x01)

Pin connected to MCU interface: D[7:0], E/RD#, R/W#, D/C#, RES#, CS#

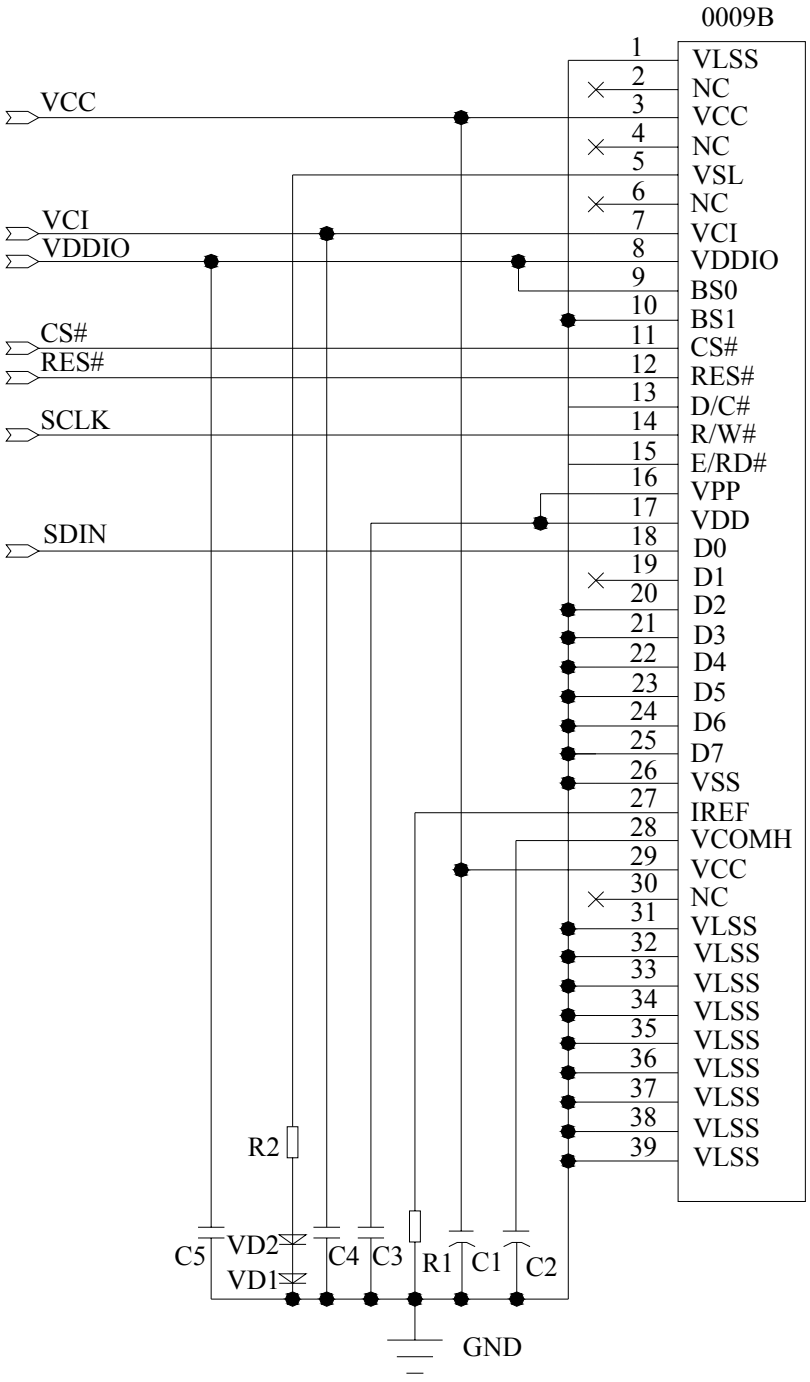
Recommended components

C1, C2,: 4.7μF/25V.ROHS (Tantalum Capacitors) C3,C4,C5: 1uF-0603-X7R±10%.ROHS

R1: 0603 1/10W +/-5% 1.2M ohm.ROHS R2: 0603 1/10W +/-5% 51 ohm.ROHS

VD1,VD2:LL4148

(3). The configuration for 3-wire SPI interface mode.




```
Write_c(0x36)          //memory access control
Write_d(0x00)
Write_d(0x01)
```

Pin connected to MCU interface: SDIN,SCLK,, RES#, CS#

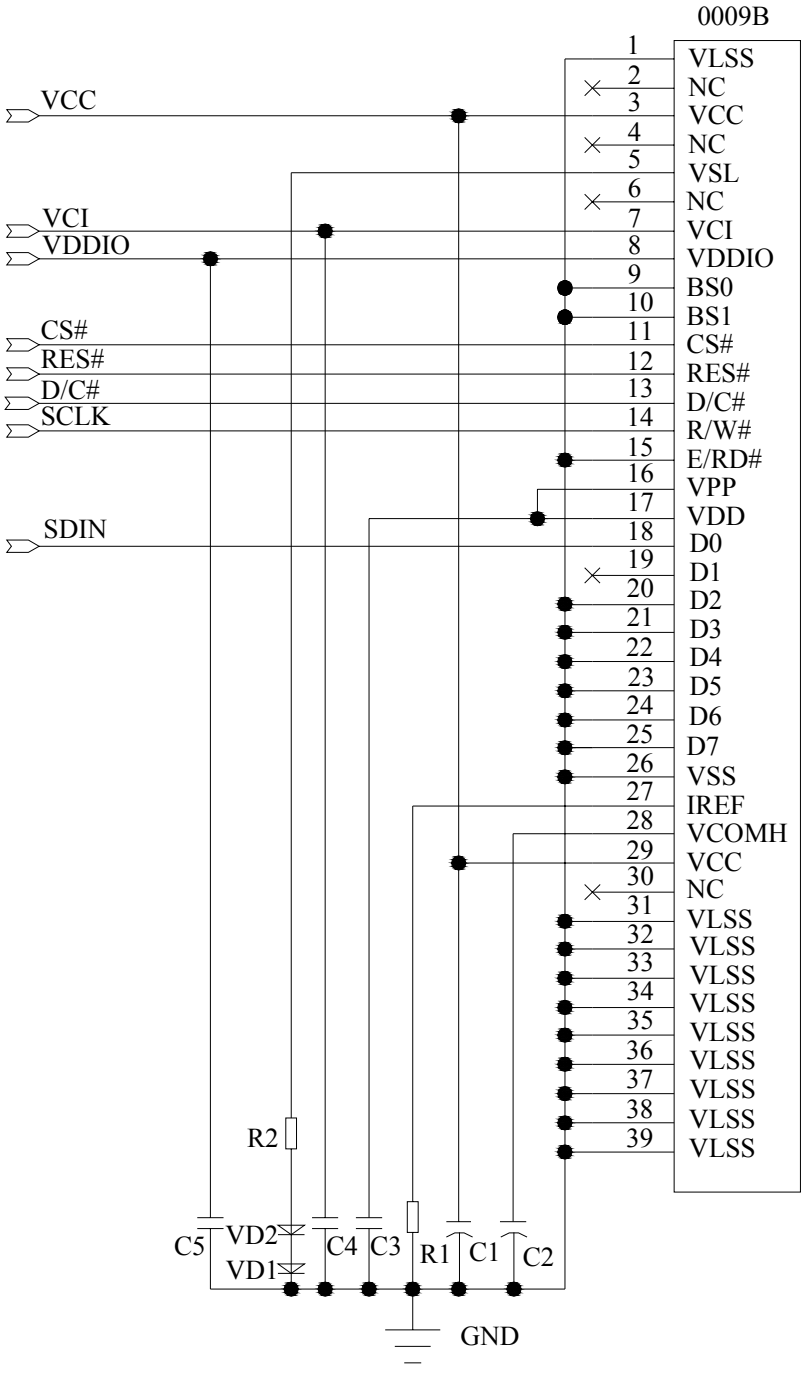
Recommended components

C1, C2,: 4.7μF/25V.ROHS (Tantalum Capacitors) C3,C4,C5: 1uF-0603-X7R±10%.ROHS

R1: 0603 1/10W +/-5% 1.2M ohm.ROHS R2: 0603 1/10W +/-5% 51 ohm.ROHS

VD1,VD2:LL4148

(4). The configuration for 4-wire SPI interface mode.



Write_c(0x36) //memory access control
Write_d(0x00)
Write_d(0x01)

Pin connected to MCU interface: SDIN,SCLK, D/C#, RES#, CS#

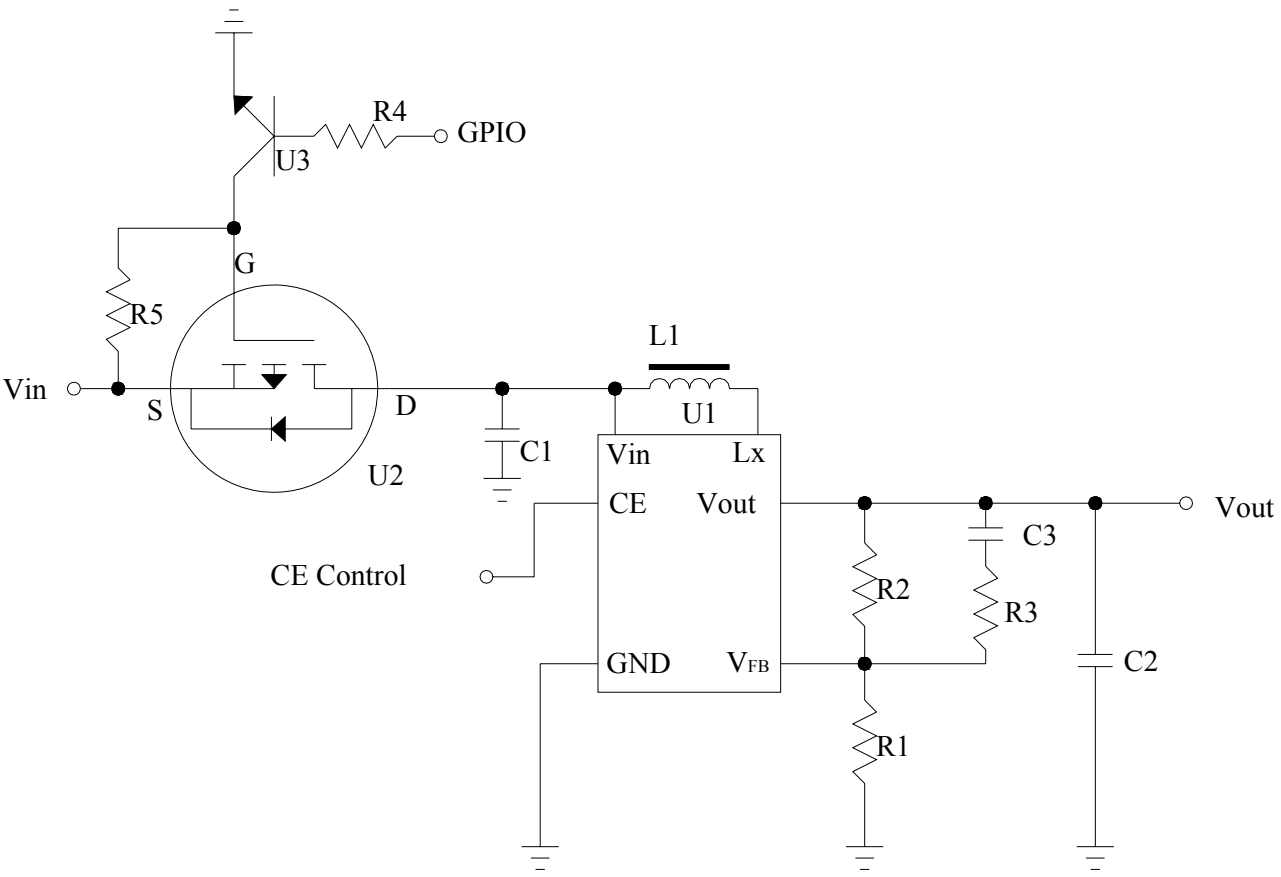
Recommended components

C1, C2,: 4.7μF/25V.ROHS (Tantalum Capacitors) C3,C4,C5: 1uF-0603-X7R±10%.ROHS

R1: 0603 1/10W +/-5% 1.2M ohm.ROHS R2: 0603 1/10W +/-5% 51 ohm.ROHS

VD1,VD2:LL4148

9.3 External DC-DC application circuit



Recommend component

The C1	: 1 uF-0603-X7R±10%.ROHS
The C2	: 1 uF-0603-X7R±10%.ROHS
The C3	: 220pF-0603-X7R±10%.ROHS
The R1	: 0603 1/10W +/-5% 10Kohm.ROHS
The R2	: 0603 1/10W +/-1% 154Kohm.ROHS
The R3	: 0603 1/10W +/-5% 2Kohm.ROHS
The R4	: 0603 1/10W +/-5% 1Kohm.ROHS
The R5	: 0603 1/10W +/-5% 10Kohm.ROHS
The L1	: 22uH
The U1	: R1200
The U2	: FDN338P
The U3	: 8050

9.4 Display Control Instruction

Refer to SSD1355U8R1 Specification.

9.5 Recommended Software Initialization

```
void init_SSD1355()
{
      cs=0;
      res=0;
      shortdelay(10);
      res=1;
      write_c(0x01);            //software reset
      write_c(0xfd);            //Command lock
      write_d(0xb3);
      write_c(0xcc);            //set VSL discharge path
      write_d(0xb0);
      write_d(0x16);
      write_c(0x11);            //sleep out
      write_c(0x13);            //normal display
      write_c(0x20);            //
     write_c(0x29);             //disable all pixels off/on
      write_c(0x2a);            //set coluum address
      write_d(0x00);
      write_d(0x7f);
      write_c(0x2b);            //set row address
      write_d(0x00);
      write_d(0x7f);
      write_c(0x34);            //disable tearing effect
      write_c(0x36);            //memory access control
      write_d(0x00);
      write_d(0x01);
      write_c(0x3a);            //interface pixel format
      write_d(0x06);
      write_c(0x51);            //write luminance
      write_d(0xf0);
      write_c(0xb3);            //function selection
      write_d(0x01);            //
      write_c(0xba);            //set contrast of R
      write_d(0xc8);            //
      write_c(0xbb);            //set contrast of G
```

```
write_d(0x55);          //
write_c(0xbc);          //set contrast of B
write_d(0x99);          //
write_c(0xbd);          //set first pre-charge voltage
write_d(0x1f);          //
write_c(0xc8);          //set display offset
write_d(0x00);          //
write_c(0xca);          //set mux ratio
write_d(0x7f);
write_c(0xcd);          //set phase length
write_d(0x55);          //
write_c(0xce);          //set second precharge period
write_d(0x07);          //
write_c(0xcf);          //set second precharge speed
write_d(0x02);          //
write_c(0xbe);
write_d(1);
write_d(2);
write_d(3);
write_d(4);
write_d(5);
write_d(6);
write_d(7);
write_d(8);
write_d(9);
write_d(10);
write_d(11);
write_d(12);
write_d(13);
write_d(14);
write_d(15);
write_d(17);
write_d(19);
write_d(23);
write_d(27);
write_d(31);
write_d(35);
write_d(39);
```

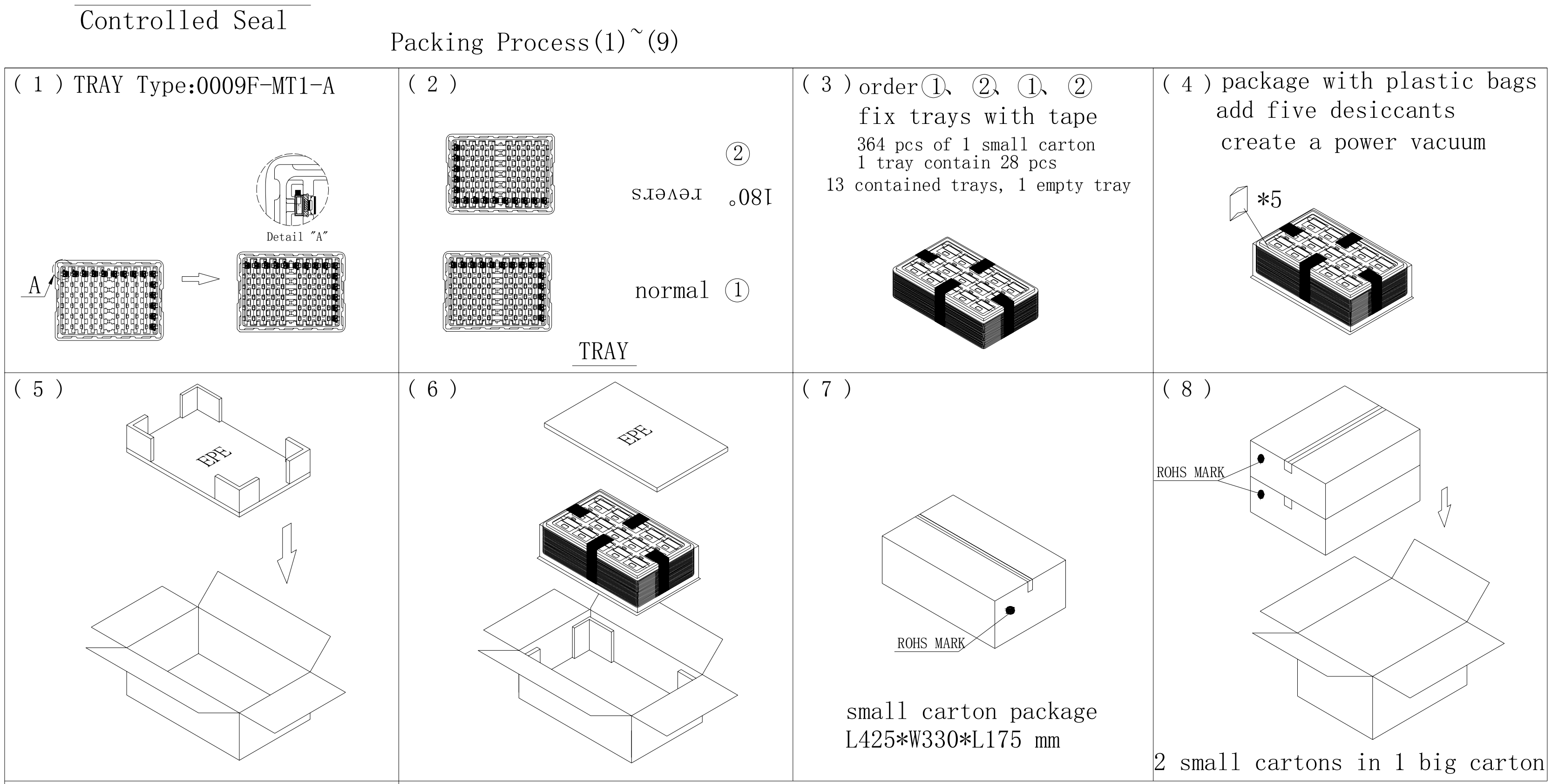
```
        write_d(47);
        write_d(53);
        write_d(63);
        write_d(73);
        write_d(83);
        write_d(93);
        write_d(99);
        write_d(109);
        write_d(117);
        write_d(127);
    //G
        write_d(2);
        write_d(3);
        write_d(4);
        write_d(5);
        write_d(7);
        write_d(9);
        write_d(11);
        write_d(13);
        write_d(15);
        write_d(17);
        write_d(19);
        write_d(27);
        write_d(33);
        write_d(37);
        write_d(41);
        write_d(45);
        write_d(49);
        write_d(53);
        write_d(57);
        write_d(61);
        write_d(65);
        write_d(69);
        write_d(73);
        write_d(79);
        write_d(85);
        write_d(91);
        write_d(97);
```

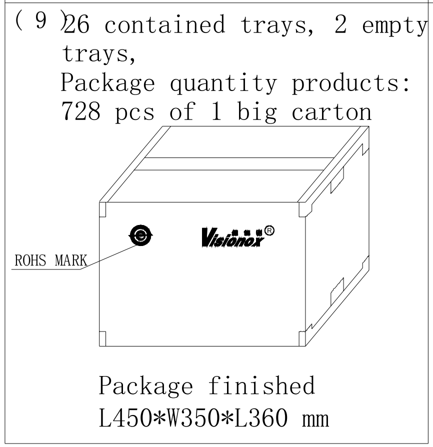
```
        write_d(103);
        write_d(109);
        write_d(115);
        write_d(121);
        write_d(127);
    //B
        write_d(1);
        write_d(2);
        write_d(3);
        write_d(4);
        write_d(5);
        write_d(6);
        write_d(7);
        write_d(8);
        write_d(9);
        write_d(10);
        write_d(11);
        write_d(12);
        write_d(13);
        write_d(14);
        write_d(15);
        write_d(17);
        write_d(19);
        write_d(23);
        write_d(27);
        write_d(31);
        write_d(35);
        write_d(39);
        write_d(47);
        write_d(53);
        write_d(63);
        write_d(73);
        write_d(83);
        write_d(93);
        write_d(99);
        write_d(109);
        write_d(117);
        write_d(127);
```

```
        write_c(0xd2);          //set display colck divider/oscillator frequency
        write_d(0x30);          //
        write_c(0xd3);          //set Vcomh
        write_d(0x00);
        write_c(0xd7);          //GPIO
        write_d(0x00);

}
```

10 Package Specification





NOTE:1、The inner carton and master carton must be sealed with adhesive tape.

2、Fill up the gap with EPE.

3、If the customer has special needs with the RoHS making, the inner carton and master carton need adhesive new RoHS marking at ⊜ .

11 Reliability

11.1 Reliability Test

NO.	ITEM	CONDITION	QUANTITY
1	High Temperature (Non-operation)	85℃,240hrs	4
2	Low Temperature (Non-operation)	-40℃,240hrs	4
3	High Temperature (Operation)	70℃,240hrs	4
4	Low Temperature (Operation)	-40℃,240hrs	4
5	High Temperature / High Humidity (Operation)	60℃,90%RH,240hrs	4
6	Thermal shock (Non-operation)	-40℃~85℃(-40℃/30min;transit/3min;85℃/30min;transit/3min) 1cycle: 66min,30cycles	4
7	Vibration	Frequency: 5~50Hz,0.5G Scan rate: 1 oct/min Time: 2 hrs/axis Test axis: X,Y, Z	1 Carton
8	Drop	Height: 100 cm Sequence: 1 angle, 3 edges and 6 faces	1 Carton

Test and measurement conditions

1. All measurements shall not be started until the specimens attain to temperature stability, the stable time is at least 15 minutes.
2. The degradation of polarizer is ignored for item 5.
3. The tolerance of temperature is ±3℃, and the tolerance of relative humidity is ±5%.

Evaluation criteria

1. The function test is OK.
2. No observable defects.
3. Luminance:≥50% of initial value.
4. Current consumption: within ± 50% of initial value.

11.2 Lifetime

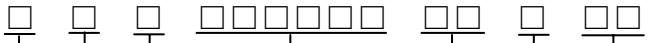
End of lifetime is specified as 50% of initial brightness and the test pattern at operating condition is 50% alternating checkerboard.

ITEM	MIN	MAX	UNIT	CONDITION
Operation Life Time	10,000	-	hrs	80cd/m^2, 50% alternating checkerboard, 22±3°C, 55±15% RH

11.3 Failure Check Standard

After the completion of the described reliability test, the samples were left at room temperature for 2 hrs prior to conducting the failure test at 22±3°C; 55±15% RH.

12 Illustration of OLED Product Name



Flow No. :

01~99

Display Color :

R—red

G—green

B—blue

Y—yellow

W—white

A—area color

F—full color

Panel Flow No. :

A0~A9, B0~B9…Z0~Z9

Display Format :

Graphic—columns and rows

Character—characters and line number

Segment—segment number

Icon—pixel number

Product Type :

P—panel

M—module

Display Type :

G—graphic

C—character

S—segment

I—Icon

M—mixed

Company :

V—Visionox

13 Outgoing Quality Control Specifications

13.1 Sampling Method

(1) GB/T 2828.1-2003/ISO2859-1：1999, inspection level Ⅱ, normal inspection, single sample inspection

(2) AQL: Major 0.65; Minor 1.0

13.2 Inspection Conditions

The environmental conditions for test and measurement are performed as follows.

Temperature: 22±3°C

Humidity: 55±15%R.H

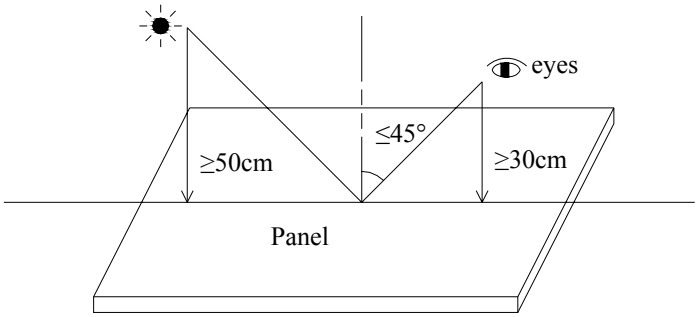
Fluorescent Lamp: 30W

Distance between the Panel & Lamp: ≥50cm

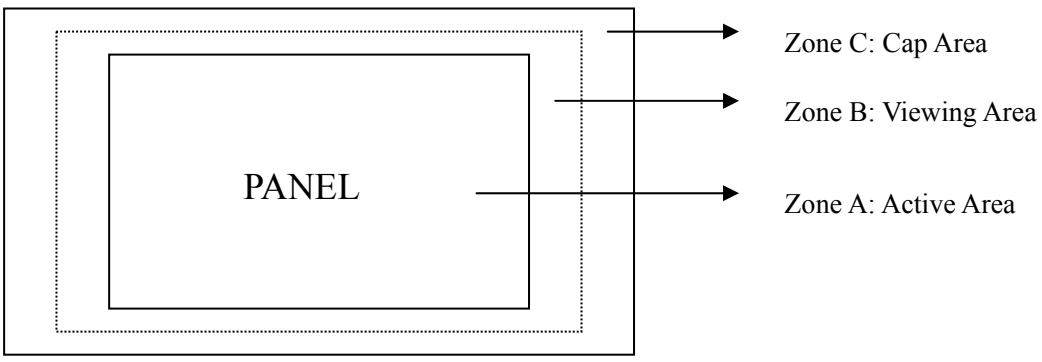
Distance between the Panel & Eyes: ≥30cm

Viewing angle from the vertical in each direction: ≤45°

(See the sketch below)

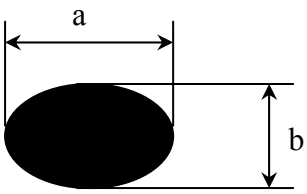


13.3 Quality Assurance Zones

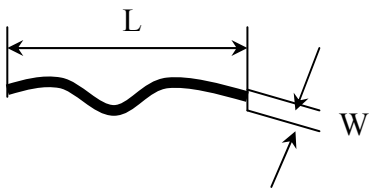


13.4 Inspection Standard

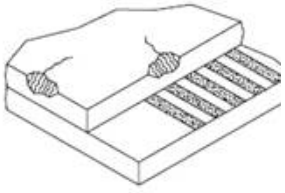
Definition of Φ&L&W (Unit: mm)

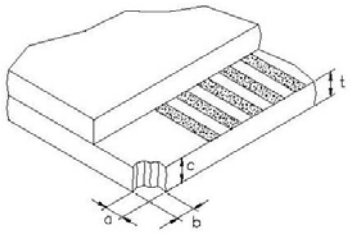
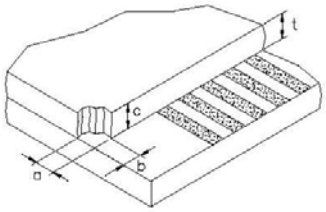
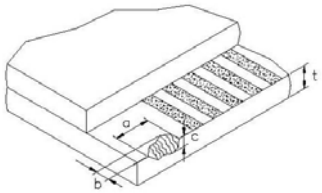
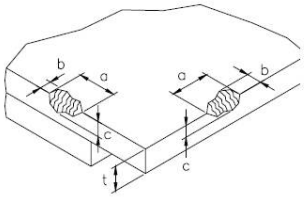
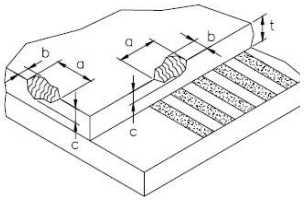


Φ=(a+b)/2



Ⅰ. Appearance Defects

<table>
<tr><th>NO.</th><th>ITEM</th><th>CRITERIA</th><th>CLASSIFICATION</th></tr>
<tr><td>1</td><td>Polarizer Black or White spot, Dirty spot, Foreign matter, Dent on the polarizer</td><td>
<table>
<tr><td rowspan="2">Average Diameter (mm)</td><td colspan="2">Acceptable Number</td></tr>
<tr><td>Zone A,B</td><td>Zone C</td></tr>
<tr><td>Φ≤0.15</td><td>Ignore</td><td rowspan="3">Ignore</td></tr>
<tr><td>0.15<Φ≤0.30</td><td>3</td></tr>
<tr><td>Φ>0.30</td><td>0</td></tr>
</table>
</td><td>Minor</td></tr>
<tr><td>2</td><td>Scratch/line on the glass/Polarizer</td><td>
<table>
<tr><td rowspan="2">Width (mm)</td><td rowspan="2">Length (mm)</td><td colspan="2">Acceptable Number</td></tr>
<tr><td>Zone A,B</td><td>Zone C</td></tr>
<tr><td>W≤0.03</td><td>---</td><td>Ignore</td><td rowspan="3">Ignore</td></tr>
<tr><td>0.03<W≤0.08</td><td>L≤5.0</td><td>3</td></tr>
<tr><td>W>0.08</td><td>---</td><td>0</td></tr>
</table>
</td><td>Minor</td></tr>
<tr><td>3</td><td>Polarizer Bubble</td><td>
<table>
<tr><td rowspan="2">Average Diameter (mm)</td><td colspan="2">Acceptable Number</td></tr>
<tr><td>Zone A,B</td><td>Zone C</td></tr>
<tr><td>Φ>0.5</td><td>0</td><td rowspan="3">Ignore</td></tr>
<tr><td>0.2<Φ≤0.5</td><td>3</td></tr>
<tr><td>Φ≤0.2</td><td>Ignore</td></tr>
</table>
</td><td>Minor</td></tr>
<tr><td>4</td><td>Any Dirt & Scratch on Polarizer’s Protective Film</td><td>Ignore for not affect the polarizer.</td><td>Acceptable</td></tr>
<tr><td>5</td><td>Glass Crack</td><td>  Propagation crack is not acceptable.</td><td>Major</td></tr>
</table>

6	Corner Chip	 t= Glass thickness Accept a≤2.0mm or b≤2.0mm, c≤t	Minor
7	Corner Chip on Cap Glass	 t= Glass thickness Accept a≤1.5mm or b≤1.5mm, c≤t	Minor
8	Chip on Contact Pad	 t= Glass thickness Accept a≤3.0mm or b≤0.8mm, c≤t (on the contact pin) a≤3.0mm or b≤1.5mm, c≤t (outside of the contact pin)	Minor
9	Chip on Face of Display	 t= Glass thickness Accept a≤1.5mm or b≤1.5mm, c≤t	Minor
10	Chip on Cap Glass	 t= Glass thickness Accept a≤3.0mm or b≤3.0mm, c≤t/2 a≤1.5mm or b≤1.5mm, t/2≤c≤t	Minor
11	Stain on Surface	Stain removable by soft cloth or air blow is acceptable.	Minor
12	TCP/FPC Damage	(1) Crack, deep scratch, deep hole and deep pressure mark on the TCP/FPC are not acceptable. (2) Terminal lead twisted or broken is not allowable. (3) Copper exposed is not allowed by naked eye inspection.	Minor
13	Dimension Unconformity	Checking by mechanical drawing.	Major

Ⅱ. Displaying Defects

<table>
<tr><th>NO.</th><th>ITEM</th><th>CRITERIA</th><th>CLASSIFICATION</th></tr>
<tr><td>1</td><td>Black/White spot
Dirty spot
Foreign matter</td><td>
<table>
<tr><td rowspan="2">Average Diameter (mm)</td><td colspan="2">Pieces Permitted</td></tr>
<tr><td>Zone A,B</td><td>Zone C</td></tr>
<tr><td>Φ≤0.10</td><td>Ignore</td><td rowspan="3">Ignore</td></tr>
<tr><td>0.10<Φ≤0.20</td><td>3</td></tr>
<tr><td>Φ>0.20</td><td>0</td></tr>
</table>
</td><td>Minor</td></tr>
<tr><td>2</td><td>No Display</td><td>Not allowable.</td><td>Major</td></tr>
<tr><td>3</td><td>Irregular Display</td><td>Not allowable.</td><td>Major</td></tr>
<tr><td>4</td><td>Missing Line
(row or column)</td><td>Not allowable.</td><td>Major</td></tr>
<tr><td>5</td><td>Short</td><td>Not allowable.</td><td>Major</td></tr>
<tr><td>6</td><td>Flicker</td><td>Not allowable.</td><td>Major</td></tr>
<tr><td>7</td><td>Abnormal Color</td><td>Refer to the SPEC.</td><td>Major</td></tr>
<tr><td>8</td><td>Luminance NG</td><td>Refer to the SPEC.</td><td>Major</td></tr>
<tr><td>9</td><td>Over Current</td><td>Refer to the SPEC.</td><td>Major</td></tr>
</table>

14 Precautions for operation and Storage

14.1 Precautions for Operation

(1) Since OLED panel is made of glass, do not apply any mechanical shock or impact or excessive force to it when installing the OLED module. Any strong mechanical impact due to falling dropping etc. may cause damage (breakage or cracking).

(2) The polarizer on the OLED surface is made of soft material and is easily scratched. Please take most care when handing. When the surface of the polarizer of OLED Module is contaminated, please wipe it off gently by using moisten soft cloth with isopropyl alcohol, do not use water, ketone or aromatics. If there is saliva or water on the OLED surface, please wipe it off immediately.

(3) When handling OLED module, please be sure that the body and the tools are properly grounded. And do not touch I/O pins with bare hands or contaminate I/O pins, it will cause disconnection or defective insulation of terminals.

(4) Do not attempt to disassemble or process the OLED module.

(5) OLED module should be used under recommended operating conditions shown in the specification. Since the higher voltage leads to the shorter lifetime, be sure to use the specified operating voltage.

(6) Foggy dew, moisture condensation or water droplets deposited on surface and contact terminals will cause polarizer stain or damage, the deteriorated display quality and electrochemical reaction then leads to shorter life time and permanent damage to the module probably. Please pay attention to the environmental temperature and humidity.

(7) An afterimage is created by the difference in brightness between unused dot and the fixed dot, according to the decrease of brightness of the emitting time. Therefore, to avoid having an afterimage, the full set should be thoroughly used instead of using a fixed dot. When the fixed dot emits, an afterimage can be created.

(8) Flicker could be come out at full on display. And it disappears when frame frequency increase, but brightness decreases too.

14.2 Soldering

(1) Soldering should be performed only on the I/O terminals.

(2) Use soldering irons with proper grounding and no leakage.

(3) Iron: no higher than 300℃ and 3~4 sec during soldering.

14.3 Precautions for Storage

(1) Please store OLED module in a dark place. Avoid exposure to sunlight, the light of fluorescent lamp or any ultraviolet ray.

(2) Keep the environment temperature between 10℃ and 35℃ and the relative humidity less than 60%. Avoid high temperature and high humidity.

(3) Keep the OLED modules stored in the container when shipped from supplier before using them is recommended.

(4) Do not leave any article on the OLED module surface for an extended period of time.

14.4 Warranty period

Visionox Display Co., Ltd. warrants for a period of 12 months from the shipping date when stored or used under normal condition.