

SATA Slim

D150Q Series

Customer: _____

Customer

Part Number: _____

InnoDisk

Part Number: _____

InnoDisk

Model Name: _____

Date: _____

| InnoDisk Approver | Customer Approver |
|--------------------------|--------------------------|
| | |

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industrial flash storage

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REVISION HISTORY

| Revision | Description | Date |
|-------------|--|------------|
| Preliminary | First Released | March 2011 |
| Rev. 1.0 | Modify the performance | April 2011 |
| Rev. 1.1 | Add the device parameters of 2GB and 32GB | May 2011 |
| Rev. 1.2 | Update SMART data structure and weight information | July 2011 |
| Rev. 1.21 | Updated mechanical drawing | AUG, 2012 |
| Rev. 1.3 | Separated into TSOP and BGA versions | AUG, 2012 |
| Rev, 1.4 | Added write protect switch information | SEP, 2012 |

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1. Product Overview

1.1 Introduction of InnoDisk SATA Slim D150Q

InnoDisk SATA Slim D150Q is designed with standard SATA interface (7+15 SATA connector), which could support most platforms with standard SATA port. Besides, with its smaller dimension, SATA Slim D150Q is an alternative solution of 2.5" SSD for those embedded system that may have mechanical and space concerns. InnoDisk SATA Slim D150Q operates under SATA II (3.0Gb/s) protocol with good performance, the sustain read/write can reach up to 130/125MB per second (max).

InnoDisk SATA Slim D150Q is also suitable in industrial field. It effectively reduces the booting time of operation system and the power consumption is less than hard disk drive (HDD). InnoDisk SATA Slim D150Q complies with ATA protocol, no additional drivers are required, and the SATA Slim can be configured as a boot device or data storage device.

1.2 Product View



Figure 1: InnoDisk SATA Slim D150Q (BGA)

1.3 Product Models

InnoDisk SATA Slim D150Q is available in follow capacities.

SATA Slim D150Q BGA 02GB ~ 64GB

1.4 SATA Interface

InnoDisk SATA Slim D150Q support SATA II interface, and compliant with Serial ATA Gen 1 and Gen 2 specification (Gen2 supports 1.5Gbps /3.0Gbps data rate). SATA connector uses a 7-pin signal segment and a 15-pin power segment.

1.5 Capacity

SATA Slim D150Q provides unformatted from 2GB up to 64GB capacities within SLC Flash IC.

2. Theory of operation

2.1 Overview

Figure 2 shows the operation of InnoDisk SATA Slim D150Q from the system level, including the major hardware blocks.

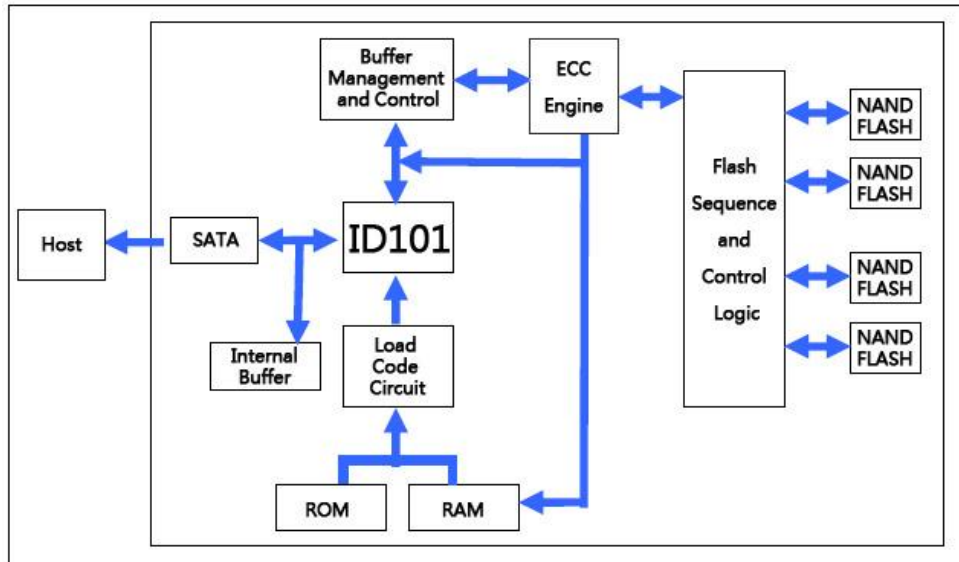


Figure 2: InnoDisk SATA SLIM D150Q Block Diagram

InnoDisk SATA Slim D150Q integrates a SATA II controller and NAND flash memories. Communication with the host occurs through the host interface, using the standard ATA protocol. Communication with the flash device(s) occurs through the flash interface.

2.2 SATA II Controller

The SATA II controller is 3.0 Gbps (Gen. 2), and support hot-plug. The Serial ATA physical, link and transport layers are compliant with Serial ATA Gen 1 and Gen 2 specification (Gen 2 supports 1.5Gbps/3.0Gbps data rate). The controller has 8 channels for flash interface.

The controller is equipped with 96KB of internal memory. 64 KB of memory is used for data buffer, and 32 KB is used for general purpose. The internal memory can also be used as an intermediate memory for storing data blocks during a wear-leveling procedure. There are 40KB of internal memory is used for code. A 10KB internal boot ROM includes basic routines for accessing the flash memories and for loading the main code into the internal memory.

2.3 Error Detection and Correction

Highly sophisticated Error Correction Code algorithms are implemented. The ECC unit consists of the Parity Unit (parity-byte generation) and the Syndrome Unit (syndrome-byte computation). This unit implements an algorithm that can correct 16 bits per 1024 bytes in an ECC block. Code-byte generation during write operations, as well as error detection during read operation, is implemented on the fly without any speed penalties.

2.4 Wear-Leveling

Flash memory can be erased within a limited number of times. This number is called the **erase cycle limit** or **write endurance limit** and is defined by the flash array vendor. The erase cycle limit applies to each individual erase block in the flash device.

InnoDisk SATA Slim D150Q uses a static wear-leveling algorithm to ensure that consecutive writes of a specific sector are not written physically to the same page/block in the flash. This spreads flash media usage evenly across all pages, thereby extending flash lifetime.

2.5 Bad Blocks Management

Bad Blocks are blocks that contain one or more invalid bits whose reliability are not guaranteed. The Bad Blocks may be presented while the SSD is shipped, or may generate during the life time of the SSD. When the Bad Blocks is detected, it will be flagged, and not be used anymore. The SSD implement Bad Blocks management and replacement, Error Correct Code to avoid data error occurred. The functions will be enabled automatically to transfer data from Bad Blocks to spare blocks, and correct error bit. After the reserved block less than 40, the SSD will be locked, and cannot be written anymore.

3. Installation Requirements

3.1 SATA Slim D150Q Pin Directions

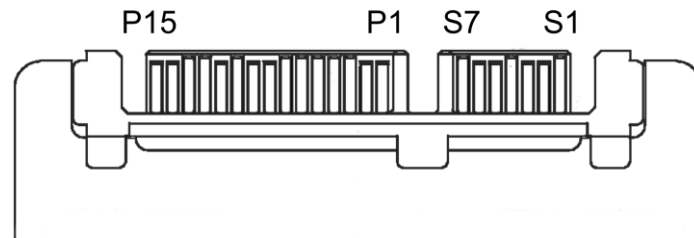


Figure 3: Signal Segment and Power Segment

3.2 Electrical Connections for SATA Slim D150Q

A Serial ATA device may be either directly connected to a host or connected to a host through a cable. For connection via cable, the cable should be no longer than 1 meter. The SATA interface has a separate connector for the power supply. Please refer to the pin description for further details.

3.3 Device drive

No additional device drives are required. The InnoDisk SATA Slim D150Q can be configured as a boot device.

4. Specifications

4.1 CE and FCC Compatibility

InnoDisk SATA Slim D150Q conforms to CE and FCC requirements.

4.2 RoHS Compliance

InnoDisk SATA Slim D150Q is fully compliant with RoHS directive.

4.3 Environmental Specifications

4.3.1 Temperature Ranges

Operating Temperature Range:

- Standard Grade: 0°C ~ +70°C
- Industrial Grade: -40°C ~ +85°C

Storage Temperature Range:

- Standard Grade: -55°C to +95°C

4.3.2 Humidity

Relative Humidity: 10-95%, non-condensing

4.3.3 Shock and Vibration

Table 1: Shock/Vibration Testing for InnoDisk SATA Slim D150Q

| Reliability | Test Conditions | Reference Standards |
|------------------|--------------------------------|---------------------|
| Vibration | 7 Hz to 2K Hz, 20G, 3 axes | IEC 68-2-6 |
| Mechanical Shock | Duration: 0.5ms, 1500G, 3 axes | IEC 68-2-27 |

4.3.4 Mean Time between Failures (MTBF)

Table 2 summarizes the MTBF prediction results for various InnoDisk SATA Slim D150Q configurations. The analysis was performed using a RAM Commander™ failure rate prediction.

- **Failure Rate:** The total number of failures within an item population, divided by the total number of life units expended by that population, during a particular measurement interval under stated condition.
- **Mean Time between Failures (MTBF):** A basic measure of reliability for repairable items: The mean number of life units during which all parts of the item perform within their specified limits, during a particular measurement interval under stated conditions.

Table 2: InnoDisk SATA Slim D150Q MTBF

| Product | Condition | MTBF (Hours) |
|--------------------------|---------------------------|---------------------|
| InnoDisk SATA SLIM D150Q | Telcordia SR-332 GB, 25°C | >4,000,000 |

4.4 Endurance

Data Retention: 10 years.

Wear-Leveling Algorithm: support.

Bad Blocks Management: Support

Error Correct Code: Support

4.5 Transfer Mode

InnoDisk SATA Slim D150Q support following transfer mode:

PIO Mode 0~4.

Ultra DMA 0~6.

Serial ATA I 1.5Gbps

Serial ATA II 3.0Gbps

4.6 Pin Assignment

InnoDisk SATA Slim D150Q uses a micro SATA pin-out. Table 3 details the pin name, types and contact order of the two internal micro SATA plug options. A brief description is also included for signal, ground and power pins. There are total of 7 pins in the signal segment and 9 pins in the power segment.

Table 3: InnoDisk SATA Slim D150Q Pin Assignment

| Name | Type | Description |
|--|---------|---|
| S1 | GND | Ground |
| S2 | A+ | Differential Signal Pair A |
| S3 | A- | |
| S4 | GND | Ground |
| S5 | B- | Differential Signal Pair B |
| S6 | B+ | |
| S7 | GND | Ground |
| Key and Spacing separate signal and power segments | | |
| P1 | NC | NC |
| P2 | NC | NC |
| P3 | NC | NC |
| P4 | GND | Ground |
| P5 | GND | Ground |
| P6 | GND | Ground |
| P7 | V5 | 5V Power, Pre-Charge |
| P8 | V5 | 5V Power |
| P9 | V5 | 5V Power |
| P10 | GND | Ground |
| P11 | DAS/DSS | Device Activity Signal / Disable Staggered Spinup |
| P12 | GND | Ground |
| P13 | NC | NC |
| P14 | NC | NC |
| P15 | NC | NC |

4.7 Mechanical Dimensions

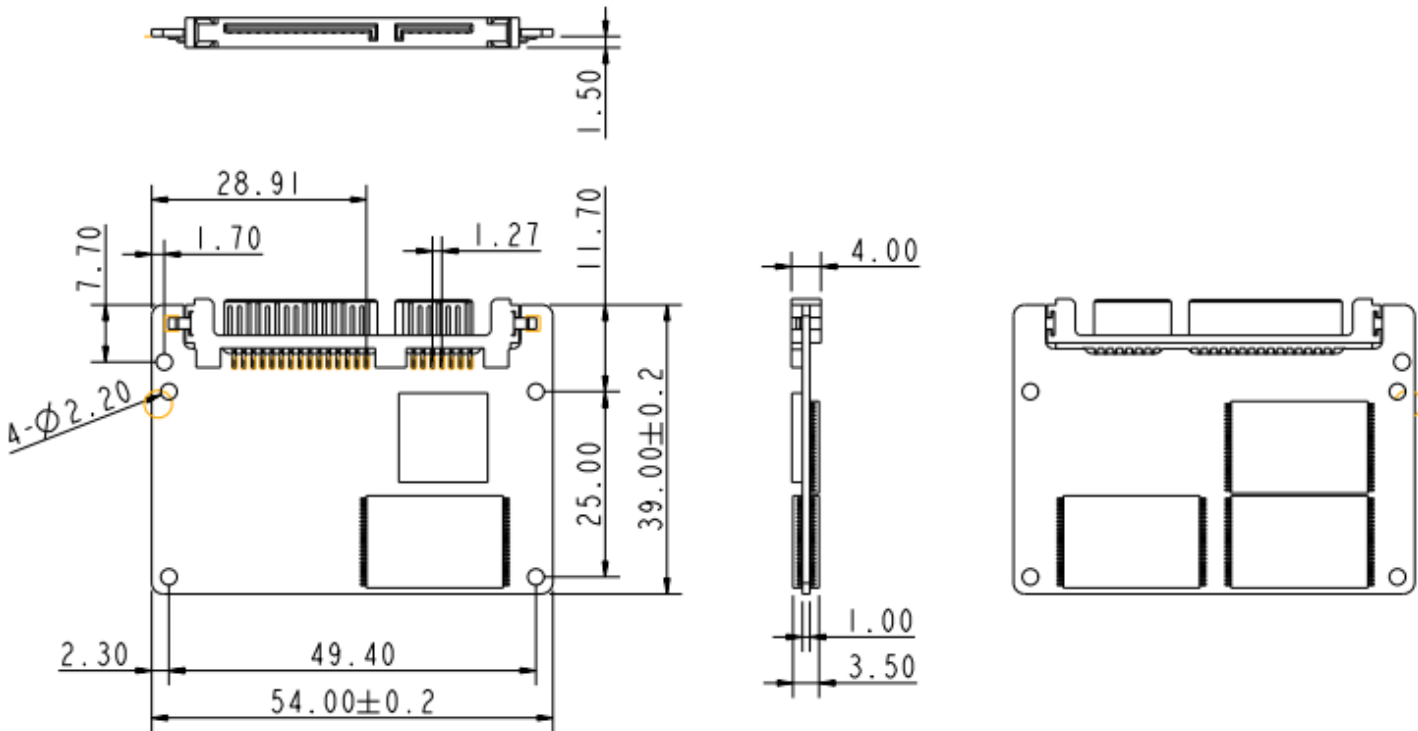


Figure 4: SATA Slim D150Q mechanical dimensions
(*Tolerance is ±0.1mm)

4.8 Weight

9g±2g

4.9 Performance

| Product name | | 2GB | 4GB | 8GB | 16GB | 32GB | 64GB |
|--------------|------------------|---------|--------|---------|---------|---------|---------|
| D150Q BGA | Sequential Read | 34 MB/S | 62MB/S | 110MB/S | 125MB/S | 130MB/S | 130MB/S |
| | Sequential Write | 26 MB/S | 36MB/S | 72MB/S | 107MB/S | 130MB/S | 130MB/S |

4.10 Seek Time

InnoDisk SATA Slim D150Q is not a magnetic rotating design. There is no seek or rotational latency required.

4.11 Hot Plug

The SSD support hot plug function and can be removed or plugged-in during operation. User has to avoid hot plugging the SSD which is configured as boot device and installed operation system.

Surprise hot plug : The insertion of a SATA device into a backplane (combine signal and power) that has power present. The device powers up and initiates an OOB sequence.

Surprise hot removal: The removal of a SATA device from a powered backplane, without first being placed in a quiescent state.

4.12 NAND Flash Memory

InnoDisk SATA Slim D150Q uses Single Level Cell (SLC) NAND flash memory, which is non-volatility, high reliability which has 100,000 program/erase times and high speed memory storage.

4.13 Electrical Specifications

4.13.1 Power Requirement

Table 4: InnoDisk SATA Slim D150Q Power Requirement

| Item | Symbol | Rating | Unit |
|---------------|-----------------|-------------------------|------|
| Input voltage | V _{IN} | +5DC +- 5% 500mA (max.) | V |

4.13.2 Power Consumption

Table 5: Power Consumption

| Mode | Power Consumption |
|-------|-------------------|
| Read | 180mA (max.) |
| Write | 200mA (max.) |
| Idle | 110mA (max.) |

4.14 Device Parameters

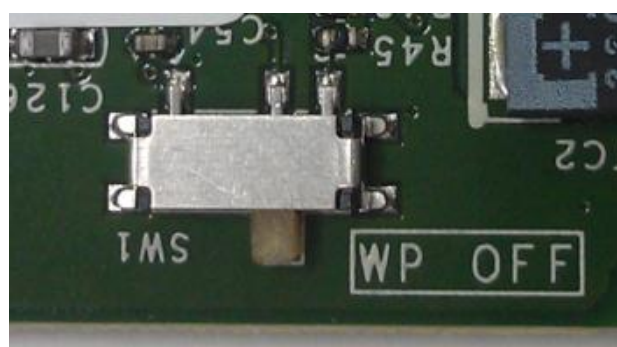
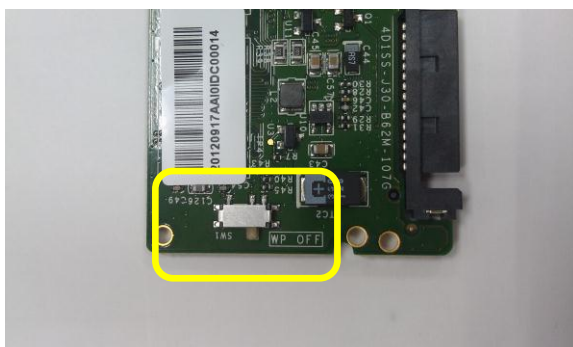
SATA Slim D150Q device parameters listed in Table 7.

Table 6: Device parameters

| Capacity | Cylinders | Heads | Sectors | LBA | User capacity(MB) |
|----------|-----------|-------|---------|-----------|-------------------|
| 2GB | 3897 | 16 | 63 | 3928176 | 1918MB |
| 4GB | 7773 | 16 | 63 | 7835184 | 3825MB |
| 8GB | 15525 | 16 | 63 | 15649200 | 7641MB |
| 16GB | 16383 | 16 | 63 | 31277232 | 15272MB |
| 32GB | 16383 | 16 | 63 | 62533296 | 30533MB |
| 64GB | 16383 | 16 | 63 | 125206528 | 61136MB |

4.15 Write protect switch

InnoDisk SATA SLIM D150Q has a write protect switch on itself, user can set the device in locked mode for read access only.



5. Supported ATA Commands

5.1 Supported ATA Commands

InnoDisk SATA Slim D150Q supports the commands listed in Table 7.

Table 7: ATA Commands

| Command Name | Code | PARAMETERS USED | | | | | |
|------------------------------|------------|-----------------|----|----|----|----|----|
| | | SC | SN | CY | DR | HD | FT |
| CHECK POWER MODE | E5h | O | X | X | O | X | X |
| DEVICE CONFIGURATION OVERLAY | B1h | X | X | X | O | X | O |
| EXECUTE DIAGNOSTICS | 90h | X | X | X | O | X | X |
| FLUSH CACHE | E7h | X | X | X | O | X | X |
| FLUSH CACHE EXT | EAh | X | X | X | O | X | X |
| IDENTIFY DEVICE | ECh | X | X | X | O | X | X |
| IDLE | E3h | O | X | X | O | X | X |
| IDLE IMMEDIATE | E1h | X | X | X | O | X | X |
| NOP | 00h | F | F | F | O | X | O |
| INITIALIZE DEVICE PARAMETERS | 91h | O | X | X | O | O | X |
| READ BUFFER | E4h | X | X | X | O | X | X |
| READ DMA | C8h or C9h | O | O | O | O | O | X |
| READ DMA EXT | 25h | O | O | O | O | O | X |
| READ FPDMA QUEUED | 60h | O | O | O | O | O | O |
| READ LOG EXT | 2Fh | O | O | O | O | O | O |
| READ MULTIPLE | C4h | O | O | O | O | O | X |
| READ MULTIPLE EXT | 29h | O | O | O | O | O | X |
| READ NATIVE MAX ADDRESS | F8h | X | X | X | O | X | X |
| READ NATIVE MAX ADDRESS EXT | 27h | X | X | X | O | X | X |
| READ SECTOR(S) | 20h or 21h | O | O | O | O | O | X |
| READ SECTOR(S) EXT | 24h | O | O | O | O | O | X |
| READ VERIFY SECTOR(S) | 40h or 41h | O | O | O | O | O | X |
| READ VERIFY SECTOR(S) EXT | 42h | O | O | O | O | O | X |
| RECALIBRATE | 10h | X | X | X | O | X | X |
| SECURITY DISABLE PASSWORD | F6h | X | X | X | O | X | X |
| SECURITY ERASE PREPARE | F3h | X | X | X | O | X | X |
| SECURITY ERASE UNIT | F4h | X | X | X | O | X | X |
| SECURITY FREEZE LOCK | F5h | X | X | X | O | X | X |
| SECURITY SET PASSWORD | F1h | X | X | X | O | X | X |
| SECURITY UNLOCK | F2h | X | X | X | O | X | X |

| | | | | | | | |
|------------------------|------------|---|---|---|---|---|---|
| SEEK | 7xh | X | X | O | O | O | X |
| SET FEATURES | EFh | O | X | X | O | X | O |
| SET MAX | F9h | O | O | O | O | O | O |
| SET MAX ADDRESS EXT | 37h | O | O | O | O | O | X |
| SET MULTIPLE MODE | C6h | O | X | X | O | X | X |
| SLEEP | E6h | X | X | X | O | X | X |
| SMART | B0h | X | X | O | O | X | O |
| STANDBY | E2h | X | X | X | O | X | X |
| STANDBY IMMEDIATE | E0h | X | X | X | O | X | X |
| WRITE BUFFER | E8h | X | X | X | O | X | X |
| WRITE DMA | CAh or CBh | O | O | O | O | O | X |
| WRITE DMA EXT | 35h | O | O | O | O | O | X |
| WRITE DMA FUA EXT | 3Dh | O | O | O | O | O | X |
| WRITE FPDMA QUEUED | 61h | O | O | O | O | O | O |
| WRITE LOG EXT | 3Fh | O | O | O | O | O | X |
| WRITE MULTIPLE | C5h | O | O | O | O | O | X |
| WRITE MULTIPLE EXT | 39h | O | O | O | O | O | X |
| WRITE MULTIPLE FUA EXT | CEh | O | O | O | O | O | X |
| WRITE SECTOR(S) | 30h or 31h | O | O | O | O | O | X |
| WRITE SECTOR(S) EXT | 34h | O | O | O | O | O | X |
| WRITE VERIFY | 3Ch | O | O | O | O | O | O |

Note:

O = Valid, X = Don't care

SC = Sector Count Register

SN = Sector Number Register

CY = Cylinder Low/High Register

DR = DEVICE SELECT Bit (DEVICE/HEAD Register Bit 4)

HD = HEAD SELECT Bit (DEVICE/HEAD Register Bit 3-0)

FT = Features Register

5.1.1 Check Power Mode

5.1.1.1 Command Code

E5h

5.1.1.2 Feature Set

Power Management feature set.

- This command is mandatory for devices.

-This command is mandatory when the Power Management feature set is implemented.

5.1.1.3 Protocol

Non-data command

5.1.1.4 Inputs

Table 8: Check power mode command for inputs information

| Register | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------------|-----|----|-----|-----|----|----|----|----|
| Features | Na | | | | | | | |
| Sector Count | Na | | | | | | | |
| LBA Low | Na | | | | | | | |
| LBA Mid | Na | | | | | | | |
| LBA High | Na | | | | | | | |
| Device | obs | Na | Obs | DEV | Na | Na | Na | Na |
| Command | E5h | | | | | | | |

Device register

DEV shall specify the selected device.

5.1.2 IDENTIFY DEVICE

5.1.2.1 Command Code

ECh

5.1.2.2 Feature Set

General feature set

-Mandatory for all devices.

-Devices implementing the PACKET Command feature set

5.1.2.3 Protocol

PIO data-in

5.1.2.4 Inputs

Table 9: Identify device command for inputs information

| Register | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------------|-----|----|-----|-----|----|----|----|----|
| Features | Na | | | | | | | |
| Sector Count | Na | | | | | | | |
| LBA Low | Na | | | | | | | |
| LBA Mid | Na | | | | | | | |
| LBA High | Na | | | | | | | |
| Device | obs | Na | Obs | DEV | Na | Na | Na | Na |
| Command | ECh | | | | | | | |

Device register

DEV shall specify the selected device.

5.1.2.5 Outputs

5.1.2.6 Normal outputs

Table 10: Identify device command for normal outputs information

| Register | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------------|----|---|---|---|---|---|---|---|
| Error | Na | | | | | | | |
| Sector Count | Na | | | | | | | |
| LBA Low | Na | | | | | | | |

| | | | | | | | | |
|----------|-----|------|-----|-----|-----|----|----|-----|
| LBA Mid | Na | | | | | | | |
| LBA High | Na | | | | | | | |
| Device | obs | Na | obs | DEV | Na | Na | Na | Na |
| Status | BSY | DRDY | DF | Na | DRQ | Na | Na | ERR |

Device register

DEV shall indicate the selected device.

Status register

BSY shall be cleared to zero indicating command completion.

DRDY shall be set to one.

DF (Device Fault) shall be cleared to zero.

DRQ shall be cleared to zero.

ERR shall be cleared to zero.

5.1.2.7 Prerequisites

DRDY set to one.

5.1.2.8 Description

The IDENTIFY DEVICE command enables the host to receive parameter information from the device. When the command is issued, the device sets the BSY bit to one, prepares to transfer the 256 words of device identification data to the host, sets the DRQ bit to one, clears the BSY bit to zero, and asserts INTRQ if nIEN is cleared to zero. The host may then transfer the data by reading the Data register. Table 8 defines the arrangement and meaning of the parameter words in the buffer. All reserved bits or words shall be zero.

Some parameters are defined as a 16-bit value. A word that is defined as a 16-bit value places the most significant bit of the value on signal line DD15 and the least significant bit on signal line DD0.

Some parameters are defined as 32-bit values (e.g. words (61:60)). Such fields are transfer using two successive word transfers. The device will first transfer the least significant bits, bits (15:0) of the value, on signal lines DD(15:0) respectively. After the least significant bits have been transferred, the most significant bits, bits(31:16) of the value, shall be transferred on DD(15:0) respectively.

Some parameters are defined as a string of ASCII characters.

Table 11: Identify device command parameters

| Word | Value | F/V | Description |
|------|-------|-----|--|
| 0 | 0040h | F | General configuration |
| | | X | 15 0 = ATA device |
| | | X | 14-8 Retired |
| | | X | 7-6 Obsolete |
| | | X | 5-3 Retired |
| | | V | 2 Response incomplete |
| | | X | 1 Retired |
| | | 0 | Reserved |
| 1 | XXXXh | F | Number of logical cylinders |
| 2 | C837h | V | Specific configuration |
| 3 | 0010h | F | Number of logical heads |
| 4-5 | 0000h | X | Retired |
| 6 | 003Fh | F | Number of logical sector per logical track |

| | | | |
|-------|-------|----------------------------|---|
| 7-8 | 0000h | | Reserved for assignment by the CompactFlash_ Association |
| 9 | 0000h | X | Retired |
| 10-19 | XXXXh | F | Serial number (20 ASCII characters) |
| 20-21 | 0000h | X | Retired |
| 22 | 0000h | X | Obsolete |
| 23-26 | XXXXh | F | Firmware revision (8 ASCII characters) |
| 27-46 | XXXXh | F | Model number (40 ASCII characters) |
| 47 | 8010h | F F | 15-8 80h 7-0 00h = Reserved 01h = Maximum number of 1 sectors on READ/WRITE MULTIPLE commands |
| 48 | 0000h | | Reserved |
| 49 | 2F00h | F F F F F X | Capabilities 15-14 Reserved for the IDENTIFY PACKET DEVICE command. 13 1 = Standby timer values as specified in this standard are supported 0 = Standby timer values shall be managed by the device 12 Reserved for the IDENTIFY PACKET DEVICE command. 11 1 = IORDY supported 0 = IORDY may be supported 10 1 = IORDY may be disabled 9 1 = LBA supported 8 1 = DMA supported. 7-0 Retired |
| 50 | 4000h | F F X F | Capabilities 15 Shall be cleared to zero. 14 Shall be set to one. 13-2 Reserved. 1 Obsolete 0 Shall be set to one to indicate a device specific Standby timer value minimum. |
| 51 | 0000h | F | 15-8 PIO data transfer cycle timing mode 7-0 Reserved |
| 52 | 0000h | X | Obsolete |
| 53 | 0007h | F F F X | 15-3 Reserved 2 1 = the fields reported in word 88 are valid 0 = the fields reported in word 88 are not valid 1 1 = the fields reported in words 70:64 are valid 0 = the fields reported in words 70:64 are not valid 0 1 = the fields reported in words 58:54 are valid 0 = the fields reported in words 58:54 are not valid |
| 54 | XXXXh | X | Number of current cylinders |
| 55 | 0010h | X | Number of current heads |
| 56 | 003Fh | X | Number of current sector per track |
| 57-58 | XXXXh | X | Current capacity in sectors |
| 59 | 0110h | V V | 15-9 Reserved 8 1 = Multiple sector setting is valid 7-0 xxh = Setting for number of sectors that shall be transferred per interrupt on R/W Multiple command |
| 60-61 | XXXXh | F | Total number of user addressable sectors |
| 62 | 0000h | X | Obsolete |
| 63 | 0X07h | | 15-11 Reserved |

| | | | | |
|-------|-------|---|-------|--|
| | | V | 10 | 1 = Multiword DMA mode 2 is selected 0 = Multiword DMA mode 2 is not selected |
| | | V | 9 | 1 = Multiword DMA mode 1 is selected 0 = Multiword DMA mode 1 is not selected |
| | | V | 8 | 1 = Multiword DMA mode 0 is selected 0 = Multiword DMA mode 0 is not selected |
| | | | 7-3 | Reserved |
| | | F | 2 | 1 = Multiword DMA mode 2 and below are supported |
| | | F | 1 | 1 = Multiword DMA mode 1 and below are supported |
| | | F | 0 | 1 = Multiword DMA mode 0 is supported |
| 64 | 0003h | | 15-8 | Reserved |
| | | F | 7-0 | Advanced PIO modes supported |
| 65 | 0078h | F | | Minimum Multiword DMA transfer cycle time per word |
| 66 | 0078h | F | | Manufacturer's recommended Multiword DMA transfer cycle time |
| 67 | 0078h | F | | Minimum PIO transfer cycle time without flow control |
| 68 | 0078h | F | | Minimum PIO transfer cycle time with IORDY flow control |
| 69-70 | 0000h | | | Reserved |
| 71-74 | 0000h | | | Reserved for the IDENTIFY PACKET DEVICE command |
| 75 | 001Fh | | | Queue depth |
| | | | 15-5 | Reserved |
| | | F | 4-0 | Maximum queue depth - 1 |
| 76 | 0106h | | | Serial ATA Capabilities |
| | | | 15-11 | Reserved for Serial ATA |
| | | F | 10 | 1 = Supports Phy Event Counts |
| | | F | 9 | 1 = Supports receipt of host initiated power management requests |
| | | F | 8 | 1 = Supports the NCQ feature set |
| | | | 7-3 | Reserved for Serial ATA |
| | | F | 2 | 1 = Supports SATA Gen2 Signaling Speed (3.0Gb/s) |
| | | F | 1 | 1 = Supports SATA Gen1 Signaling Speed (1.5Gb/s) |
| | | F | 0 | Shall be cleared to zero |
| 77 | 0000h | | | Reserved for Serial ATA |
| 78 | 0044h | | | Serial ATA feature supported |
| | | | 15-7 | Reserved for Serial ATA |
| | | F | 6 | 1 = Device supports Software Settings Preservation |
| | | | 5 | Reserved for Serial ATA |
| | | F | 4 | 1 = Device supports in-order data delivery |
| | | F | 3 | 1 = Device supports initiating power management |
| | | F | 2 | 1 = Device supports DMA Setup auto-activation |
| | | F | 1 | 1 = Device supports non-zero buffer offsets |
| | | F | 0 | Shall be cleared to zero |
| 79 | 0040h | | | Serial ATA feature enabled |
| | | | 15-7 | Reserved for Serial ATA |
| | | V | 6 | 1 = Software Settings Preservation enabled |
| | | | 5 | Reserved for Serial ATA |
| | | V | 4 | 1 = In-order data delivery enabled |
| | | V | 3 | 1 = Device initiated power management enabled |
| | | V | 2 | 1 = DMA Setup auto-activation enabled |
| | | V | 1 | 1 = Non-zero buffer offsets enabled |
| | | F | 0 | Shall be cleared to zero |
| 80 | 01F0h | | | Major version number 0000h or FFFFh = device does not report version |
| | | | 15 | Reserved |
| | | F | 14 | Reserved for ATA/ATAPI-14 |
| | | F | 13 | Reserved for ATA/ATAPI-13 |
| | | F | 12 | Reserved for ATA/ATAPI-12 |
| | | F | 11 | Reserved for ATA/ATAPI-11 |
| | | F | 10 | Reserved for ATA/ATAPI-10 |
| | | F | 9 | Reserved for ATA/ATAPI-9 |

| | | | | |
|----|-------|---|----|--|
| | | F | 8 | Reserved for ATA/ATAPI-8 |
| | | F | 7 | 1 = supports ATA/ATAPI-7 |
| | | F | 6 | 1 = supports ATA/ATAPI-6 |
| | | F | 5 | 1 = supports ATA/ATAPI-5 |
| | | F | 4 | 1 = supports ATA/ATAPI-4 |
| | | F | 3 | Obsolete |
| | | X | 2 | Obsolete |
| | | X | 1 | Obsolete |
| | | | 0 | Reserved |
| 81 | 0000h | F | | Minor version number |
| 82 | 746Bh | X | 15 | Command and feature sets supported Obsolete |
| | | F | 14 | 1 = NOP command supported |
| | | F | 13 | 1 = READ BUFFER command supported |
| | | F | 12 | 1 = WRITE BUFFER command supported |
| | | X | 11 | Obsolete |
| | | F | 10 | 1 = Host Protected Area feature set supported |
| | | F | 9 | 1 = DEVICE RESET command supported |
| | | F | 8 | 1 = SERVICE interrupt supported |
| | | F | 7 | 1 = release interrupt supported |
| | | F | 6 | 1 = look-ahead supported |
| | | F | 5 | 1 = write cache supported |
| | | F | 4 | Shall be cleared to zero to indicate that the PACKET Command feature set is not supported. |
| | | F | 3 | 1 = mandatory Power Management feature set supported |
| | | F | 2 | 1 = Removable Media feature set supported |
| | | F | 1 | 1 = Security Mode feature set supported |
| | | | 0 | 1 = SMART feature set supported |
| 83 | 7D08h | F | 15 | Command and feature sets supported Shall be cleared to zero |
| | | F | 14 | Shall be set to one |
| | | F | 13 | 1 = The FLUSH CACHE EXT command is supported |
| | | F | 12 | Shall be set to one to indicate that the mandatory FLUSH CACHE command is supported |
| | | F | 11 | 1 = The DCO feature set is supported |
| | | F | 10 | 1 = The 48-bit Address feature set is supported |
| | | F | 9 | 1 = The AAM feature set is supported |
| | | | 8 | 1 = SET MAX security extension supported |
| | | F | 7 | Reserved |
| | | F | 6 | 1 = SET FEATURES subcommand required to spinup after power-up |
| | | F | 5 | 1 = Power-Up In Standby feature set supported |
| | | F | 4 | 1 = Removable Media Status Notification feature set supported |
| | | F | 3 | 1 = Advanced Power Management feature set supported |
| | | F | 2 | 1 = CFA feature set supported |
| | | | 1 | 1 = READ/WRITE DMA QUEUED supported |
| | | | 0 | 1 = DOWNLOAD MICROCODE command supported |

| | | | | |
|----|-------|---|-------|--|
| 84 | 4040h | F | 15 | Shall be cleared to zero |
| | | F | 14 | Shall be set to one |
| | | F | 13 | 1 = The IDLE IMMEDIATE command with UNLOAD feature is supported |
| | | X | 12-11 | Reserved for TLC |
| | | F | 10-9 | Obsolete |
| | | F | 8 | 1 = The 64-bit World wide name is supported |
| | | F | 7 | 1 = The WRITE DMA QUEUED FUA EXT command is supported |
| | | F | 6 | 1 = The WRITE DMA FUA EXT and WRITE MULTIPLE FUA EXT commands are supported |
| | | F | 5 | 1 = The GPL feature set is supported |
| | | F | 4 | 1 = The Streaming feature set is supported |
| | | F | 3 | 1 = The Media Card Pass Through Command feature set is supported |
| | | F | 2 | 1 = Media serial number is supported |
| | | F | 1 | 1 = SMART self-test supported |
| | | F | 0 | 1 = SMART error logging supported |
| 85 | 746Xh | Command and feature sets supported or enable | | |
| | | X | 15 | Obsolete |
| | | F | 14 | 1 = The NOP command is supported |
| | | F | 13 | 1 = The READ BUFFER command is supported |
| | | F | 12 | 1 = The WRITE BUFFER command is supported |
| | | X | 11 | Obsolete |
| | | V | 10 | 1 = HPA feature set is supported |
| | | F | 9 | Shall be cleared to zero to indicate that the DEVICE RESET command is not supported |
| | | V | 8 | 1 = The SERVICE interrupt is enabled |
| | | V | 7 | 1 = The release interrupt is enabled |
| | | V | 6 | 1 = Read look-ahead is enabled |
| | | F | 5 | 1 = The volatile write cache is enabled |
| | | F | 4 | Shall be cleared to zero to indicate that the PACKET Command feature set is not supported. |
| | | V | 3 | Shall be set to one to indicate that the mandatory Power Management feature is supported |
| V | 2 | Obsolete | | |
| V | 1 | 1 = The Security feature set is enabled | | |
| V | 0 | 1 = The SMART feature set is enabled | | |
| 86 | BC00h | Command and feature sets supported or enable | | |
| | | F | 15 | 1 = Words 119-120 are valid |
| | | F | 14 | Reserved |
| | | F | 13 | 1 = FLUSH CACHE EXT command supported |
| | | F | 12 | 1 = FLUSH CACHE command supported |
| | | F | 11 | 1 = The DCO feature set is supported |
| | | F | 10 | 1 = The 48-bit Address feature set is supported |
| | | V | 9 | 1 = The AAM feature set is enable |
| | | V | 8 | 1 = The SET MAX security extension is enabled by SET MAX SET PASSWORD |
| | | F | 7 | Reserved for Address Offset Reserved Area Boot Method |
| | | V | 6 | 1 = SET FEATURES subcommand required to spin-up after power-up |
| | | X | 5 | 1 = The PUIS feature set is enabled |
| | | V | 4 | Obsolete |
| | | F | 3 | 1 = The APM feature set is enabled |
| F | 2 | 1 = The CFA feature set is supported | | |
| F | 1 | 1 = The TCQ feature set is supported | | |
| F | 0 | 1 = The DOWNLOAD MICROCODE command is supported | | |
| 87 | 4040h | Command and feature sets supported or enabled | | |
| | | F | 15 | Shall be cleared to zero |
| | | F | 14 | Shall be set to one |
| F | 13 | 1 = The IDLE IMMEDIATE command with UNLOAD feature is | | |

| | | | |
|---------|-------|---|---|
| | | X | supported |
| | | F | 12-11 Reserved for TLC |
| | | F | 10-9 Obsolete |
| | | F | 8 1 = The 64-bit World wide name is supported |
| | | F | 7 1 = The WRITE DMA QUEUED FUA EXT command is supported |
| | | F | 6 1 = The WRITE DMA FUA EXT and WRITE MULTIPLE FUA EXT commands are supported |
| | | V | 5 1 = The GPL feature set is supported |
| | | V | 4 Obsolete |
| | | F | 3 1 = The Media Card Pass Through Command feature set is supported |
| | | F | 2 1 = Media serial number is supported |
| | | 1 | 1 = SMART self-test supported |
| | | 0 | 1 = SMART error logging supported |
| 88 | XX7Fh | V | Ultra DMA modes |
| | | V | 15 Reserved |
| | | V | 14 1 = Ultra DMA mode 6 is selected 0 = Ultra DMA mode 6 is not selected |
| | | V | 13 1 = Ultra DMA mode 5 is selected 0 = Ultra DMA mode 5 is not selected |
| | | V | 12 1 = Ultra DMA mode 4 is selected 0 = Ultra DMA mode 4 is not selected |
| | | V | 11 1 = Ultra DMA mode 3 is selected 0 = Ultra DMA mode 3 is not selected |
| | | V | 10 1 = Ultra DMA mode 2 is selected 0 = Ultra DMA mode 2 is not selected |
| | | V | 9 1 = Ultra DMA mode 1 is selected 0 = Ultra DMA mode 1 is not selected |
| | | V | 8 1 = Ultra DMA mode 0 is selected 0 = Ultra DMA mode 0 is not selected |
| | | | 7 Reserved |
| | | F | 6 1 = Ultra DMA mode 6 and below are supported |
| | | F | 5 1 = Ultra DMA mode 5 and below are supported |
| | | F | 4 1 = Ultra DMA mode 4 and below are supported |
| | | F | 3 1 = Ultra DMA mode 3 and below are supported |
| | | F | 2 1 = Ultra DMA mode 2 and below are supported |
| | | F | 1 1 = Ultra DMA mode 1 and below are supported |
| | | F | 0 1 = Ultra DMA mode 0 is supported |
| 89 | 001Eh | F | 15-8 Reserved |
| | | | 7-0 Time required for Normal Erase mode SECURITY ERASE UNIT command |
| 90 | 001Eh | F | 15-8 Reserved |
| | | | 7-0 Time required for Enhanced Erase mode SECURITY ERASE UNIT command |
| 91 | 0000h | V | Current APM level value |
| 92 | FFFEh | V | Master Password Identifier |
| 93 | 0000h | X | Hardware reset result |
| 94 | 0000h | F | Current AAM value |
| | | V | 15-8 Vendor's recommended AAM value |
| | | | 7-0 Current AAM value |
| 95-99 | 0000h | | Reserved |
| 100-103 | XXXXh | X | Total Number of User Addressable Logical Sectors for 48-bit commands (QWord) |
| 104-105 | 0000h | | Reserved |
| 106 | 4000h | F | Physical sector size / logical sector size |
| | | F | 15 Shall be cleared to zero |
| | | F | 14 Shall be set to one |
| | | F | 13 1 = Device has multiple logical sectors per physical sector |

| | | | | |
|---------|-------|---|------|---|
| | | F | 12 | 1 = Device Logical Sector longer than 256 Words |
| | | | 11-4 | Reserved |
| | | F | 3-0 | 2x logical sectors per physical sector |
| 107 | 0000h | F | | Inter-seek delay for ISO 7779 standard acoustic testig |
| 108-111 | XXXXh | F | | Worldwide name |
| 112-115 | 0000h | | | Reserved |
| 116 | 0000h | | | Reserved for TLC |
| 117-118 | 0000h | F | | Logical sector size (DWord) |
| 119 | 4000h | | | Commands and feature sets supported (Continued from words 84:82) |
| | | F | 15 | Shall be cleared to zero |
| | | F | 14 | Shall be set to one |
| | | | 13-6 | Reserved |
| | | F | 5 | 1= The Free-fall Control feature set is supported |
| | | F | 4 | 1 = The DOWNLOAD MICROCODE command with mode 3 is supported |
| | | F | 3 | 1 = The READ LOG DMA EXT and WRITE LOG DMA EXT commands are supported |
| | | F | 2 | 1 = The WRITE UNCORRECTABLE EXT command is supported |
| | | F | 1 | 1 = The Write-Read-Verify feature set is supported |
| | | F | 0 | Reserved for DDT |
| 120 | 4000h | | | Commands and feature sets supported or enabled (Continued from words 87:85) |
| | | F | 15 | Shall be cleared to zero |
| | | F | 14 | Shall be set to one |
| | | V | 13-6 | Reserved |
| | | F | 5 | 1= The Free-fall Control feature set is enabled |
| | | F | 4 | 1 = The DOWNLOAD MICROCODE command with mode 3 is supported |
| | | F | 3 | 1 = The READ LOG DMA EXT and WRITE LOG DMA EXT commands are supported |
| | | V | 2 | 1 = The WRITE UNCORRECTABLE EXT command is supported |
| | | V | 1 | 1 = The Write-Read-Verify feature set is enabled |
| | | V | 0 | Reserved for DDT |
| 121-126 | 0000h | | | Reserved for expended supported and enabled settings |
| 127 | 0000h | X | | Obsolete |
| 128 | 0021h | | | Security status |
| | | | 15-9 | Reserved |
| | | V | 8 | Security level 0 = High, 1 = Maximum |
| | | | 7-6 | Reserved |
| | | F | 5 | 1 = Enhanced security erase supported |
| | | V | 4 | 1 = Security count expired |
| | | V | 3 | 1 = Security frozen |
| | | V | 2 | 1 = Security locked |
| | | V | 1 | 1 = Security enabled |
| | | F | 0 | 1 = Security supported |
| 129-159 | 0000h | X | | Vendor specific |
| 160 | 0000h | | | CFA power mode |
| | | F | 15 | Word 160 supported |
| | | | 14 | Reserved |
| | | F | 13 | CFA power mode 1 is required for one or more commands implemented by the device |
| | | V | 12 | CFA power mode 1 disabled |
| | | F | 11:0 | Maximum current in ma |
| 161-167 | 0000h | | | Reserved for the Compact Flash Association |
| 168 | 0003h | | 15:4 | Reserved |

| | | | | |
|---------|-------|---|-------|---|
| | | F | 3:0 | Device Nominal Form Factor |
| 169 | 0000h | | | DATA SET MANAGEMENT is supported |
| | | F | 15:1 | Reserved |
| | | F | 0 | 1 = the Trim bit in the DATA SET MANAGEMENT is supported |
| 170-173 | 0000h | F | | Additional Product Identifier (ATA String) |
| 174-175 | 0000h | | | Reserved |
| 176-205 | 0000h | V | | Current media serial number (ATA String) |
| 206 | 0000h | X | | SCT Command Transport |
| | | | 15:12 | Vendor Specific |
| | | | 11:6 | Reserved |
| | | F | 5 | The SCT Data Tables command is supported |
| | | F | 4 | The SCT Feature Control command is supported |
| | | F | 3 | The SCT Error Recovery Control command is supported |
| | | F | 2 | The SCT Write Same command is supported |
| | | F | 1 | Obsolete |
| | | F | 0 | The SCT Command Transport is supported |
| 207-208 | 0000h | | | Reserved for CE-ATA |
| 209 | 4000h | | | Alignment of logical blocks within a physical block |
| | | | 15 | Shall be cleared to zero |
| | | | 14 | Shall be set to one |
| | | F | 13:0 | Logical sector offset within the first physical sector where the first logical sector is placed |
| 210-211 | 0000h | V | | Write-Read-Verify Sector Count Mode 3 (DWord) |
| 212-213 | 0000h | F | | Write-Read-Verify Sector Count Mode 2 (DWord) |
| 214 | 0000h | F | | NV Cache Capabilities |
| | | F | 15:12 | NC+V Cache feature set version |
| | | F | 11:8 | NV Cache Power Mode feature set version |
| | | | 7:5 | Reserved |
| | | V | 4 | 1 = NV Cache feature set enabled |
| | | | 3:2 | Reserved |
| | | V | 1 | 1 = NV Cache Power Mode feature set enabled |
| | | F | 0 | 1 = NV Cache Power Mode feature set supported |
| 215-216 | 0000h | V | | NV Cache Size in Logical Blocks (DWord) |
| 217 | 0001h | F | | Nominal media rotation rate |
| 218 | 0000h | | | Reserved |
| 219 | 0000h | F | | NV Cache Options |
| | | | 15:8 | Reserved |
| | | | 7:0 | Device Estimated Time to Spin Up in Seconds |
| 220 | 0000h | V | | 15:8 Reserved |
| | | | 7:0 | Write-Read-Verify feature set current mode |
| 221 | 0000h | | | Reserved |
| 222 | 101Fh | | | Transport major version number |
| | | | | 0000h or FFFFh = device does not report version |
| | | F | 15:12 | Transport Type |
| | | | | 0h = Parallel |
| | | | | 1h = Serial |
| | | | | 2h-Fh = Reserved |
| | | | | Parallel Serial |
| | | | 11:5 | Reserved Reserved |
| | | F | 4 | Reserved SATA Rev 2.6 |
| | | F | 3 | Reserved SATA Rev 2.5 |
| | | F | 2 | Reserved SATA II: Extensions |
| | | F | 1 | ATA/ATAPI-7 SATA 1.0a |
| | | F | 0 | ATA8-APT ATA8-AST |

| | | | |
|---------|-------|---|--|
| 223 | 0000h | F | Transport minor version number |
| 224-233 | 0000h | | Reserved for CE-ATA |
| 234 | 0000h | F | Minimum number of 512-byte data blocks per DOWNLOAD MICROCODE command for mode 3 |
| 235 | 0000h | F | Maximum number of 512-byte data blocks per DOWNLOAD MICROCODE command for mode 3 |
| 236-254 | 0000h | | Reserved |
| 255 | XXXXh | V | Integrity word |
| | | V | 15-8 Checksum |
| | | V | 7-0 Checksum Validity Indicator |

Key:

F/V – Fixed/variable content

F = the content of the word is fixed and does not change. For removable media devices, these values may change when media is removed or changed.

V = the contents of the word is variable and may change depending on the state of the device or the commands executed by the device.

X = the content of the word may be fixed or variable.

5.1.3 IDLE

5.1.3.1.1 Command Code

E3h

5.1.3.1.2 Feature Set

Power Management Feature Set.

5.1.3.1.3 Protocol

Non-Data

5.1.3.1.4 Inputs

Values other than zero in the Sector Count register when the IDLE command is issued shall determine the time period programmed into the Standby timer.

Table 12: Idle command for inputs information

| Register | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------------|--------------------|----|-----|-----|----|----|----|----|
| Features | Na | | | | | | | |
| Sector Count | Timer period value | | | | | | | |
| LBA Low | Na | | | | | | | |
| LBA Mid | Na | | | | | | | |
| LBA High | Na | | | | | | | |
| Device | Obs | Na | Obs | DEV | Na | Na | Na | Na |
| Command | E3h | | | | | | | |

Device register-

DEV shall specify the selected device.

Table 13: Idle command sector count register contents information

| Sector Count register contents | Corresponding timeout period |
|--------------------------------|------------------------------|
| 0 (00h) | Timeout disabled |
| 1-240 (01h-F0h) | (value*5)s |
| 241-251 (F1h-FBh) | ((Value-240)*30)min |

| | |
|------------------------------|-----------------------------|
| 252 (FCh) | 21min |
| 253 (FDh) | Period between 8 and 12 hrs |
| 254 (FEh) | Reserved |
| 255 (FFh) | 21 min 15 s |
| NOTE – Times are approximate | |

5.1.3.1.5 Normal Outputs

Table 14: Idle command for normal outputs information

| Register | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------------|-----|------|-----|-----|-----|----|----|-----|
| Error | Na | | | | | | | |
| Sector Count | Na | | | | | | | |
| LBA Low | Na | | | | | | | |
| LBA Mid | Na | | | | | | | |
| LBA High | Na | | | | | | | |
| Device | obs | Na | obs | DEV | Na | Na | Na | Na |
| Status | BSY | DRDY | DF | Na | DRQ | Na | Na | ERR |

Device Register-

DEV shall indicate the selected device.

Status register-

BSY will be cleared to zero indicating command completion.

DRDY will be set to one.

DF (Device Fault) will be cleared to zero.

DRQ shall be cleared to zero.

ERR shall be cleared to zero.

5.1.3.1.6 Error Outputs

Table 15: Idle command for error outputs information

| Register | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------------|-----|------|-----|-----|-----|------|----|-----|
| Error | Na | Na | Na | Na | Na | ABRT | Na | Na |
| Sector Count | Na | | | | | | | |
| LBA Low | Na | | | | | | | |
| LBA Mid | Na | | | | | | | |
| LBA High | Na | | | | | | | |
| Device | obs | Na | obs | DEV | Na | | | |
| Status | BSY | DRDY | DF | Na | DRQ | Na | Na | ERR |

5.1.3.1.7 Prerequisites

DRDY set to one

5.1.3.1.8 Description

The IDLE command allows the host to place the device in the idle mode and also set the Standby timer.

5.1.4 Idle Immediate

5.1.4.1.1 Command Code

E1h

5.1.4.1.2 Feature Set

Power Management Feature Set.

5.1.4.1.3 Protocol

Non-Data

5.1.4.1.4 Inputs

Table 16: Idle immediate command for inputs information

| Register | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------------|-----|----|-----|-----|----|----|----|----|
| Features | Na | | | | | | | |
| Sector Count | Na | | | | | | | |
| LBA Low | Na | | | | | | | |
| LBA Mid | Na | | | | | | | |
| LBA High | Na | | | | | | | |
| Device | obs | Na | obs | DEV | Na | Na | Na | Na |
| Command | E1h | | | | | | | |

Device register-

DEV shall specify the selected device.

5.1.4.1.5 Normal Outputs

Table 17: Idle immediate command for normal outputs information

| Register | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------------|-----|------|-----|-----|-----|----|----|-----|
| Error | Na | | | | | | | |
| Sector Count | Na | | | | | | | |
| LBA Low | Na | | | | | | | |
| LBA Mid | Na | | | | | | | |
| LBA High | Na | | | | | | | |
| Device | obs | Na | obs | DEV | Na | Na | Na | Na |
| Status | BSY | DRDY | DF | Na | DRQ | Na | Na | ERR |

Device Register-

DEV shall indicate the selected device.

Status register-

BSY will be cleared to zero indicating command completion.

DRDY will be set to one.

DF (Device Fault) will be cleared to zero.

DRQ shall be cleared to zero.

ERR shall be cleared to zero.

5.1.4.2 Prerequisites

DRDY set to one

5.1.4.3 Description

The IDLE IMMEDIATE command allows the host to immediately place the device in the idle

mode.

5.1.5 SMART

Individual SMART commands are identified by the value placed in the Feature register.

Table 18: SMART Feature register values

| Value | Command |
|-------|--------------------------|
| D0h | SMATR Read Data |
| D8h | SMART ENABLE OPERATIONS |
| D9h | SMART DISABLE OPERATIONS |

5.1.5.1 SMART Read Data

5.1.5.1.1 Command Code

B0h with a Feature register value of D0h

5.1.5.1.2 Feature Set

Smart Feature Set

- Operation when the SMART feature set is implemented.

5.1.5.1.3 Protocol

PIO data-in

5.1.5.1.4 Inputs

Table 19: SMART command for inputs information

| Register | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------------|-----|----|-----|-----|----|----|----|----|
| Features | D0h | | | | | | | |
| Sector Count | Na | | | | | | | |
| LBA Low | Na | | | | | | | |
| LBA Mid | 4Fh | | | | | | | |
| LBA High | C2h | | | | | | | |
| Device | Obs | Na | obs | DEV | Na | Na | Na | Na |
| Command | B0h | | | | | | | |

Device register-

DEV shall specify the selected device.

5.1.5.1.5 Normal Outputs

Table 20: SMART command for normal outputs information

| Register | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------------|-----|------|-----|-----|-----|----|----|-----|
| Error | Na | | | | | | | |
| Sector Count | Na | | | | | | | |
| LBA Low | Na | | | | | | | |
| LBA Mid | Na | | | | | | | |
| LBA High | Na | | | | | | | |
| Device | Obs | Na | obs | DEV | Na | Na | Na | Na |
| Status | BSY | DRDY | DF | Na | DRQ | Na | Na | ERR |

Device Register-

DEV shall indicate the selected device.

Status register-

BSY will be cleared to zero indicating command completion.

DRDY will be set to one.

DF (Device Fault) will be cleared to zero.

DRQ shall be cleared to zero.

ERR shall be cleared to zero.

5.1.5.1.6 Prerequisites

DRDY set to one. SMART enabled.

5.1.5.1.7 Description

This command returns the Device SMART data structure to the host.

Table 21: ID of SMART data structure

| | +0 | +1 | +2 | +3 | +4 | +5 | +6 | +7 | +8 | +9 | +10 | +11 |
|--------------------------------|-----|-------|-----|------|-------|---------------------|-----|------|-----|------|-----|-----|
| Attribute Name | ID | Flags | | Init | Worst | Raw Attribute Value | | | | | | Rsv |
| Read Error Rate | 01h | 0Bh | 00h | 64h | 64h | FFh | FFh | FFh | 00h | 00h | 00h | 00h |
| Throughput Performance | 02h | 05h | 00h | 64h | 64h | 00h | 00h | 00h | 00h | 00h | 00h | 00h |
| Spin Up Time | 03h | 07h | 00h | 64h | 64h | 00h | 00h | 00h | 00h | 00h | 00h | 00h |
| Reallocated Sector Count | 05h | 13h | 00h | 64h | 64h | 00h | 00h | 00h | 00h | 00h | 00h | 00h |
| Seek Error Rate | 07h | 0Bh | 00h | 64h | 64h | 00h | 00h | 00h | 00h | 00h | 00h | 00h |
| Seek Time performance | 08h | 05h | 00h | 64h | 64h | 00h | 00h | 00h | 00h | 00h | 00h | 00h |
| Power-On hours Count | 09h | 12h | 00h | 64h | 64h | (1) | | 00h | 00h | 00h | 00h | 00h |
| Spin Retry Count | 0Ah | 13h | 00h | 64h | 64h | 00h | 00h | 00h | 00h | 00h | 00h | 00h |
| Drive Power Cycle Count | 0Ch | 12h | 00h | 64h | 64h | (2) | | 00h | 00h | 00h | 00h | 00h |
| SATA PHY Error Count | A8h | 12h | 00h | 64h | 64h | (3) | | 00h | 00h | 00h | 00h | 00h |
| Bad Block Count | AAh | 03h | 00h | 64h | 64h | 00h | 00h | (4) | | (5) | | 00h |
| Erase Count | ADh | 12h | 00h | 64h | 64h | (6) | | (7) | | (6) | (7) | 00h |
| Bad Cluster Table Count | AFh | 03h | 00h | 64h | 64h | (8) | | 00h | 00h | 00h | 00h | 00h |
| Unexpected Power Loss Count | C0h | 12h | 00h | 64h | 64h | (9) | | 00h | 00h | 00h | 00h | 00h |
| Temperature | C2h | 22h | 00h | (10) | 64h | (10) | 00h | (11) | 00h | (12) | 00h | 00h |
| Current Pending Sector Counter | C5h | 12h | 00h | 64h | 64h | 00h | 00h | 00h | 00h | 00h | 00h | 00h |
| Write Head | F0h | 13h | 00h | 64h | 64h | 00h | 00h | 00h | 00h | 00h | 00h | 00h |

Table 22: Smart command for average/max erase count information

| | SMART | DI 101 |
|-------------|------------------------------------|---|
| | F: Fixed V: Variable X: None | |
| Byte | F/V | Description |
| 0-188 | X | |
| 189-190 | F | Total Bad Block Number of System(190:MSB 189:LSB) |
| 191-192 | F | Later Bad Block Number of System(192:MSB 191:LSB) |
| 193-198 | X | |
| 199-200.203 | F | Average Erase Count(203:MSB 199:LSB) |

| | | |
|-------------|---|--------------------------------------|
| 201-202.204 | V | Maximum Erase Count(204:MSB 201:LSB) |
| 205-510 | X | |
| 511 | V | Check Sum |

When the Maximum erase count is 255 bigger than average erase count, the wear-leveling will be executed.

5.1.5.2 SMART ENABLE OPERATIONS

5.1.5.2.1 Command Code

B0h with a Feature register value of D8h

5.1.5.2.2 Feature Set

Smart Feature Set

5.1.5.2.3 Protocol

Non-data

5.1.5.2.4 Inputs

Table 23: SMART Enable command for inputs information

| Register | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------------|-----|----|-----|-----|----|----|----|----|
| Features | D8h | | | | | | | |
| Sector Count | Na | | | | | | | |
| LBA Low | Na | | | | | | | |
| LBA Mid | 4Fh | | | | | | | |
| LBA High | C2h | | | | | | | |
| Device | Obs | Na | obs | DEV | Na | Na | Na | Na |
| Command | B0h | | | | | | | |

Device register-

DEV shall specify the selected device.

5.1.5.2.5 Normal Outputs

Table 24: SMART command for normal outputs information

| Register | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------------|-----|------|-----|-----|-----|----|----|-----|
| Error | Na | | | | | | | |
| Sector Count | Na | | | | | | | |
| LBA Low | Na | | | | | | | |
| LBA Mid | Na | | | | | | | |
| LBA High | Na | | | | | | | |
| Device | Obs | Na | obs | DEV | Na | Na | Na | Na |
| Status | BSY | DRDY | DF | Na | DRQ | Na | Na | ERR |

Device Register-

DEV shall indicate the selected device.

Status register-

BSY will be cleared to zero indicating command completion.

DRDY will be set to one.

DF (Device Fault) will be cleared to zero.

DRQ shall be cleared to zero.

ERR shall be cleared to zero.

5.1.5.2.6 Prerequisites

DRDY set to one.

5.1.5.2.7 Description

This command enables access to all SMART capabilities within device.

5.1.5.3 SMART DISABLE OPERATIONS

5.1.5.3.1 Command Code

B0h with a Feature register value of D9h

5.1.5.3.2 Feature Set

Smart Feature Set

5.1.5.3.3 Protocol

Non-data

5.1.5.3.4 Inputs

Table 25: SMART DISABLE Command for inputs information

| Register | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------------|-----|----|-----|-----|----|----|----|----|
| Features | D9h | | | | | | | |
| Sector Count | Na | | | | | | | |
| LBA Low | Na | | | | | | | |
| LBA Mid | 4Fh | | | | | | | |
| LBA High | C2h | | | | | | | |
| Device | Obs | Na | obs | DEV | Na | Na | Na | Na |
| Command | B0h | | | | | | | |

Device register-

DEV shall specify the selected device.

5.1.5.3.5 Normal Outputs

Table 26: SMART command for normal outputs information

| Register | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------------|-----|------|-----|-----|-----|----|----|-----|
| Error | Na | | | | | | | |
| Sector Count | Na | | | | | | | |
| LBA Low | Na | | | | | | | |
| LBA Mid | Na | | | | | | | |
| LBA High | Na | | | | | | | |
| Device | Obs | Na | obs | DEV | Na | Na | Na | Na |
| Status | BSY | DRDY | DF | Na | DRQ | Na | Na | ERR |

Device Register-

DEV shall indicate the selected device.

Status register-

BSY will be cleared to zero indicating command completion.

DRDY will be set to one.

DF (Device Fault) will be cleared to zero.

DRQ shall be cleared to zero.

ERR shall be cleared to zero.

5.1.5.3.6 Prerequisites

DRDY set to one. SMART enabled.

5.1.5.3.7 Description

This command disables all SMART capabilities within device.

5.1.6 Read Multiple

5.1.6.1 Command Code

C4h

5.1.6.2 Protocol

PIO data-in

5.1.6.3 Inputs

Table 27: Read multiple command for inputs information

| Register | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------------|--------------|----|-----|-----|------------|---|---|---|
| Features | Na | | | | | | | |
| Sector Count | Sector Count | | | | | | | |
| LBA Low | LBA(7:0) | | | | | | | |
| LBA Mid | LBA(15:8) | | | | | | | |
| LBA High | LBA(23:16) | | | | | | | |
| Device | obs | Na | obs | DEV | LBA(27:24) | | | |
| Command | C4h | | | | | | | |

Sector Count-

Number of sectors to be transferred. A value of 00h specifies that 256 sectors are to be transferred.

LBA Low-

Starting LBA bits (7:0).

LBA Mid-

Starting LBA bits (15:8)

LBA High-

Starting LBA bits (23:16)

Device –

DEV shall specify the selected device.

Bit (3:0) starting LBA bits (27:24)

5.1.6.4 Normal Output

Table 28: Read multiple command for normal output information

| Register | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----------|----|---|---|---|---|---|---|---|
| Error | Na | | | | | | | |

| | | | | | | | | |
|--------------|-----|------|-----|-----|-----|----|----|-----|
| Sector Count | Na | | | | | | | |
| LBA Low | Na | | | | | | | |
| LBA Mid | Na | | | | | | | |
| LBA High | Na | | | | | | | |
| Device | obs | Na | obs | DEV | Na | Na | Na | Na |
| Status | BSY | DRDY | DF | Na | DRQ | Na | Na | ERR |

Device register-

DEV shall specify the selected device.

Status register

BSY will be cleared to zero indicating command completion

DRDY will be set to one.

DF (Device Fault) will be cleared to zero.

DRQ will be cleared to zero

ERR will be cleared to zero.

5.1.6.5 Error Outputs

An unrecoverable error encountered during the execution of this command results in the termination of the command. The Command Block registers contain the address of the sector where the first unrecoverable error occurred. The amount of data transferred is indeterminate.

Table 29: Read multiple command for error output information

| | | | | | | | | |
|--------------|------------|------|-----|------|------------|------|----|-----|
| Register | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Error | Na | UNC | MC | IDNF | MCR | ABRT | NM | Obs |
| Sector Count | Na | | | | | | | |
| LBA Low | LBA(7:0) | | | | | | | |
| LBA Mid | LBA(15:8) | | | | | | | |
| LBA High | LBA(23:16) | | | | | | | |
| Device | obs | Na | obs | DEV | LBA(27:24) | | | |
| Status | BSY | DRDY | DF | Na | DRQ | Na | Na | ERR |

Error register-

UNC shall be set to one if data is uncorrectable.

IDNF shall be set to one if a user-accessible address is requested could not be found.

LBA Low, LBA Mid, and LBA High, Device

Shall be written with the address of first unrecoverable error.

Status register

BSY will be cleared to zero indicating command completion

DRDY will be set to one.

DF (Device Fault) will be cleared to zero.

DRQ will be cleared to zero

ERR will be set to one if an Error register bit is set to one.

5.1.6.6 Prerequisites

DRDY set to one.

5.1.6.7 Description

This command reads the number of sectors specified in the sector Count register.

The number of sectors per block is defined by the content of word 59 in the IDENTIFY DEVICE response.

5.1.7 Read Sector(s)

5.1.7.1 Command Code

20h

5.1.7.2 Protocol

PIO data-in

5.1.7.3 Inputs

Table 30: Read sector command for inputs information

| Register | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------------|--------------|----|-----|-----|------------|---|---|---|
| Features | Na | | | | | | | |
| Sector Count | Sector Count | | | | | | | |
| LBA Low | LBA(7:0) | | | | | | | |
| LBA Mid | LBA(15:8) | | | | | | | |
| LBA High | LBA(23:16) | | | | | | | |
| Device | obs | Na | obs | DEV | LBA(27:24) | | | |
| Command | 20h | | | | | | | |

Sector Count-

Number of sectors to be transferred. A value of 00h specifies that 256 sectors are to be transferred.

LBA Low-

Starting LBA bits (7:0).

LBA Mid-

Starting LBA bits (15:8)

LBA High-

Starting LBA bits (23:16)

Device –

DEV shall specify the selected device.

Bit (3:0) starting LBA bits (27:24)

5.1.7.4 Normal Output

Table 31: Read sector command for normal outputs information

| Register | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------------|----|---|---|---|---|---|---|---|
| Error | Na | | | | | | | |
| Sector Count | Na | | | | | | | |
| LBA Low | Na | | | | | | | |
| LBA Mid | Na | | | | | | | |

| | | | | | | | | |
|----------|-----|------|-----|-----|-----|----|----|-----|
| LBA High | Na | | | | | | | |
| Device | obs | Na | obs | DEV | Na | Na | Na | Na |
| Status | BSY | DRDY | DF | Na | DRQ | Na | Na | ERR |

Device register-

DEV shall specify the selected device.

Status register

BSY will be cleared to zero indicating command completion

DRDY will be set to one.

DF (Device Fault) will be cleared to zero.

DRQ will be cleared to zero

ERR will be cleared to zero.

5.1.7.5 Error Outputs

An unrecoverable error encountered during the execution of this command results in the termination of the command. The Command Block registers contain the address of the sector where the first unrecoverable error occurred. The amount of data transferred us indeterminate.

Table 32: Read sector command for error outputs information

| | | | | | | | | |
|--------------|------------|------|-----|------|------------|------|----|-----|
| Register | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Error | Na | UNC | MC | IDNF | MCR | ABRT | NM | Obs |
| Sector Count | Na | | | | | | | |
| LBA Low | LBA(7:0) | | | | | | | |
| LBA Mid | LBA(15:8) | | | | | | | |
| LBA High | LBA(23:16) | | | | | | | |
| Device | obs | Na | obs | DEV | LBA(27:24) | | | |
| Status | BSY | DRDY | DF | Na | DRQ | Na | Na | ERR |

Error register-

UNC shall be set to one if data is uncorrectable.

IDNF shall be set to one if a user-accessible address is requested could not be found.

LBA Low, LBA Mid, and LBA High, Device

Shall be written with the address of first unrecoverable error.

Status register

BSY will be cleared to zero indicating command completion

DRDY will be set to one.

DF (Device Fault) will be cleared to zero.

DRQ will be cleared to zero

ERR will be set to one if an Error register bit is set to one.

5.1.7.6 Prerequisites

DRDY set to one.

5.1.7.7 Description

This command reads from 1 to 256 sectors as specified in the Sector Count register. A sector

count of 0 requests 256 sectors. This transfer shall begin at the sector specified in the LBA Low, LBA Mid, LBA High, and Device registers.

The DRQ bit is always set to one prior to data transfer regardless of the presence or absence of an error condition. The device shall interrupt for each DRQ block transferred.

5.1.8 Read Verify Sector

5.1.8.1 Command Code

40h

5.1.8.2 Protocol

Non-data

5.1.8.3 Inputs

Table 33: Read verify sector command for inputs information

| Register | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------------|--------------|----|-----|-----|------------|---|---|---|
| Features | Na | | | | | | | |
| Sector Count | Sector Count | | | | | | | |
| LBA Low | LBA(7:0) | | | | | | | |
| LBA Mid | LBA(15:8) | | | | | | | |
| LBA High | LBA(23:16) | | | | | | | |
| Device | obs | Na | obs | DEV | LBA(27:24) | | | |
| Command | 40h | | | | | | | |

Sector Count-

Number of sectors to be transferred. A value of 00h specifies that 256 sectors are to be transferred.

LBA Low-

Starting LBA bits (7:0).

LBA Mid-

Starting LBA bits (15:8)

LBA High-

Starting LBA bits (23:16)

Device –

The LBA bit shall be set to one to specify the address is an LBA.

DEV shall specify the selected device.

Bit (3:0) starting LBA bits (27:24)

5.1.8.4 Normal Output

Table 34: Read verify sector command for normal output information

| Register | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------------|----|---|---|---|---|---|---|---|
| Error | Na | | | | | | | |
| Sector Count | Na | | | | | | | |
| LBA Low | Na | | | | | | | |
| LBA Mid | Na | | | | | | | |

| | | | | | | | | |
|----------|-----|------|-----|-----|-----|----|----|-----|
| LBA High | Na | | | | | | | |
| Device | obs | Na | obs | DEV | Na | Na | Na | Na |
| Status | BSY | DRDY | DF | Na | DRQ | Na | Na | ERR |

Device register-

DEV shall specify the selected device.

Status register

BSY will be cleared to zero indicating command completion

DRDY will be set to one.

DF (Device Fault) will be cleared to zero.

DRQ will be cleared to zero

ERR will be cleared to zero.

5.1.8.5 Error Outputs

An unrecoverable error encountered during the execution of this command results in the termination of the command. The Command Block registers contain the address of the sector where the first unrecoverable error occurred.

Table 35: Read verify sector command for normal output information

| | | | | | | | | |
|--------------|------------|------|-----|------|------------|------|----|-----|
| Register | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Error | Na | UNC | MC | IDNF | MCR | ABRT | NM | Obs |
| Sector Count | Na | | | | | | | |
| LBA Low | LBA(7:0) | | | | | | | |
| LBA Mid | LBA(15:8) | | | | | | | |
| LBA High | LBA(23:16) | | | | | | | |
| Device | obs | Na | obs | DEV | LBA(27:24) | | | |
| Status | BSY | DRDY | DF | Na | DRQ | Na | Na | ERR |

Error register-

UNC shall be set to one if data is uncorrectable.

IDNF shall be set to one if a user-accessible address could not be found.

LBA Low, LBA Mid, and LBA High, Device

Shall be written with the address of first unrecoverable error.

Status register

BSY will be cleared to zero indicating command completion

DRDY will be set to one.

DF (Device Fault) will be cleared to zero.

DRQ will be cleared to zero

ERR will be set to one if an Error register bit is set to one.

5.1.8.6 Prerequisites

DRDY set to one.

5.1.8.7 Description

This command is identical to the READ SECTOR(s) command, except that the device shall have read the data from the SSD, the DRQ bit is never set to one, and no data is transferred to

the host.

5.1.9 Read DMA

5.1.9.1 Command Code

C8h

5.1.9.2 Protocol

DMA

5.1.9.3 Inputs

Table 36: Read DMA command for inputs information

| Register | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------------|--------------|----|-----|-----|------------|---|---|---|
| Features | Na | | | | | | | |
| Sector Count | Sector Count | | | | | | | |
| LBA Low | LBA(7:0) | | | | | | | |
| LBA Mid | LBA(15:8) | | | | | | | |
| LBA High | LBA(23:16) | | | | | | | |
| Device | obs | Na | obs | DEV | LBA(27:24) | | | |
| Command | C4h | | | | | | | |

Sector Count-

Number of sectors to be transferred. A value of 00h specifies that 256 sectors are to be transferred.

LBA Low-

Starting LBA bits (7:0).

LBA Mid-

Starting LBA bits (15:8)

LBA High-

Starting LBA bits (23:16)

Device –

DEV shall specify the selected device.

Bit (3:0) starting LBA bits (27:24)

5.1.9.4 Normal Output

Table 37: Read DMA command for normal output information

| Register | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------------|-----|------|-----|-----|-----|----|----|-----|
| Error | Na | | | | | | | |
| Sector Count | Na | | | | | | | |
| LBA Low | Na | | | | | | | |
| LBA Mid | Na | | | | | | | |
| LBA High | Na | | | | | | | |
| Device | obs | Na | obs | DEV | Na | Na | Na | Na |
| Status | BSY | DRDY | DF | Na | DRQ | Na | Na | ERR |

Device register-

DEV shall specify the selected device.

Status register

BSY will be cleared to zero indicating command completion

DRDY will be set to one.

DF (Device Fault) will be cleared to zero.

DRQ will be cleared to zero

ERR will be cleared to zero.

5.1.9.5 Error Outputs

An unrecoverable error encountered during the execution of this command results in the termination of the command. The Command Block registers contain the address of the sector where the first unrecoverable error occurred. The amount of data transferred is indeterminate.

Table 38: Read DMA command for error output information

| Register | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------------|------------|------|-----|------|------------|------|----|-----|
| Error | ICRC | UNC | MC | IDNF | MCR | ABRT | NM | Obs |
| Sector Count | Na | | | | | | | |
| LBA Low | LBA(7:0) | | | | | | | |
| LBA Mid | LBA(15:8) | | | | | | | |
| LBA High | LBA(23:16) | | | | | | | |
| Device | Obs | Na | obs | DEV | LBA(27:24) | | | |
| Status | BSY | DRDY | DF | Na | DRQ | Na | Na | ERR |

Error register-

ICRC shall be set to one if an interface CRC error has occurred during an Ultra DMA data transfer. The content of this bit is not applicable for Multiword DMA transfers.

UNC shall be set to one if data is uncorrectable.

IDNF shall be set to one if a user-accessible address could not be found.

LBA Low, LBA Mid, and LBA High, Device

Shall be written with the address of first unrecoverable error.

Status register

BSY will be cleared to zero indicating command completion

DRDY will be set to one.

DF (Device Fault) will be cleared to zero.

DRQ will be cleared to zero

ERR will be set to one if an Error register bit is set to one.

5.1.9.6 Prerequisites

DRDY set to one. The host shall initialize the DMA channel.

5.1.9.7 Description

The READ DMA command allows the host to read data using the DMA data transfer protocol.

5.1.10 Set Multiple Mode

5.1.10.1 Command Code

C6h

5.1.10.2 Protocol

Non-data

5.1.10.3 Inputs

If the content of the Sector Count Register is not zero, then the Sector Count register contains the number of sectors per block for the device to be used on all following READ/WRITE MULTIPLE commands. The content of the Sector Count register shall be less than or equal to the value in bits (7:0) in word 47 in the IDENTIFY DEVICE information. The host should set the content of the Sector Count register to 1.

Table 39: Set multiple mode command for inputs information

| Register | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------------|------------------|----|-----|-----|----|---|---|---|
| Features | Na | | | | | | | |
| Sector Count | Sector per block | | | | | | | |
| LBA Low | Na | | | | | | | |
| LBA Mid | Na | | | | | | | |
| LBA High | Na | | | | | | | |
| Device | obs | Na | obs | DEV | Na | | | |
| Command | C6h | | | | | | | |

5.1.10.4 Normal Output

Table 40: Set multiple mode command for normal output information

| Register | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------------|-----|------|-----|-----|-----|----|----|-----|
| Error | Na | | | | | | | |
| Sector Count | Na | | | | | | | |
| LBA Low | Na | | | | | | | |
| LBA Mid | Na | | | | | | | |
| LBA High | Na | | | | | | | |
| Device | obs | Na | obs | DEV | Na | Na | Na | Na |
| Status | BSY | DRDY | DF | Na | DRQ | Na | Na | ERR |

Device register-

DEV shall specify the selected device.

Status register

BSY will be cleared to zero indicating command completion

DRDY will be set to one.

DF (Device Fault) will be cleared to zero.

DRQ will be cleared to zero

ERR will be cleared to zero.

5.1.10.5 Error Outputs

Table 41: Set multiple mode command for error outputs information

| Register | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----------|---|---|---|---|---|---|---|---|
|----------|---|---|---|---|---|---|---|---|

| | | | | | | | | |
|--------------|-----|------|-----|-----|-----|------|----|-----|
| Error | Na | Na | obs | Na | Na | ABRT | Na | Na |
| Sector Count | Na | | | | | | | |
| LBA Low | Na | | | | | | | |
| LBA Mid | Na | | | | | | | |
| LBA High | Na | | | | | | | |
| Device | Obs | Na | obs | DEV | Na | | | |
| Status | BSY | DRDY | DF | Na | DRQ | Na | Na | ERR |

Status register

BSY will be cleared to zero indicating command completion

DRDY will be set to one.

DF (Device Fault) will be cleared to one if a device fault has occurred.

DRQ will be cleared to zero

ERR will be set to one if an Error register bit is set to one.

5.1.10.6 Prerequisites

DRDY set to one.

5.1.10.7 Description

This command establishes the block count for READ MULTIPLE, READ MULTI EXT, WRITE MULTIPLE.

SSD can only support 1 sector per block.

5.1.11 Set Sleep Mode

5.1.11.1 Command Code

E6h

5.1.11.2 Protocol

Non-data

5.1.11.3 Inputs

Table 42: Set sleep mode for inputs information

| | | | | | | | | |
|--------------|-----|----|-----|-----|----|---|---|---|
| Register | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Features | Na | | | | | | | |
| Sector Count | Na | | | | | | | |
| LBA Low | Na | | | | | | | |
| LBA Mid | Na | | | | | | | |
| LBA High | Na | | | | | | | |
| Device | obs | Na | obs | DEV | Na | | | |
| Command | E6h | | | | | | | |

Device register–

DEV shall specify the selected device.

5.1.11.4 Normal Output

Table 43: Set sleep mode for normal output information

| | | | | | | | | |
|----------|---|---|---|---|---|---|---|---|
| Register | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----------|---|---|---|---|---|---|---|---|

| | | | | | | | | |
|--------------|-----|------|-----|-----|-----|----|----|-----|
| Error | Na | | | | | | | |
| Sector Count | Na | | | | | | | |
| LBA Low | Na | | | | | | | |
| LBA Mid | Na | | | | | | | |
| LBA High | Na | | | | | | | |
| Device | obs | Na | obs | DEV | Na | Na | Na | Na |
| Status | BSY | DRDY | DF | Na | DRQ | Na | Na | ERR |

Device register-

DEV shall specify the selected device.

Status register

BSY will be cleared to zero indicating command completion

DRDY will be set to one.

DF (Device Fault) will be cleared to zero.

DRQ will be cleared to zero

ERR will be cleared to zero.

5.1.11.5 Error Outputs

Table 44: Set sleep mode for error output information

| | | | | | | | | |
|--------------|-----|------|-----|-----|-----|------|----|-----|
| Register | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Error | Na | Na | Na | Na | Na | ABRT | Na | Na |
| Sector Count | Na | | | | | | | |
| LBA Low | Na | | | | | | | |
| LBA Mid | Na | | | | | | | |
| LBA High | Na | | | | | | | |
| Device | Obs | Na | obs | DEV | Na | | | |
| Status | BSY | DRDY | DF | Na | DRQ | Na | Na | ERR |

Status register

BSY will be cleared to zero indicating command completion

DRDY will be set to one.

DF (Device Fault) will be set to one if a device fault has occurred.

DRQ will be cleared to zero

ERR will be set to one if an Error register bit is set to one.

5.1.11.6 Prerequisites

DRDY set to one.

5.1.11.7 Description

This command is the only way to cause the device to enter Sleep mode.

5.1.12 Flush Cache

5.1.12.1 Command Code

E7h

5.1.12.2 Protocol

Non-data

5.1.12.3 Inputs

Table 45: Flush cache command for inputs information

| Register | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------------|-----|----|-----|-----|----|---|---|---|
| Features | Na | | | | | | | |
| Sector Count | Na | | | | | | | |
| LBA Low | Na | | | | | | | |
| LBA Mid | Na | | | | | | | |
| LBA High | Na | | | | | | | |
| Device | obs | Na | obs | DEV | Na | | | |
| Command | E7h | | | | | | | |

Device register–

DEV shall specify the selected device.

5.1.12.4 Normal Output

Table 46: Flush cache command for normal output information

| Register | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------------|-----|------|-----|-----|-----|----|----|-----|
| Error | Na | | | | | | | |
| Sector Count | Na | | | | | | | |
| LBA Low | Na | | | | | | | |
| LBA Mid | Na | | | | | | | |
| LBA High | Na | | | | | | | |
| Device | obs | Na | obs | DEV | Na | Na | Na | Na |
| Status | BSY | DRDY | DF | Na | DRQ | Na | Na | ERR |

Device register-

DEV shall specify the selected device.

Status register

BSY will be cleared to zero indicating command completion

DRDY will be set to one.

DF (Device Fault) will be cleared to zero.

DRQ will be cleared to zero

ERR will be cleared to zero.

5.1.12.5 Error Outputs

Table 47: Flush cache command for error output information

| Register | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------------|------------|----|-----|-----|------------|------|----|----|
| Error | Na | Na | Na | Na | Na | ABRT | Na | Na |
| Sector Count | Na | | | | | | | |
| LBA Low | LBA(7:0) | | | | | | | |
| LBA Mid | LBA(15:8) | | | | | | | |
| LBA High | LBA(23:16) | | | | | | | |
| Device | Obs | Na | obs | DEV | LBA(27:24) | | | |

| | | | | | | | | |
|--------|-----|------|----|----|-----|----|----|-----|
| Status | BSY | DRDY | DF | Na | DRQ | Na | Na | ERR |
|--------|-----|------|----|----|-----|----|----|-----|

Error register-

ABRT may be set to one if the device is not able to complete the action requested by the command.

LBA Low, LBA Mid, and LBA High, Device

Shall be written with the address of first unrecoverable error.

Status register

BSY will be cleared to zero indicating command completion

DRDY will be set to one.

DF (Device Fault) will be cleared to one if a device fault has occurred.

DRQ will be cleared to zero

ERR will be set to one if an Error register bit is set to one.

5.1.12.6 Prerequisites

DRDY set to one.

5.1.12.7 Description

This command is used by the host to request the device to flush the write cache. If there is data in write cache, that data shall be written to the SSD. The BSY bit shall remain set to one until all data has been successfully written or an error occurs.

5.1.13 Standby

5.1.13.1 Command Code

E2h

5.1.13.2 Protocol

Non-data

5.1.13.3 Inputs

The value in the Sector Count register when the STANDBY command is issued shall determine the time period programmed into the Standby timer.

Table 48: Standby command for inputs information

| Register | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------------|-------------------|----|-----|-----|----|---|---|---|
| Features | Na | | | | | | | |
| Sector Count | Time period value | | | | | | | |
| LBA Low | Na | | | | | | | |
| LBA Mid | Na | | | | | | | |
| LBA High | Na | | | | | | | |
| Device | obs | Na | obs | DEV | Na | | | |
| Command | E2h | | | | | | | |

Device register-

DEV shall specify the selected device.

5.1.13.4 Normal Output

Table 49: Standby command for normal output information

| | | | | | | | | |
|--------------|-----|------|-----|-----|-----|----|----|-----|
| Register | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Error | Na | | | | | | | |
| Sector Count | Na | | | | | | | |
| LBA Low | Na | | | | | | | |
| LBA Mid | Na | | | | | | | |
| LBA High | Na | | | | | | | |
| Device | obs | Na | obs | DEV | Na | Na | Na | Na |
| Status | BSY | DRDY | DF | Na | DRQ | Na | Na | ERR |

Device register-

DEV shall specify the selected device.

Status register

BSY will be cleared to zero indicating command completion

DRDY will be set to one.

DF (Device Fault) will be cleared to zero.

DRQ will be cleared to zero

ERR will be cleared to zero.

5.1.13.5 Error Outputs

Table 50: Standby command for error output information

| | | | | | | | | |
|--------------|-----|------|-----|-----|-----|------|----|-----|
| Register | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Error | Na | Na | Na | Na | Na | ABRT | Na | Na |
| Sector Count | Na | | | | | | | |
| LBA Low | Na | | | | | | | |
| LBA Mid | Na | | | | | | | |
| LBA High | Na | | | | | | | |
| Device | Obs | Na | obs | DEV | Na | | | |
| Status | BSY | DRDY | DF | Na | DRQ | Na | Na | ERR |

Error register-

ABRT may be set to one if the device is not able to complete the action requested by the command.

Status register

BSY will be cleared to zero indicating command completion

DRDY will be set to one.

DF (Device Fault) will be set to one if a device fault has occurred.

DRQ will be cleared to zero

ERR will be set to one if an Error register bit is set to one.

5.1.13.6 Prerequisites

DRDY set to one.

5.1.13.7 Description

This command causes the device to enter the Standby mode.

If the Sector Count register is non-zero then Standby timer shall be enabled. The value in the

Sector Count register shall be used determine the time programmed into the Standby timer. If the Sector Count register is zero then the Standby timer is disabled.

5.1.14 Standby Immediate

5.1.14.1 Command Code

E0h

5.1.14.2 Protocol

Non-data

5.1.14.3 Inputs

Table 51: Standby immediate command for inputs information

| Register | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------------|-----|----|-----|-----|----|---|---|---|
| Features | Na | | | | | | | |
| Sector Count | Na | | | | | | | |
| LBA Low | Na | | | | | | | |
| LBA Mid | Na | | | | | | | |
| LBA High | Na | | | | | | | |
| Device | obs | Na | obs | DEV | Na | | | |
| Command | E0h | | | | | | | |

Device register-

DEV shall specify the selected device.

5.1.14.4 Normal Output

Table 52: Standby immediate command for normal output information

| Register | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------------|-----|------|-----|-----|-----|----|----|-----|
| Error | Na | | | | | | | |
| Sector Count | Na | | | | | | | |
| LBA Low | Na | | | | | | | |
| LBA Mid | Na | | | | | | | |
| LBA High | Na | | | | | | | |
| Device | obs | Na | obs | DEV | Na | Na | Na | Na |
| Status | BSY | DRDY | DF | Na | DRQ | Na | Na | ERR |

Device register-

DEV shall specify the selected device.

Status register

BSY will be cleared to zero indicating command completion

DRDY will be set to one.

DF (Device Fault) will be cleared to zero.

DRQ will be cleared to zero

ERR will be cleared to zero.

5.1.14.5 Error Outputs

Table 53: Standby immediate command for error output information

| | | | | | | | | |
|--------------|-----|------|-----|-----|-----|------|----|-----|
| Register | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Error | Na | Na | Na | Na | Na | ABRT | Na | Na |
| Sector Count | Na | | | | | | | |
| LBA Low | Na | | | | | | | |
| LBA Mid | Na | | | | | | | |
| LBA High | Na | | | | | | | |
| Device | Obs | Na | obs | DEV | Na | | | |
| Status | BSY | DRDY | DF | Na | DRQ | Na | Na | ERR |

Error register-

ABRT may be set to one if the device is not able to complete the action requested by the command.

Status register

BSY will be cleared to zero indicating command completion

DRDY will be set to one.

DF (Device Fault) will be set to one if a device fault has occurred.

DRQ will be cleared to zero

ERR will be set to one if an Error register bit is set to one.

5.1.14.6 Prerequisites

DRDY set to one.

5.1.14.7 Description

This command causes the device to immediately enter the Standby mode.

5.1.15 Write Multiple

5.1.15.1 Command Code

C5h

5.1.15.2 Protocol

PIO data-out

5.1.15.3 Inputs

The LBA mid, LBA High, Device, and LBA Low specify the starting sector address to be written.

The Sector Count register specifies the number of sectors to be transferred.

Table 54: Write multiple command for inputs information

| | | | | | | | | |
|--------------|--------------|----|-----|-----|------------|---|---|---|
| Register | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Features | Na | | | | | | | |
| Sector Count | Sector Count | | | | | | | |
| LBA Low | LBA(7:0) | | | | | | | |
| LBA Mid | LBA(15:8) | | | | | | | |
| LBA High | LBA(23:16) | | | | | | | |
| Device | obs | Na | obs | DEV | LBA(27:24) | | | |
| Command | C5h | | | | | | | |

Sector Count-

Number of sectors to be transferred. A value of 00h specifies that 256 sectors shall be transferred.

LBA Low-

Starting LBA bits (7:0)

LBA Mid-

Starting LBA bits (15:8)

LBA High-

Starting LBA bits (23:16)

Device –

The LBA bit shall be set to one to specify the address is an LBA.

DEV shall specify the selected device.

Bits(3:0) starting LBA bits (27:24)

5.1.15.4 Normal Output

Table 55: Write multiple command for normal output information

| Register | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------------|-----|------|-----|-----|-----|----|----|-----|
| Error | Na | | | | | | | |
| Sector Count | Na | | | | | | | |
| LBA Low | Na | | | | | | | |
| LBA Mid | Na | | | | | | | |
| LBA High | Na | | | | | | | |
| Device | obs | Na | obs | DEV | Na | Na | Na | Na |
| Status | BSY | DRDY | DF | Na | DRQ | Na | Na | ERR |

Device register-

DEV shall specify the selected device.

Status register

BSY will be cleared to zero indicating command completion

DRDY will be set to one.

DF (Device Fault) will be cleared to zero.

DRQ will be cleared to zero

ERR will be cleared to zero.

5.1.15.5 Error Outputs

An unrecoverable error encountered during the execution of this command results in the termination of the command. The Command Block register contain the address of the sector where the first unrecoverable error occurred. The amount of data transferred is indeterminate.

Table 56: Write multiple command for normal output information

| Register | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------------|-----------|----|----|------|-----|------|----|----|
| Error | Na | WP | MC | IDNF | MCR | ABRT | NM | Na |
| Sector Count | Na | | | | | | | |
| LBA Low | LBA(7:0) | | | | | | | |
| LBA Mid | LBA(15:8) | | | | | | | |

| | | | | | | | | |
|----------|------------|------|-----|-----|------------|----|----|-----|
| LBA High | LBA(23:16) | | | | | | | |
| Device | Obs | Na | obs | DEV | LBA(27:24) | | | |
| Status | BSY | DRDY | DF | Na | DRQ | Na | Na | ERR |

Error register-

IDNF shall be set to one if a user-accessible address could not be found. IDNF shall be set to one if an address outside of the range user-accessible address is requested if command aborted is not returned.

ABRT shall be set to one if an error, include an ICRC error, has occurred during an Ultra DMA data transfer. ABRT shall be set to one if an address outside of the range of user-accessible address is requested if IDNF is not set to one.

LBA Low, LBA Mid, and LBA High, Device -

Shall be written with the address of first unrecoverable error.

Status register

BSY will be cleared to zero indicating command completion

DRDY will be set to one.

DF (Device Fault) will be set to one if a device fault has occurred.

DRQ will be cleared to zero

ERR will be set to one if an Error register bit is set to one.

5.1.15.6 Prerequisites

DRDY set to one. If bit 8 of IDENTIFY DEVICE word 59 is cleared to zero, a successful SET MULTIPLE MODE command shall proceed a WRITE MULTIPLE command.

5.1.15.7 Description

This command writes the number of sectors specified in the Sector Count register.

The number of sectors per block is defined by the content of word 59 of the IDENTIFY DEVICE response.

When the WRITE MULTIPLE command is issued, the SECTOR Count register contains the number of sectors (not the number of blocks) requested. The device shall interrupt for each DRQ block transferred.

IF the number of requested sectors is not evenly divisible by the block count, as many full blocks as possible are transferred, followed by a final, partial block transfer. The partial block transfer is for n sectors, where:

$$N = \text{Remainder (sector count / block count)}.$$

If the WRITE MULTIPLE command is received when WRITE MULTIPLE commands are disabled, the Write Multiple operation shall be rejected with command aborted.

Device errors encountered during WRITE MULTIPLE commands are posted after the attempted device write of the block or partial block transferred. The command ends with the sector in error, even if the error was in the middle of a block. Subsequent blocks are not transferred in the event of an error.

The contents of the Command Block Registers following the transfer of a data block that had a sector in error are undefined. The host should retry the transfer as individual requests to

obtain valid error information. Interrupt pending is set when the DRQ bit is set to one at the beginning of each block or partial block.

5.1.16 Write Sector

5.1.16.1 Command Code

30h

5.1.16.2 Protocol

PIO data-out

5.1.16.3 Inputs

The LBA mid, LBA High, Device, and LBA Low specify the starting sector address to be written. The Sector Count register specifies the number of sectors to be transferred.

Table 57: Write sector command for inputs information

| Register | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------------|--------------|-----|-----|-----|------------|---|---|---|
| Features | Na | | | | | | | |
| Sector Count | Sector Count | | | | | | | |
| LBA Low | LBA(7:0) | | | | | | | |
| LBA Mid | LBA(15:8) | | | | | | | |
| LBA High | LBA(23:16) | | | | | | | |
| Device | obs | LBA | obs | DEV | LBA(27:24) | | | |
| Command | 30h | | | | | | | |

Sector Count-

Number of sectors to be transferred. A value of 00h specifies that 256 sectors shall be transferred.

LBA Low-

Starting LBA bits (7:0)

LBA Mid-

Starting LBA bits (15:8)

LBA High-

Starting LBA bits (23:16)

Device –

The LBA bit shall be set to one to specify the address is an LBA.

DEV shall specify the selected device.

Bits(3:0) starting LBA bits (27:24)

5.1.16.4 Normal Output

Table 58: Write sector command for inputs information

| Register | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------------|----|---|---|---|---|---|---|---|
| Error | Na | | | | | | | |
| Sector Count | Na | | | | | | | |
| LBA Low | Na | | | | | | | |
| LBA Mid | Na | | | | | | | |

| | | | | | | | | |
|----------|-----|------|-----|-----|-----|----|----|-----|
| LBA High | Na | | | | | | | |
| Device | obs | Na | obs | DEV | Na | Na | Na | Na |
| Status | BSY | DRDY | DF | Na | DRQ | Na | Na | ERR |

Device register-

DEV shall specify the selected device.

Status register

BSY will be cleared to zero indicating command completion

DRDY will be set to one.

DF (Device Fault) will be cleared to zero.

DRQ will be cleared to zero

ERR will be cleared to zero.

5.1.16.5 Error Outputs

An unrecoverable error encountered during the execution if this command results in the termination of the command. The Command Block registers contain the address of the sector where the first unrecoverable error occurred. The amount of data transferred is indeterminate.

Table 59: Write sector command for error outputs information

| | | | | | | | | |
|--------------|------------|------|-----|------|------------|------|----|-----|
| Register | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Error | Na | WP | MC | IDNF | MCR | ABRT | NM | Na |
| Sector Count | Na | | | | | | | |
| LBA Low | LBA(7:0) | | | | | | | |
| LBA Mid | LBA(15:8) | | | | | | | |
| LBA High | LBA(23:16) | | | | | | | |
| Device | Obs | Na | obs | DEV | LBA(27:24) | | | |
| Status | BSY | DRDY | DF | Na | DRQ | Na | Na | ERR |

Error register-

IDNF shall be set to one if a user-accessible address could not be found. IDNF shall be set to one if an address outside of the range of user-accessible addresses is requested if command aborted is not returned.

ABRT shall be set to one if an error, including an ICRC error, has occurred during an Ultra DMA data transfer. ABRT shall be set to one if the device is not able to complete the action requested by the command. ABRT shall be set to one if an address outside of the range of user-accessible addresses is requested if IDNF is not set to one.

LBA Low, LBA Mid, and LBA High, Device

Shall be written with the address of first unrecoverable error.

Status register

BSY will be cleared to zero indicating command completion

DRDY will be set to one.

DF (Device Fault) will be set to one if a device fault has occurred.

DRQ will be cleared to zero

ERR will be set to one if an Error register bit is set to one.

5.1.16.6 Prerequisites

DRDY set to one.

5.1.16.7 Description

This command writes from 1 to 256 sectors as specified in the Sector Count register. A sector count of 0 requests 256 sectors. The device shall interrupt for each DRQ block transferred.

5.1.17 Write DMA

5.1.17.1 Command Code

CAh

5.1.17.2 Protocol

DMA

5.1.17.3 Inputs

The LBA Mid, LBA High, Device, and LBA Low specify the starting sector address to be written. The Sector Count register specifies the number of sectors to be transferred.

Table 60: Write DMA command for input information

| Register | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------------|--------------|-----|-----|-----|------------|---|---|---|
| Features | Na | | | | | | | |
| Sector Count | Sector Count | | | | | | | |
| LBA Low | LBA(7:0) | | | | | | | |
| LBA Mid | LBA(15:8) | | | | | | | |
| LBA High | LBA(23:16) | | | | | | | |
| Device | obs | LBA | obs | DEV | LBA(27:24) | | | |
| Command | CAh | | | | | | | |

Sector Count-

Number of sectors to be transferred. A value of 00h specifies that 256 sectors shall be transferred.

LBA Low-

Starting LBA bits (7:0)

LBA Mid-

Starting LBA bits (15:8)

LBA High-

Starting LBA bits (23:16)

Device –

The LBA bit shall be set to one to specify the address is an LBA.

DEV shall specify the selected device.

Bits (3:0) starting LBA bits (27:24)

Normal Output

Table 61: Write DMA command for normal output information

| Register | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----------|---|---|---|---|---|---|---|---|
| | | | | | | | | |

| | | | | | | | | |
|--------------|-----|------|-----|-----|-----|----|----|-----|
| Error | Na | | | | | | | |
| Sector Count | Na | | | | | | | |
| LBA Low | Na | | | | | | | |
| LBA Mid | Na | | | | | | | |
| LBA High | Na | | | | | | | |
| Device | obs | Na | obs | DEV | Na | Na | Na | Na |
| Status | BSY | DRDY | DF | Na | DRQ | Na | Na | ERR |

Device register-

DEV shall specify the selected device.

Status register

BSY will be cleared to zero indicating command completion

DRDY will be set to one.

DF (Device Fault) will be cleared to zero.

DRQ will be cleared to zero

ERR will be cleared to zero.

5.1.17.4 Error Outputs

Table 62: Write DMA command for error outputs information

| | | | | | | | | |
|--------------|------------|------|-----|------|------------|------|----|-----|
| Register | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Error | ICRC | WP | MC | IDNF | MCR | ABRT | NM | Obs |
| Sector Count | Na | | | | | | | |
| LBA Low | LBA(7:0) | | | | | | | |
| LBA Mid | LBA(15:8) | | | | | | | |
| LBA High | LBA(23:16) | | | | | | | |
| Device | Obs | Na | obs | DEV | LBA(27:24) | | | |
| Status | BSY | DRDY | DF | Na | DRQ | Na | Na | ERR |

Error register-

ICRC shall be set to one if an interface CRC error has occurred during an Ultra DMA data transfer. The content of this bit is not applicable for Multiword DMA transfers.

IDNF shall be set to one if a user-accessible address could not be found. IDNF shall be set to one if an address outside of the range of user-accessible address is requested if command aborted is not returned.

ABRT shall be set to one if an error, including an ICRC error, has occurred during an Ultra DMA data transfer. ABRT shall be set to one if the device is not able to complete the action requested by the command. ABRT shall be set to one if an address outside of the range of user-accessible addresses is requested if IDNF is not set to one.

LBA Low, LBA Mid, and LBA High, Device

Shall be written with the address of first unrecoverable error.

Status register

BSY will be cleared to zero indicating command completion

DRDY will be set to one.

DF (Device Fault) will be set to one if a device fault has occurred.

DRQ will be cleared to zero

ERR will be set to one if an Error register bit is set to one.

5.1.17.5 Prerequisites

DRDY set to one. The host shall initialize the DMA channel.

5.1.17.6 Description

The Write DMA command allows the host to write data using the DMA data transfer protocol.

5.1.18 Execute Device Diagnostic

5.1.18.1 Command Code

90h

5.1.18.2 Feature Set

General feature set

5.1.18.3 Protocol

Device diagnostic

5.1.18.4 Inputs

Only the command code (90h). All other registers shall be ignored.

Table 63: Execute device diagnostic command for inputs information

| Register | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------------|-----|----|-----|----|----|---|---|---|
| Features | Na | | | | | | | |
| Sector Count | Na | | | | | | | |
| LBA Low | Na | | | | | | | |
| LBA Mid | Na | | | | | | | |
| LBA High | Na | | | | | | | |
| Device | obs | Na | obs | Na | Na | | | |
| Command | 90h | | | | | | | |

Device –

DEV shall be ignored.

Normal Outputs

The diagnostic code written into the Error register is an 8-bit code.

Table 64: Execute device diagnostic command for normal outputs information

| Register | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------------|-----------------|------|----|----|-----|----|----|-----|
| Error | Diagnostic Code | | | | | | | |
| Sector Count | Signature | | | | | | | |
| LBA Low | Signature | | | | | | | |
| LBA Mid | Signature | | | | | | | |
| LBA High | Signature | | | | | | | |
| Device | Signature | | | | | | | |
| Status | BSY | DRDY | DF | Na | DRQ | Na | Na | ERR |

Error register-

Diagnostic Code
Sector Count, LBA Low, LBA Mid, LBA High, Device registers
Device signature
Device register
DEV shall be cleared to zero.
Status register
TBD

Table 65: Execute device diagnostic command for status register information

| Code | Description |
|--------|---------------|
| 01h | Device passed |
| Others | Device failed |

5.1.18.5 Error Outputs

Table 10 shows the error information that is returned as a diagnostic code in the Error register.

5.1.18.6 Prerequisites

This command shall be accepted regardless of the state of DRDY.

5.1.18.7 Description

This command shall cause the devices to perform the internal diagnostic tests.

5.1.19 Security Set Password

5.1.19.1 Command Code

F1h

5.1.19.2 Feature Set

Security Mode feature set

5.1.19.3 Protocol

PIO data-out

5.1.19.4 Inputs

Table 66: Security set password command for inputs information

| Register | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------------|-----|----|-----|----|----|---|---|---|
| Features | Na | | | | | | | |
| Sector Count | Na | | | | | | | |
| LBA Low | Na | | | | | | | |
| LBA Mid | Na | | | | | | | |
| LBA High | Na | | | | | | | |
| Device | obs | Na | obs | Na | Na | | | |
| Command | F1h | | | | | | | |

Device –

DEV shall specify the selected device.

Normal Outputs

Table 67: Security set password command for normal outputs information

| Register | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----------|---|---|---|---|---|---|---|---|
|----------|---|---|---|---|---|---|---|---|

| | | | | | | | | |
|--------------|-----|------|-----|-----|-----|----|----|-----|
| Error | Na | | | | | | | |
| Sector Count | Na | | | | | | | |
| LBA Low | Na | | | | | | | |
| LBA Mid | Na | | | | | | | |
| LBA High | Na | | | | | | | |
| Device | obs | Na | obs | DEV | Na | | | |
| Status | BSY | DRDY | DF | Na | DRQ | Na | Na | ERR |

Device register

DEV shall indicate the selected device.

Status register

BSY will be cleared to zero indicating command completion

DRDY will be set to one.

DF (Device Fault) will be set to zero.

DRQ will be cleared to zero

ERR will be set to zero.

5.1.19.5 Error Outputs

Table 68: Security set password command for error outputs information

| Register | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------------|-----|------|-----|-----|-----|------|----|-----|
| Error | Na | Na | Na | Na | Na | ABRT | Na | Na |
| Sector Count | Na | | | | | | | |
| LBA Low | Na | | | | | | | |
| LBA Mid | Na | | | | | | | |
| LBA High | Na | | | | | | | |
| Device | obs | Na | obs | DEV | Na | | | |
| Status | BSY | DRDY | DF | Na | DRQ | Na | Na | ERR |

Error Register

ABRT may be set to one if the device is not able to complete the action requested by the command

Device register

DEV shall indicate the selected device.

Status register

BSY will be cleared to zero indicating command completion

DRDY will be set to one.

DF (Device Fault) should be set to one if a device fault has occurred.

DRQ will be cleared to zero

ERR will be set to one if an Error register bit is set to one.

5.1.19.6 Prerequisites

DRDY set to one.

5.1.19.7 Description

This command transfer 512 byte of data from the host. Table 10 defines the content of this

5.1.20.4 Inputs

Table 71: Security unlock command for inputs information

| Register | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------------|-----|----|-----|----|----|---|---|---|
| Features | Na | | | | | | | |
| Sector Count | Na | | | | | | | |
| LBA Low | Na | | | | | | | |
| LBA Mid | Na | | | | | | | |
| LBA High | Na | | | | | | | |
| Device | obs | Na | obs | Na | Na | | | |
| Command | F2h | | | | | | | |

Device register–

DEV shall specify the selected device.

Normal Outputs

Table 72: Security unlock command for inputs information

| Register | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------------|-----|------|-----|-----|-----|----|----|-----|
| Error | Na | | | | | | | |
| Sector Count | Na | | | | | | | |
| LBA Low | Na | | | | | | | |
| LBA Mid | Na | | | | | | | |
| LBA High | Na | | | | | | | |
| Device | obs | Na | obs | DEV | Na | | | |
| Status | BSY | DRDY | DF | Na | DRQ | Na | Na | ERR |

Device register

DEV shall indicate the selected device.

Status register

BSY will be cleared to zero indicating command completion

DRDY will be set to one.

DF (Device Fault) will be set to zero.

DRQ will be cleared to zero

ERR will be set to zero.

5.1.20.5 Error Outputs

The device shall return aborted if the device is in Frozen mode.

Table 73: Security unlock command for inputs information

| Register | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------------|-----|----|-----|-----|----|------|----|----|
| Error | Na | Na | Na | Na | Na | ABRT | Na | Na |
| Sector Count | Na | | | | | | | |
| LBA Low | Na | | | | | | | |
| LBA Mid | Na | | | | | | | |
| LBA High | Na | | | | | | | |
| Device | obs | Na | obs | DEV | Na | | | |

| | | | | | | | | |
|--------|-----|------|----|----|-----|----|----|-----|
| Status | BSY | DRDY | DF | Na | DRQ | Na | Na | ERR |
|--------|-----|------|----|----|-----|----|----|-----|

Error Register

ABRT may be set to one if the device is not able to complete the action requested by the command

Device register

DEV shall indicate the selected device.

Status register

BSY will be cleared to zero indicating command completion

DRDY will be set to one.

DF (Device Fault) should be set to one if a device fault has occurred.

DRQ will be cleared to zero

ERR will be set to one if an Error register bit is set to one.

5.1.20.6 Prerequisites

DRDY set to one.

5.1.20.7 Description

This command transfers 512 bytes of data from the host. Table13 defines the content of this information. If the Identifier bit is set to Master and the device is in high security level, then the password supplied shall be compared with the stored Master password. If the device is in maximum security level then the unlock shall be rejected.

If the Identifier bit is set to user then the device shall compare the supplied password with the stored User password. If the password compare fails then the device shall return command aborted to the host and decrements the unlock counter. This counter shall be initially set to five and shall decremented for each password mismatch when SECURITY UNLOCK and SECURITY ERASE UNIT commands shall be command aborted until a power-on reset or a hardware reset. SECURITY UNLOCK commands issued when the device is unlocked have no effect on the unlock counter.

5.1.21 Security Erase Prepare

5.1.21.1 Command Code

F3h

5.1.21.2 Feature Set

Security Mode feature set

5.1.21.3 Protocol

Non-data

5.1.21.4 Inputs

Table 74: Security erase prepare command for inputs information

| Register | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------------|----|---|---|---|---|---|---|---|
| Features | Na | | | | | | | |
| Sector Count | Na | | | | | | | |
| LBA Low | Na | | | | | | | |

| | | | | | |
|----------|-----|----|-----|----|----|
| LBA Mid | Na | | | | |
| LBA High | Na | | | | |
| Device | obs | Na | obs | Na | Na |
| Command | F3h | | | | |

Device register–

DEV shall specify the selected device.

Normal Outputs

Table 75: Security erase prepare command for normal outputs information

| Register | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------------|-----|------|-----|-----|-----|----|----|-----|
| Error | Na | | | | | | | |
| Sector Count | Na | | | | | | | |
| LBA Low | Na | | | | | | | |
| LBA Mid | Na | | | | | | | |
| LBA High | Na | | | | | | | |
| Device | obs | Na | obs | DEV | Na | Na | Na | Na |
| Status | BSY | DRDY | DF | Na | DRQ | Na | Na | ERR |

Device register

DEV shall indicate the selected device.

Status register

BSY will be cleared to zero indicating command completion

DRDY will be set to one.

DF (Device Fault) will be set to zero.

DRQ will be cleared to zero

ERR will be set to zero.

5.1.21.5 Error Outputs

The device shall return aborted if the device is in Frozen mode.

Table 76: Security erase prepare command for error outputs information

| Register | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------------|-----|------|-----|-----|-----|------|----|-----|
| Error | Na | Na | Na | Na | Na | ABRT | Na | Na |
| Sector Count | Na | | | | | | | |
| LBA Low | Na | | | | | | | |
| LBA Mid | Na | | | | | | | |
| LBA High | Na | | | | | | | |
| Device | obs | Na | obs | DEV | Na | | | |
| Status | BSY | DRDY | DF | Na | DRQ | Na | Na | ERR |

Error Register

ABRT shall be set to one if the device is in Frozen mode. ABRT may be set to one if the device is not able to complete the action requested by the command

Device register

DEV shall indicate the selected device.

Status register

BSY will be cleared to zero indicating command completion

DRDY will be set to one.

DF (Device Fault) should be set to one if a device fault has occurred.

DRQ will be cleared to zero

ERR will be set to one if an Error register bit is set to one.

5.1.21.6 Prerequisites

DRDY set to one.

5.1.21.7 Description

The SECURITY ERASE PREPARE command shall be issued immediately before the SECURITY ERASE UNIT command to enable device erasing and unlocking. This command prevents accidental loss of data on the device.

5.1.22 Security Erase Unit

5.1.22.1 Command Code

F4h

5.1.22.2 Feature Set

Security Mode feature set

5.1.22.3 Protocol

PIO data-out.

5.1.22.4 Inputs

Table 77: Security erase unit command for inputs information

| Register | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------------|-----|----|-----|----|----|----|----|----|
| Features | Na | | | | | | | |
| Sector Count | Na | | | | | | | |
| LBA Low | Na | | | | | | | |
| LBA Mid | Na | | | | | | | |
| LBA High | Na | | | | | | | |
| Device | obs | Na | obs | Na | Na | Na | Na | Na |
| Command | F4h | | | | | | | |

Device register–

DEV shall specify the selected device.

Normal Outputs

Table 78: Security erase unit command for normal outputs information

| Register | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------------|----|---|---|---|---|---|---|---|
| Error | Na | | | | | | | |
| Sector Count | Na | | | | | | | |
| LBA Low | Na | | | | | | | |
| LBA Mid | Na | | | | | | | |
| LBA High | Na | | | | | | | |

| | | | | | | | | |
|--------|-----|------|-----|-----|-----|----|----|-----|
| Device | obs | Na | obs | DEV | Na | Na | Na | Na |
| Status | BSY | DRDY | DF | Na | DRQ | Na | Na | ERR |

Device register

DEV shall indicate the selected device.

Status register

BSY shall be cleared to zero indicating command completion

DRDY shall be set to one.

DF (Device Fault) will be set to zero.

DRQ shall be cleared to zero

ERR shall be cleared to zero.

5.1.22.5 Error Outputs

The device shall return aborted if the device is in Frozen mode, not preceded by a SECURITY ERASE PREPARE command, if Enhance Erase is specified but not supported, or if the data area is not successfully overwritten.

Table 79: Security erase unit command for error outputs information

| Register | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------------|-----|------|-----|-----|-----|------|----|-----|
| Error | Na | Na | Na | Na | Na | ABRT | Na | Na |
| Sector Count | Na | | | | | | | |
| LBA Low | Na | | | | | | | |
| LBA Mid | Na | | | | | | | |
| LBA High | Na | | | | | | | |
| Device | obs | Na | obs | DEV | Na | | | |
| Status | BSY | DRDY | DF | Na | DRQ | Na | Na | ERR |

Error Register

ABRT shall be set to one if the device is in Frozen mode, not preceded by a SECURITY ERASE PREPARE command, or if the data area is not successfully overwritten. ABRT may be set to one if the device is not able to complete the action requested by the command.

Device register

DEV shall indicate the selected device.

Status register

BSY will be cleared to zero indicating command completion

DRDY will be set to one.

DF (Device Fault) should be set to one if a device fault has occurred.

DRQ will be cleared to zero

ERR will be set to one if an Error register bit is set to one.

5.1.22.6 Prerequisites

DRDY set to one. This command shall be immediately preceded by a SECURITY ERASE PREPARE command.

5.1.22.7 Description

This command transfer 512 bytes of data from the host. Table12 defines the content of this

| | |
|---------|-----|
| Command | F5h |
|---------|-----|

Device register–

DEV shall specify the selected device.

Normal Outputs

Table 82: Security freeze lock for normal outputs information

| Register | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------------|-----|------|-----|-----|-----|----|----|-----|
| Error | Na | | | | | | | |
| Sector Count | Na | | | | | | | |
| LBA Low | Na | | | | | | | |
| LBA Mid | Na | | | | | | | |
| LBA High | Na | | | | | | | |
| Device | Obs | Na | obs | DEV | Na | Na | Na | Na |
| Status | BSY | DRDY | DF | Na | DRQ | Na | Na | ERR |

Device register

DEV shall indicate the selected device.

Status register

BSY shall be cleared to zero indicating command completion

DRDY shall be set to one.

DF (Device Fault) will be set to zero.

DRQ shall be cleared to zero

ERR shall be cleared to zero.

5.1.23.5 Error Outputs

The device shall return aborted if the device is in Frozen mode, not preceded by a SECURITY ERASE PREPARE command, if Enhance Erase is specified but not supported, or if the data area is not successfully overwritten.

Table 83: Security freeze lock for error outputs information

| Register | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------------|-----|------|-----|-----|-----|------|----|-----|
| Error | Na | Na | Na | Na | Na | ABRT | Na | Na |
| Sector Count | Na | | | | | | | |
| LBA Low | Na | | | | | | | |
| LBA Mid | Na | | | | | | | |
| LBA High | Na | | | | | | | |
| Device | Obs | Na | obs | DEV | Na | | | |
| Status | BSY | DRDY | DF | Na | DRQ | Na | Na | ERR |

Error Register

ABRT shall be set to one if the device is in locked mode. ABRT may be set to one if the device is not able to complete the action requested by the command.

Device register

DEV shall indicate the selected device.

Status register

BSY will be cleared to zero indicating command completion

DRDY will be set to one.

DF (Device Fault) should be set to one if a device fault has occurred.

DRQ will be cleared to zero

ERR will be set to one if an Error register bit is set to one.

5.1.23.6 Prerequisites

DRDY set to one.

5.1.23.7 Description

The SECURITY FREEZE LOCK command shall set the device to Frozen mode. After command completion any other commands that update the device Lock mode shall be command aborted. Frozen mode shall be disabled by power-off or hardware reset. If SECURITY FREEZE LOCK shall be issued when the device in Frozen mode, the command executes and the device shall remain in Frozen mode.

Command disabled by SECURITY FREEZE LOCK are:

- SECURITY SET PASSWORD
- SECURITY UNLOCK
- SECURITY DISABLE PASSWORD
- SECURITY ERASE PREPARE
- SECURITY ERASE UNIT

5.1.24 Security Disable Password

5.1.24.1 Command Code

F6h

5.1.24.2 Feature Set

Security Mode feature set

5.1.24.3 Protocol

PIO data-out.

5.1.24.4 Inputs

Table 84: Security disable password command for inputs information

| Register | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------------|-----|----|-----|----|----|----|----|----|
| Features | Na | | | | | | | |
| Sector Count | Na | | | | | | | |
| LBA Low | Na | | | | | | | |
| LBA Mid | Na | | | | | | | |
| LBA High | Na | | | | | | | |
| Device | obs | Na | obs | Na | Na | Na | Na | Na |
| Command | F6h | | | | | | | |

Device register–

DEV shall specify the selected device.

Normal Outputs

Table 85: Security disable password command for normal outputs information

| Register | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------------|-----|------|-----|-----|-----|----|----|-----|
| Error | Na | | | | | | | |
| Sector Count | Na | | | | | | | |
| LBA Low | Na | | | | | | | |
| LBA Mid | Na | | | | | | | |
| LBA High | Na | | | | | | | |
| Device | obs | Na | obs | DEV | Na | Na | Na | Na |
| Status | BSY | DRDY | DF | Na | DRQ | Na | Na | ERR |

Device register

DEV shall indicate the selected device.

Status register

BSY shall be cleared to zero indicating command completion

DRDY shall be set to one.

DF (Device Fault) will be set to zero.

DRQ shall be cleared to zero

ERR shall be cleared to zero.

5.1.24.5 Error Outputs

The device shall return aborted if the device is in Locked mode, or device is in Frozen mode.

Table 86: Security disable password command for error outputs information

| Register | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------------|-----|------|-----|-----|-----|------|----|-----|
| Error | Na | Na | Na | Na | Na | ABRT | Na | Na |
| Sector Count | Na | | | | | | | |
| LBA Low | Na | | | | | | | |
| LBA Mid | Na | | | | | | | |
| LBA High | Na | | | | | | | |
| Device | obs | Na | obs | DEV | Na | | | |
| Status | BSY | DRDY | DF | Na | DRQ | Na | Na | ERR |

Error Register

ABRT may be set to one if the device is not able to complete the action requested by the command.

Device register

DEV shall indicate the selected device.

Status register

BSY will be cleared to zero indicating command completion

DRDY will be set to one.

DF (Device Fault) should be set to one if a device fault has occurred.

DRQ will be cleared to zero

ERR will be set to one if an Error register bit is set to one.

5.1.24.6 Prerequisites

Verification of Compliance

Product Name : **SATA Slim Series**
Model Number : **D1SS-XXXJXXXXXXXX**
Applicant : **InnoDisk Corporation**
Address : **9F., No.100, Sec. 1Xintai5th Rd., Xizhi Dist., New Taipei City
221, Taiwan**
Report Number : **C22-U070-1101-404**
Issue Date : **March 3, 2011**
Applicable Standards : **EN 55022:2006+A1:2007 Class B ITE
EN 55024:1998+A1:2001+A2:2003
EN 61000-4-2:1995+A1:1998+A2:2001
EN 61000-4-3:2006+A1:2008
EN 61000-4-4:2004**

Based on the EMC Directive 2004/108/EC and the specifications of the customer, one sample of the designated product has been tested in our laboratory and found to be in compliance with the EMC standards cited above.



TAF 0905
FCC CAB Code TW1053
NVLAP Lab Code 200575-0
IC Code 4699A
VCCI Accep. No. R-1527, C-1609, T-131, T-1441, G-10



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(Tsun-Yu Shih/ General Manager)

Date: March 3, 2011

Verification of Compliance

Product Name : **SATA Slim Series**
Model Number : **D1SS-XXXJXXXXXX**
Applicant : **InnoDisk Corporation**
Address : **9F., No.100, Sec. 1Xintai5th Rd., Xizhi Dist., New Taipei City
221, Taiwan**
Report Number : **F-U070-1101-404**
Issue Date : **March 3, 2011**

Applicable Standards : **FCC Part 15, Subpart B Class B ITE
ANSI C63.4:2003
Industry Canada ICES-003 Issue 4
CSA-IEC CISPR22: 02 Class B ITE**

One sample of the designated product has been tested in our laboratory and found to be in compliance with the FCC rules cited above.



NVLAP LAB CODE 200575-0

TAF 0905
FCC CAB Code TW1053
IC Code 4699A
VCCI Accep. No. R-1527, C-1609, T-131, T-1441, G-10



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(Tsun-Yu Shih/ General Manager)

Date: March 3, 2011