

# InnoRobust II

## 2.5" SATA SSD

Customer: \_\_\_\_\_

Customer \_\_\_\_\_

Part Number: \_\_\_\_\_

Innodisk \_\_\_\_\_

Part Number: \_\_\_\_\_

Innodisk \_\_\_\_\_

Model Name: \_\_\_\_\_

Date: \_\_\_\_\_

Innodisk Approver	Customer Approver

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## REVISION HISTORY

Revision	Description	Date
Rev. 1.0	First release	NOV. 2012
Rev. 1.1	Remove industrial grade and add extended grade	APR. 2013
Rev. 1.2	1. Correct industrial grade and extended grade information 2. Add Destroy vendor command description	AUG. 2013

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# 1. Product Overview

## 1.1 Introduction of InnoRobust II SATA SSD

InnoRobust II series provides high capacity flash memory Solid State Drive (SSD) that electrically complies with Serial ATA (SATA) II 3.0G standard and delivers excellent performance, for SLC type, sustained read speed can reach up to 170 MB per second (max.) while sustained write reach up to 140 MB per second (max); and complies with ATA protocol and supports TRIM command set.

InnoRobust II SATA SSD is compatible with standard 2.5-inch form factor and designed for military field, which provides several data security functions, including SEraser, QErase, Destroy, and Write Protect.

## 1.2 Product View



Figure 1: InnoRobust II 2.5" SATA SSD

## 1.3 Product Models

InnoRobust II SATA SSD is available in follows capacities, within SLC and MLC flash ICs:

SLC

[InnoRobust II 2.5" SATA SSD 8GB \(SLC\)](#) [InnoRobust II 2.5" SATA SSD 16GB \(SLC\)](#)

[InnoRobust II 2.5" SATA SSD 32GB \(SLC\)](#) [InnoRobust II 2.5" SATA SSD 64GB \(SLC\)](#)

[InnoRobust II 2.5" SATA SSD 128GB \(SLC\)](#) [InnoRobust II 2.5" SATA SSD 256GB \(SLC\)](#)

MLC

[InnoRobust II 2.5" SATA SSD 32GB \(MLC\)](#) [InnoRobust II 2.5" SATA SSD 64GB \(MLC\)](#)

[InnoRobust II 2.5" SATA SSD 128GB \(MLC\)](#) [InnoRobust II 2.5" SATA SSD 256GB \(MLC\)](#)

[InnoRobust II 2.5" SATA SSD 512GB \(MLC\)](#)

## 1.4 SATA Interface

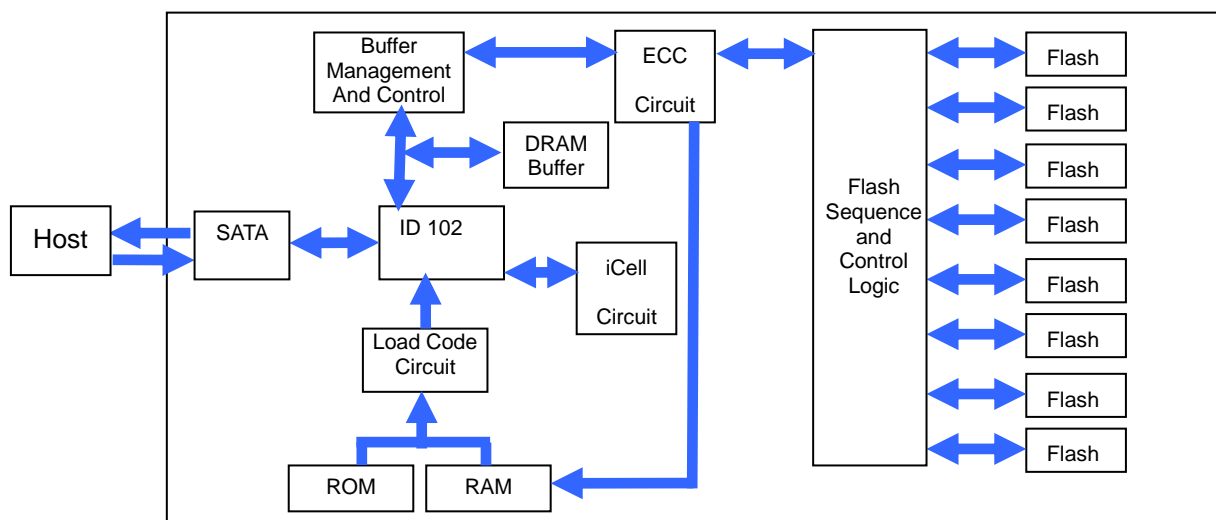
InnoRobust II SATA SSD support SATA II interface, and compliant with SATA I. SATA II interface can work with Serial Attached SCSI (SAS) host system, which is used in server computer. SATA connector uses a 7-pin

signal segment and a 15-pin power segment.

## 2. Theory of operation

### 2.1 Overview

Figure 2 shows the operation of InnoRobust II SATA SSD from the system level, including the major hardware blocks.



**Figure 2: InnoRobust II SATA SSD Block Diagram**

InnoRobust II integrates a SATA II controller and NAND flash memories. Communication with the host occurs through the host interface, using the standard ATA protocol. Communication with the flash device(s) occurs through the flash interface.

### 2.2 SATA II Controller

The SATA II controller is 3.0 Gbps (Gen. 2), and support hot-plug. The Serial ATA physical, link and transport layers are compliant with Serial ATA Gen 1 and Gen 2 specification (Gen 2 supports 1.5Gbps/3.0Gbps data rate). The controller has 8 channels for flash interface.

The controller is equipped with 128KB internal memory for data buffer. iCell circuit is designed with several capacitors to be able to provide power after host power off. The SSD controller can write all DRAM buffer data to flash, so that is why InnoRobust II SATA SSD can ensure all data can be written to disk without any data loss.

### 2.3 Error Detection and Correction

Highly sophisticated Error Correction Code algorithms are implemented. The ECC unit consists of the Parity Unit (parity-byte generation) and the Syndrome Unit (syndrome-byte computation). This unit implements an

algorithm that can correct 24 bits per 1024 bytes in an ECC block. Code-byte generation during write operations, as well as error detection during read operation, is implemented on the fly without any speed penalties.

## 2.4 Wear-Leveling

Flash memory can be erased within a limited number of times. This number is called the **erase cycle limit** or **write endurance limit** and is defined by the flash array vendor. The erase cycle limit applies to each individual erase block in the flash device.

InnoRobust II SATA SSD uses a static wear-leveling algorithm to ensure that consecutive writes of a specific sector are not written physically to the same page/block in the flash. This spreads flash media usage evenly across all pages, thereby extending flash lifetime.

## 2.5 Bad Blocks Management

Bad Blocks are blocks that contain one or more invalid bits whose reliability are not guaranteed. The Bad Blocks may be presented while the SSD is shipped, or may develop during the life time of the SSD. The Bad Blocks will not exceed more than 2% of the total device volume. When the Bad Blocks is detected, it will be flagged, and not be used anymore. The SSD implement Bad Blocks management, Bad Blocks replacement, Error Correct Code to avoid data error occurred. The functions will be enabled automatically to transfer data from Bad Blocks to spare blocks, and correct error bit.

## 2.6 TRIM

TRIM is one of commands of the ATA Data Set Management Command (also called *DisableDeleteNotify*). The command allows the operating system\* to inform the disk which data blocks are no longer in use and can be erased internally to restore the disk space in advance, as well as to ensure endurance and performance.

\* TRIM is supported by Microsoft Windows 7, Windows Server 2008, and newer operating systems.

## 2.7 Thermal Sensor

Within thermal sensor design, the SSD can operate according to the environmental temperature. Once the temperature goes extremely, SSD receives the feedback from thermal sensor and thus it can either change speed or flash access mechanism to stay within temperature limits accordingly. The benefit of thermal sensor design can ensure that SSD prevents any reliability failures due to overheating or supercooling.

## 3. Installation Requirements

### 3.1 InnoRobust II SATA SSD Pin Directions

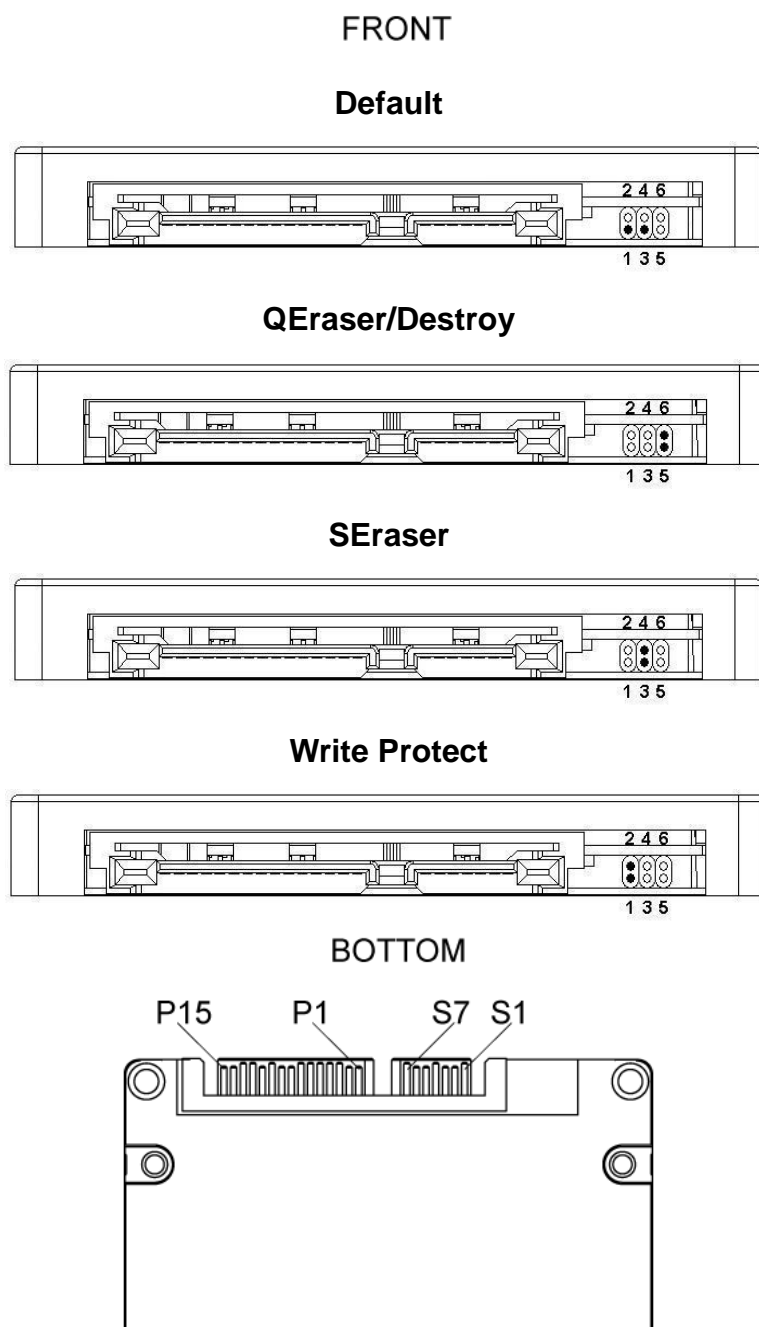


Figure 3: Signal Segment and Power Segment

### 3.2 Electrical Connections for InnoRobust II SATA SSD

A Serial ATA device may be either directly connected to a host or connected to a host through a cable. For connection via cable, the cable should be no longer than 1meter. The SATA interface has a separate connector for the power supply. Please refer to the pin description for further details.

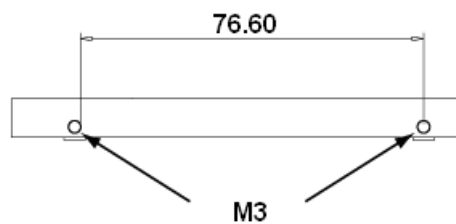
### 3.3 Form Factor

Please prepare following things:

- Screw driver.
- Four M3 screws.
- SATA single cable (7-pin, Maximum length 1 meter).
- SATA power cable (15-pin).

Please turn off your computer, and open your computer's case. Find one of available 2.5-inch slot, and plug the SSD in. To use the screws fix the SSD. Plug in the SATA single cable, and power cable.

Please boot the installation Operation System from CD-ROM, and install Operation System into SSD.



**Figure 4: InnoRobust II SATA SSD Mechanical Screw Hole**

## 4. Specifications

### 4.1 CE and FCC Compatibility

InnoRobust II SATA SSD conforms to CE and FCC requirements.

### 4.2 RoHS Compliance

InnoRobust II SATA SSD is fully compliant with RoHS directive.

### 4.3 Environmental Specifications

InnoRobust II 2.5" SATA SSD is compliant with MIL-STD-810G/F specifications.

#### 4.3.1 Temperature Ranges

Operating Temperature Range:

- Standard Grade : 0°C to +70°C
- Industrial Grade : -40°C to +85°C (SLC only)
- Extended Grade : -20°C to +85°C (MLC only)

Storage Temperature Range:

- -55°C to +95°C

#### 4.3.2 Humidity

Relative Humidity: 5-95%, non-condensing

#### 4.3.3 Shock and Vibration

Table 1: Shock/Vibration Testing for InnoRobust II SATA SSD

Reliability	Test Conditions	Reference Standards
Vibration	20G, 7 Hz to 2K Hz, 3 axes	MIL-STD-810G/F 514.5
Shock	1500G, 0.5ms, 3 axes	MIL-STD-810G/F 516.5

#### 4.3.4 Mean Time between Failures (MTBF)

Table 2 summarizes the MTBF prediction results for InnoRobust II SATA SSD. The analysis was performed using a RAM Commander™ failure rate prediction.

- **Failure Rate:** The total number of failures within an item population, divided by the total number of life units expended by that population, during a particular measurement interval under stated condition.
- **Mean Time between Failures (MTBF):** A basic measure of reliability for repairable items: The mean

number of life units during which all parts of the item perform within their specified limits, during a particular measurement interval under stated conditions.

**Table 2: InnoRobust II SATA SSD MTBF**

Product	Condition	MTBF (Hours)
InnoRobust II SATA SSD	Telcordia SR-332 GB, 25°C	>3,000,000

## 4.4 Transfer Mode

InnoRobust II SATA SSD support following transfer mode:

PIO Mode 0~4

Ultra DMA 0~6

Serial ATA I 1.5Gbps

Serial ATA II 3.0Gbps

## 4.5 Pin Assignment

InnoRobust II SATA SSD uses a standard SATA pin-out. See Table 3 for InnoRobust II SATA SSD pin assignments.

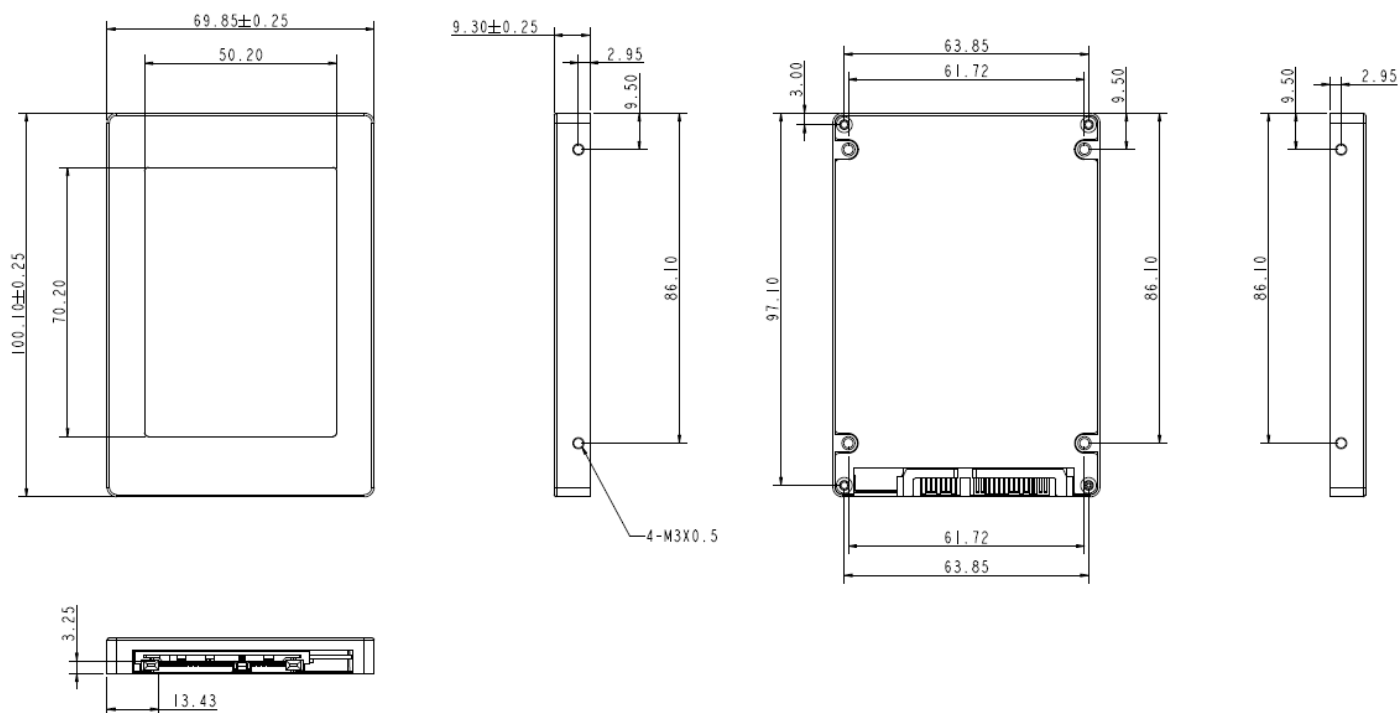
**Table 3: InnoRobust II SATA SSD Pin Assignment**

Name	Type	Description
S1	GND	NA
S2	A+	Differential Signal Pair A
S3	A-	
S4	GND	NA
S5	B-	Differential Signal Pair B
S6	B+	
S7	GND	NA
Key and Spacing separate signal and power segments		
P1	NA	NA
P2	NA	NA
P3	NA	NA
P4	GND	NA
P5	GND	NA
P6	GND	NA
P7	V5	5V Power, Pre-Charge
P8	V5	5V Power
P9	V5	5V Power
P10	GND	NA



P11	DAS/DSS	Device Activity Signal / Disable Staggered Spinup
P12	GND	NA
P13	NA	NA
P14	NA	NA
P15	NA	NA

## 4.6 Mechanical Dimensions



**Figure 5: InnoRobust II 2.5" SATA SSD mechanical dimensions**

## 4.7 Assembly weight

An InnoRobust II SATA SSD within flash ICs, 16GB's weight is 100 grams approx. If the capacity is different, the flash chip's weight needs to be added.

## 4.8 Performance

Burst Transfer Rate: 3.0 Gbps

SLC	8GB	16GB	32GB	64GB	128GB	256GB	
Sequential Read (MB/sec.) (max.)	TBD	TBD	220	170	170	170	
Sequential Write (MB/sec.) (max.)	TBD	TBD	130	140	140	140	

MLC			32GB	64GB	128GB	256GB	512GB
Sequential Read (MB/sec.) (max.)			220	220	220	220	220
Sequential Write (MB/sec.) (max.)			50	70	120	120	120

## 4.9 Seek Time

InnoRobust II SATA SSD is not a magnetic rotating design. There is no seek or rotational latency required.

## 4.10 Hot Plug

The SSD support hot plug function and can be removed or plugged-in during operation. User has to avoid hot plugging the SSD which is configured as boot device and installed operation system.

Surprise hot plug : The insertion of a SATA device into a backplane (combine signal and power) that has power present. The device powers up and initiates an OOB sequence.

Surprise hot removal : The removal of a SATA device from a powered backplane, without first being placed in a quiescent state.

## 4.11 NAND Flash Memory

InnoRobust II SATA SSD uses Single Level Cell (SLC) and Multiple Level Cell (MLC) NAND flash memory, which is non-volatility, high reliability and high speed memory storage. There are two statuses 0 or 1 of one cell for SLC while there are four statuses, 00, 01, 10 and 11 of two cells for MLC. Read or Write data to flash memory for SSD is control by micro processor.

## 4.12 Electrical Specifications

### 4.12.1 Power Requirement

Table 4: InnoRobust II SATA SSD Power Requirement

Item	Symbol	Rating	Unit
Input voltage	V <sub>IN</sub>	+5DC +- 5% 750mA (max.)	V

### 4.12.2 Power Consumption

Table 5: Power Consumption

Mode	Power Consumption
Read	675mA (max.)
Write	750mA (max.)
Idle	480mA (max.)

Target: SLC: 256GB; MLC: 512GB

### 4.13 Device Parameters

InnoRobust II SATA SSD device parameters are shown in Table 6.

**Table 6: Device parameters**

<b>SLC</b>					
<b>Capacity</b>	<b>LBA</b>	<b>Cylinders</b>	<b>Heads</b>	<b>Sectors</b>	<b>User Capacity (MB)</b>
256GB	491520000	16383	16	63	240000
128GB	245760000	16383	16	63	120000
64GB	122880000	16383	16	63	60000
32GB	61440000	16383	16	63	30000
16GB	30720000	16383	16	63	15000
8GB	15360000	15238	16	63	7500
<b>MLC</b>					
<b>Capacity</b>	<b>LBA</b>	<b>Cylinders</b>	<b>Heads</b>	<b>Sectors</b>	<b>User Capacity (MB)</b>
512GB	976442432	16383	16	63	476778
256GB	483721216	16383	16	63	236192
128GB	241860608	16383	16	63	118096
64GB	120930304	16383	16	63	59048
32GB	60465152	16383	16	63	29524

# Supported ATA Commands

## 5.1 Supported ATA Commands

InnoRobust II SATA SSD supports the commands listed in Table 7.

**Table 7: ATA Commands**

Command Name	Code	PARAMETERS USED					
		SC	SN	CY	DR	HD	FT
CHECK POWER MODE	E5h	X	X	X	O	X	X
IDENTIFY DEVICE	ECh	X	X	X	O	X	X
IDLE	E3h	O	X	X	O	X	X
IDLE IMMEDIATE	E1h	X	X	X	O	X	X
READ MULTIPLE	C4h	O	O	O	O	O	X
READ SECTOR(S)	20h	O	O	O	O	O	X
READ VERIFY SECTOR(S)	40h	O	O	O	O	O	X
READ DMA	C8h	O	O	O	O	O	X
SET FEATURES	EFh	O	X	X	O	X	O
SET MULTIPLE MODE	C6h	O	X	X	O	X	X
SLEEP	E6h	X	X	X	O	X	X
FLUSH CACHE	E7h	X	X	X	O	X	X
STANDBY	E2h	X	X	X	O	X	X
STANDBY IMMEDIATE	E0h	X	X	X	O	X	X
WRITE MULTIPLE	C5h	O	O	O	O	O	X
WRITE SECTOR(S)	30h	O	O	O	O	O	X
WRITE DMA	CAh	O	O	O	O	O	X
EXECUTE DIAGNOSTICS	90h	X	X	X	O	X	X
SECURITY SET PASSWORD	F1h	X	X	X	O	X	X
SECURITY UNLOCK	F2	X	X	X	O	X	X
SECURITY ERASE UNIT	F4	X	X	X	O	X	X
SECURITY ERASE PREPARE	F3	X	X	X	O	X	X
SECURITY FREEZE LOCK	F5	X	X	X	O	X	X
SECURITY DISABLE PASSWORD	F6	X	X	X	O	X	X
READ BUFFER	E4h	X	X	X	O	X	X
WRITE BUFFER	E8h	X	X	X	O	X	X

### 5.1.1 Check Power Mode

#### 5.1.1.1 Command Code

E5h

**5.1.1.2 Feature Set**

Power Management feature set.

- This command is mandatory for devices.

-This command is mandatory when the Power Management feature set is implemented.

**5.1.1.3 Protocol**

Non-data command

**5.1.1.4 Inputs****Table 8: Check power mode command for inputs information**

Register	7	6	5	4	3	2	1	0
Features	Na							
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	obs	Na	Obs	DEV	Na	Na	Na	Na
Command	E5h							

Device register

**DEV** shall specify the selected device.**5.1.2 IDENTIFY DEVICE****5.1.2.1 Command Code**

ECh

**5.1.2.2 Feature Set**

General feature set

-Mandatory for all devices.

-Devices implementing the PACKET Command feature set

**5.1.2.3 Protocol**

PIO data-in

**5.1.2.4 Inputs****Table 9: Identify device command for inputs information**

Register	7	6	5	4	3	2	1	0
Features	Na							
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	obs	Na	Obs	DEV	Na	Na	Na	Na

Command	ECh
---------	-----

Device register

**DEV** shall specify the selected device.

#### 5.1.2.5 Outputs

#### 5.1.2.6 Normal outputs

**Table 10: Identify device command for normal outputs information**

Register	7	6	5	4	3	2	1	0
Error	Na							
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	obs	Na	obs	DEV	Na	Na	Na	Na
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Device register

**DEV** shall indicate the selected device.

Status register

**BSY** shall be cleared to zero indicating command completion.

**DRDY** shall be set to one.

**DF** (Device Fault) shall be cleared to zero.

**DRQ** shall be cleared to zero.

**ERR** shall be cleared to zero.

#### 5.1.2.7 Prerequisites

**DRDY** set to one.

#### 5.1.2.8 Description

The IDENTIFY DEVICE command enables the host to receive parameter information from the device. When the command is issued, the device sets the BSY bit to one, prepares to transfer the 256 words of device identification data to the host, sets the DRQ bit to one, clears the BSY bit to zero, and asserts INTRQ if nIEN is cleared to zero. The host may then transfer the data by reading the Data register. Table 8 defines the arrangement and meaning of the parameter words in the buffer. All reserved bits or words shall be zero.

Some parameters are defined as a 16-bit value. A word that is defined as a 16-bit value places the most significant bit of the value on signal line DD15 and the least significant bit on signal line DD0. Some parameters are defined as 32-bit values (e.g. words (61:60)). Such fields are transfer using two successive word transfers. The device will first transfer the least significant bits, bits (15:0) of the value, on signal lines DD(15:0) respectively. After the least significant bits have been transferred, the most significant bits, bits(31:16) of the value, shall be transferred on DD(15:0) respectively.

Some parameters are defined as a string of ASCII characters.

**Table 11: Identify device command parameters**

Word	Description	Value
0	General configuration bit-significant information:  15 0 = ATA device  14-8 Retired  7 1 = removable media device  6 Obsolete  5-3 Retired  2 Response incomplete  1 Retired  0 Reserved	045Ah
1	Obsolete	XXXXh
2	Specific configuration	0000h
3	Obsolete	00XXh
4-5	Retired	0000h
6	Obsolete	XXXXh
7-8	Reserved for assignment by the CompactFlash™ Association	0000h
9	Retired	0000h
10-19	Serial number (20 ASCII characters)	20 ASCII characters
20-21	Retired	0000h
22	Obsolete	0000h
23-26	Firmware revision (8 ASCII characters)	8 ASCII characters
27-46	Model number (40 ASCII characters)	40 ASCII characters
47	15-8 80h 7-0 00h = Reserved 01h-FFh = Maximum number of sectors that shall be transferred per interrupt on READ/WRITE MULTIPLE commands	8001h
48	Reserved	0000h
49	Capabilities  15-14 Reserved for the IDENTIFY PACKET DEVICE command.  13 1 = Standby timer values as specified in this standard are supported 0 = Standby timer values shall be managed by the device  12 Reserved for the IDENTIFY PACKET DEVICE command.	0F00h

	11 1 = IORDY supported 0 = IORDY may be supported 10 1 = IORDY may be disabled 9 1 = LBA supported 8 1 = DMA supported. 7-0 Retired	
50	Capabilities 15 Shell be cleared to zero 14: Shall be set to one 13-2 Reserved 1 Obsolete 0 Shall be set to one to indicate a device specific Standby timer value minimum.	4000h
51	Obsolete	0200h
52	Obsolete	0200h
53	15-3 Reserved 2 1 = the fields reported in word 88 are valid 0 = the fields reported in word 88 are not valid 1 1 = the fields reported in words (70:64) are valid 0 = the fields reported in words (70:64) are not valid 0 Obsolete	0007h
54	Number of current logical cylinders	XXXXh
55	Number of current logical heads	XXXXh
56	Number of current logical sectors per logical track	XXXXh
57-58	Current capacity in sectors	XXXXh
59	15-9 Reserved 8 1 = Multiple sector setting is valid 7-0 xxh = Current setting for number of sectors that shall be transferred per interrupt on R/W Multiple command	01XXh
60-61	Total number of user addressable sectors	XXXXXXXXh
62	Obsolete	0000h
63	15-11 Reserved 10 1 = Multiword DMA mode 2 is selected 0 = Multiword DMA mode 2 is not selected 9 1 = Multiword DMA mode 1 is selected 0 = Multiword DMA mode 1 is not selected 8 1 = Multiword DMA mode 0 is selected 0 = Multiword DMA mode 0 is not selected 7-3 Reserved 2 1 = Multiword DMA mode 2 and below are supported	0X07h



	1      1 = Multiword DMA mode 1 and below are supported 0      1 = Multiword DMA mode 0 is supported	
64	15-8    Reserved 7-0      PIO modes supported	0003h
65	Minimum Multiword DMA transfer cycle time per word 15-0    Cycle time in nanoseconds	0078h
66	Manufacturer's recommended Multiword DMA transfer cycle time 15-0    Cycle time in nanoseconds	0078h
67	Minimum PIO transfer cycle time without flow control 15-0    Cycle time in nanoseconds	00F0h
68	Minimum PIO transfer cycle time with IORDY flow control 15-0    Cycle time in nanoseconds	0078h
69-70	Reserved (for future command overlap and queuing)	0000h
71-74	Reserved for the IDENTIFY PACKET DEVICE command.	0000h
75	Queue depth 15-5    Reserved 4-0      Maximum queue depth - 1	0000h
76-79	Reserved for Serial ATA	0006h 0000h 0040h 0040h
80	Major version number 0000h or FFFFh = device does not report version 15      Reserved 14      Reserved for ATA/ATAPI-14 13      Reserved for ATA/ATAPI-13 12      Reserved for ATA/ATAPI-12 11      Reserved for ATA/ATAPI-11 10      Reserved for ATA/ATAPI-10 9       Reserved for ATA/ATAPI-9 8       Reserved for ATA/ATAPI-8 7       1 = supports ATA/ATAPI-7 6       1 = supports ATA/ATAPI-6 5       1 = supports ATA/ATAPI-5 4       1 = supports ATA/ATAPI-4 3       Obsolete 2       Obsolete 1       Obsolete 0       Reserved	00F0h

81	<p>Minor version number</p> <p>0000h or FFFFh = device does not report version</p> <p>0001h-FFFEh = See 6.17.41</p>	0000h
82	<p>Command set supported.</p> <p>15    Obsolete</p> <p>14    1 = NOP command supported</p> <p>13    1 = READ BUFFER command supported</p> <p>12    1 = WRITE BUFFER command supported</p> <p>11    Obsolete</p> <p>10    1 = Host Protected Area feature set supported</p> <p>9    1 = DEVICE RESET command supported</p> <p>8    1 = SERVICE interrupt supported</p> <p>7    1 = release interrupt supported</p> <p>6    1 = look-ahead supported</p> <p>5    1 = write cache supported</p> <p>4    Shall be cleared to zero to indicate that the PACKET Command feature set is not supported.</p> <p>3    1 = mandatory Power Management feature set supported</p> <p>2    1 = Removable Media feature set supported</p> <p>1    1 = Security Mode feature set supported</p> <p>0    1 = SMART feature set supported</p>	746Bh
83	<p>Command sets supported.</p> <p>15    Shall be cleared to zero</p> <p>14    Shall be set to one</p> <p>13    1 = FLUSH CACHE EXT command supported</p> <p>12    1 = mandatory FLUSH CACHE command supported</p> <p>11    1 = Device Configuration Overlay feature set supported</p> <p>10    1 = 48-bit Address feature set supported</p> <p>9    1 = Automatic Acoustic Management feature set supported</p> <p>8    1 = SET MAX security extension supported</p> <p>7    See Address Offset Reserved Area Boot, INCITS TR27:2001</p> <p>6    1 = SET FEATURES subcommand required to spinup after power-up</p> <p>5    1 = Power-Up In Standby feature set supported</p> <p>4    1 = Removable Media Status Notification feature set supported</p> <p>3    1 = Advanced Power Management feature set supported</p> <p>2    1 = CFA feature set supported</p> <p>1    1 = READ/WRITE DMA QUEUED supported</p> <p>0    1 = DOWNLOAD MICROCODE command supported</p>	7508h

84	<p>Command set/feature supported extension</p> <p>15 Shall be cleared to zero</p> <p>14 Shall be set to one</p> <p>13 1 = IDLE IMMEDIATE with UNLOAD FEATURE supported</p> <p>12 Reserved for technical report</p> <p>11 Reserved for technical report</p> <p>10 1 = URG bit supported for WRITE STREAM DMA EXT and WRITE STREAM EXT</p> <p>9 1 = URG bit supported for READ STREAM DMA EXT and READ STREAM EXT</p> <p>8 1 = 64-bit World wide name supported</p> <p>7 1 = WRITE DMA QUEUED FUA EXT command supported</p> <p>6 1 = WRITE DMA FUA EXT and WRITE MULTIPLE FUA EXT commands supported</p> <p>5 1 = General Purpose Logging feature set supported</p> <p>4 1 = Streaming feature set supported</p> <p>3 1 = Media Card Pass Through Command feature set supported</p> <p>2 1 = Media serial number supported</p> <p>1 1 = SMART self-test supported</p> <p>0 1 = SMART error logging supported</p>	4040h
85	<p>Command and feature sets supported or enabled</p> <p>15 Obsolete</p> <p>14 1 = NOP command enabled</p> <p>13 1 = READ BUFFER command enabled</p> <p>12 1 = WRITE BUFFER command enabled</p> <p>11 Obsolete</p> <p>10 1 = Host Protected Area feature set enabled</p> <p>9 1 = DEVICE RESET command enabled</p> <p>8 1 = SERVICE interrupt enabled</p> <p>7 1 = release interrupt enabled</p> <p>6 1 = look-ahead enabled</p> <p>5 1 = Write Cache enabled</p> <p>4 Shall be cleared to zero to indicate that the PACKET Command feature set is not supported.</p> <p>3 1 = Power Management feature set enabled</p> <p>2 1 = Removable Media feature set enabled</p> <p>1 1 = Security Mode feature set enabled</p> <p>0 1 = SMART feature set enabled</p>	<p>0</p> <p>1</p> <p>1</p> <p>1</p> <p>0</p> <p>1</p> <p>0</p> <p>0</p> <p>0</p> <p>0</p> <p>X</p> <p>X</p> <p>0</p> <p>1</p> <p>0</p> <p>X</p> <p>X</p>
86	<p>Command set/feature enabled</p> <p>15-14 0 = Reserved</p> <p>13 1 = FLUSH CACHE EXT command supported</p> <p>12 1 = FLUSH CACHE command supported</p>	3400h

	11 1 = Device Configuration Overlay supported 10 1 = 48-bit Address features set supported 9 1 = Automatic Acoustic Management feature set enabled 8 1 = SET MAX security extension enabled by SET MAX SET PASSWORD 7 See Address Offset Reserved Area Boot, INCITS TR27:2001 6 1 = SET FEATURES subcommand required to spin-up after power-up 5 1 = Power-Up In Standby feature set enabled 4 1 = Removable Media Status Notification feature set enabled 3 1 = Advanced Power Management feature set enabled 2 1 = CFA feature set enabled 1 1 = READ/WRITE DMA QUEUED command supported 0 1 = DOWNLOAD MICROCODE command supported	
87	Command and feature sets supported or enabled 15 Shall be cleared to zero 14 Shall be set to one 13 1 = IDLE IMMEDIATE with UNLOAD FEATURE supported 12 Reserved for technical report- 11 Reserved for technical report- 10 1 = URG bit supported for WRITE STREAM DMA EXT and WRITE STREAM EXT 9 1 = URG bit supported for READ STREAM DMA EXT and READ STREAM EXT 8 1 = 64 bit World wide name supported 7 1 = WRITE DMA QUEUED FUA EXT command supported 6 1 = WRITE DMA FUA EXT and WRITE MULTIPLE FUA EXT commands supported 5 1 = General Purpose Logging feature set supported 4 1 = Valid CONFIGURE STREAM command has been executed 3 1 = Media Card Pass Through Command feature set enabled 2 1 = Media serial number is valid 1 1 = SMART self-test supported 0 1 = SMART error logging supported	4040h
88	15 Reserved 14 1 = Ultra DMA mode 6 is selected 0 = Ultra DMA mode 6 is not selected 13 1 = Ultra DMA mode 5 is selected 0 = Ultra DMA mode 5 is not selected 12 1 = Ultra DMA mode 4 is selected 0 = Ultra DMA mode 4 is not selected 11 1 = Ultra DMA mode 3 is selected 0 = Ultra DMA mode 3 is not selected 10 1 = Ultra DMA mode 2 is selected	XX7Fh

	<p>0 = Ultra DMA mode 2 is not selected</p> <p>9 1 = Ultra DMA mode 1 is selected</p> <p>0 = Ultra DMA mode 1 is not selected</p> <p>8 1 = Ultra DMA mode 0 is selected</p> <p>0 = Ultra DMA mode 0 is not selected</p> <p>7 Reserved</p> <p>6 1 = Ultra DMA mode 6 and below are supported</p> <p>5 1 = Ultra DMA mode 5 and below are supported</p> <p>4 1 = Ultra DMA mode 4 and below are supported</p> <p>3 1 = Ultra DMA mode 3 and below are supported</p> <p>2 1 = Ultra DMA mode 2 and below are supported</p> <p>1 1 = Ultra DMA mode 1 and below are supported</p> <p>0 1 = Ultra DMA mode 0 is supported</p>	
89	Time required for security erase unit completion	00FFh
90	Time required for Enhanced security erase completion	0000h
91	Current advanced power management value	0000h
92	Master Password Revision Code	FFFEh
93	<p>Hardware reset result. The contents of bits (12:0) of this word shall change only during the execution of a hardware reset.</p> <p>15 Shall be cleared to zero.</p> <p>14 Shall be set to one.</p> <p>13 1 = device detected CBLID- above ViH 0 = device detected CBLID- below ViL</p> <p>12-8 Device 1 hardware reset result. Device 0 shall clear these bits to zero. Device 1 shall set these bits as follows:</p> <p>12 Reserved.</p> <p>11 0 = Device 1 did not assert PDIAG-. 1 = Device 1 asserted PDIAG-.</p> <p>10-9 These bits indicate how Device 1 determined the device number: 00 = Reserved. 01 = a jumper was used. 10 = the CSEL signal was used. 11 = some other method was used or the method is unknown.</p> <p>8 Shall be set to one.</p>	XXXXh

	<p>7-0 Device 0 hardware reset result. Device 1 shall clear these bits to zero. Device 0 shall set these bits as follows:</p> <p>7 Reserved.</p> <p>6 0 = Device 0 does not respond when Device 1 is selected. 1 = Device 0 responds when Device 1 is selected.</p> <p>5 0 = Device 0 did not detect the assertion of DASP-. 1 = Device 0 detected the assertion of DASP-.</p> <p>4 0 = Device 0 did not detect the assertion of PDIAG-. 1 = Device 0 detected the assertion of PDIAG-.</p> <p>3 0 = Device 0 failed diagnostics. 1 = Device 0 passed diagnostics.</p> <p>2-1 These bits indicate how Device 0 determined the device number:</p> <p>00 = Reserved. 01 = a jumper was used. 10 = the CSEL signal was used. 11 = some other method was used or the method is unknown.</p> <p>0 Shall be set to one.</p>	
94	<p>15-8 Vendor's recommended acoustic management value.</p> <p>7-0 Current automatic acoustic management value.</p>	0000h
95	Stream Minimum Request Size	0000h
96	Streaming Transfer Time - DMA	0000h
97	Streaming Access Latency - DMA and PIO	0000h
98-99	Streaming Performance Granularity	0000h
100-103	Maximum user LBA for 48-bit Address feature set.	XXXXh
104	Streaming Transfer Time - PIO	0000h
105	Reserved	0000h
106	<p>Physical sector size / Logical Sector Size</p> <p>15 Shall be cleared to zero</p> <p>14 Shall be set to one</p> <p>13 1 = Device has multiple logical sectors per physical sector.</p> <p>12 1 = Device Logical Sector Longer than 256 Words</p> <p>11-4 Reserved</p> <p>3-0 2 logical sectors per physical sector</p>	4000h
107	Inter-seek delay for ISO-7779 acoustic testing in microseconds	0000h
108	<p>15-12 NAA (3:0)</p> <p>11-0 IEEE OUI (23:12)</p>	0000h
109	<p>15-4 IEEE OUI (11:0)</p> <p>3-0 Unique ID (35:32)</p>	0000h
110	15-0 Unique ID (31:16)	0000h
111	15-0 Unique ID (15:0)	0000h

112-115	Reserved for world wide name extension to 128 bits	0000h
116	Reserved for technical report-	0000h
117-118	Words per Logical Sector	0000h
119-120	Reserved	0000h
121-126	Reserved	0000h
127	Removable Media Status Notification feature set support	0000h
	15-2 Reserved 1-0 00 = Removable Media Status Notification feature set not supported 01 = Removable Media Status Notification feature supported 10 = Reserved 11 = Reserved	
128	Security Status	
	15-9 Reserved	0
	8 Security level 0 = high, 1 = Maximum	X
	7-6 Reserved	0
	5 1= Enhanced security erase supported	0
	4 1= Security count expired	0
	3 1 = Security frozen	X
	2 1 = Security locked	X
	1 1 = Security enabled	X
	0 1 = Security supported	1
129-149	Vendor specific	0000h
150-153	Firmware Version	3230h
		3039h
		3036h
		3234h
154	Secure Function Support	
	7-15 Reserved	0
	6 1= Secure Erase ATA Vendor Command Supported	X
	5 Reserved	0
	4 1=Quick Erase ATA Vendor Command Supported	X
	3 1=Destroy ATA Vendor Command Supported	X
	2 1=Jumper Secure Erase Supported	X
	1 1=Jumper Write Protect Supported	X
	0 1=Jumper Quick Erase Supported	X
155	Secure Function Status(Enable/Disable)	
	2-15 Reserved	
	1 1= Write Protect Enabled	X
	0 Reserved	0

156-158	Vendor Specific	
159	8~15 Function of Jumper "QE" 0x20: Destroy 0x21 or Others: Quick Erase 0~7 Secure Erase Function of Jumper "SE" 0x22: AFFSI 5020 0x23: DoD 5220.22-M 0x24: USA Navy NAVSO P-5239-26 0x25: NSA Manual 130-2 0x26: USA-Army 380-19 0x27: NISPOMSUP Chap 8, Sect. 8-501 0x28: NSA Manual 9-12 0x29: IRIG106	XXXXh
160	CFA power mode 1 15 Word 160 supported 14 Reserved 13 CFA power mode 1 is required for one or more commands implemented by the device 12 CFA power mode 1 disabled 11-0 Maximum current in ma	0000h
161-175	Reserved for assignment by the CompactFlash™ Association	0000h
176-205	Current media serial number	0000h
206-254	Reserved	0000h
255	Integrity word 15-8 Checksum 7-0 Signature	XXXXh

### 5.1.3 IDLE

#### 5.1.3.1 Command Code

E3h

#### 5.1.3.2 Feature Set

Power Management Feature Set.

#### 5.1.3.3 Protocol

Non-Data

#### 5.1.3.4 Inputs

Values other than zero in the Sector Count register when the IDLE command is issued shall determine the time period programmed into the Standby timer.



**Table 12: Idle command for inputs information**

Register	7	6	5	4	3	2	1	0
Features	Na							
Sector Count	Timer period value							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	Obs	Na	Obs	DEV	Na	Na	Na	Na
Command	E3h							

Device register-

**DEV** shall specify the selected device.

**Table 13: Idle command sector count register contents information**

Sector Count register contents	Corresponding timeout period
0 (00h)	Timeout disabled
1-240 (01h-F0h)	(value*5)s
241-251 (F1h-FBh)	((Value-240)*30)min
252 (FCh)	21min
253 (FDh)	Period between 8 and 12 hrs
254 (FEh)	Reserved
255 (FFh)	21 min 15 s
NOTE – Times are approximate	

### 5.1.3.5 Normal Outputs

**Table 14: Idle command for normal outputs information**

Register	7	6	5	4	3	2	1	0
Error	Na							
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	obs	Na	obs	DEV	Na	Na	Na	Na
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Device Register-

**DEV** shall indicate the selected device.

Status register-

**BSY** will be cleared to zero indicating command completion.

**DRDY** will be set to one.

**DF** (Device Fault) will be cleared to zero.

**DRQ** shall be cleared to zero.

**ERR** shall be cleared to zero.

#### 5.1.3.6 Error Outputs

**Table 15: Idle command for error outputs information**

Register	7	6	5	4	3	2	1	0
Error	Na	Na	Na	Na	Na	ABRT	Na	Na
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	obs	Na	obs	DEV	Na			
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

#### 5.1.3.7 Prerequisites

**DRDY** set to one

#### 5.1.3.8 Description

The IDLE command allows the host to place the device in the idle mode and also set the Standby timer.

### 5.1.4 Idle Immediate

#### 5.1.4.1 Command Code

E1h

#### 5.1.4.2 Feature Set

Power Management Feature Set.

#### 5.1.4.3 Protocol

Non-Data

#### 5.1.4.4 Inputs

**Table 16: Idle immediate command for inputs information**

Register	7	6	5	4	3	2	1	0
Features	Na							
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	obs	Na	obs	DEV	Na	Na	Na	Na
Command	E1h							

Device register-

**DEV** shall specify the selected device.

#### 5.1.4.5 Normal Outputs

**Table 17: Idle immediate command for normal outputs information**

Register	7	6	5	4	3	2	1	0
Error	Na							
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	obs	Na	obs	DEV	Na	Na	Na	Na
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Device Register-

**DEV** shall indicate the selected device.

Status register-

**BSY** will be cleared to zero indicating command completion.

**DRDY** will be set to one.

**DF** (Device Fault) will be cleared to zero.

**DRQ** shall be cleared to zero.

**ERR** shall be cleared to zero.

#### 5.1.4.6 Prerequisites

**DRDY** set to one

#### 5.1.4.7 Description

The IDLE IMMEDIATE command allows the host to immediately place the device in the idle mode.

### 5.1.5 Read Multiple

#### 5.1.5.1 Command Code

C4h

#### 5.1.5.2 Protocol

PIO data-in

#### 5.1.5.3 Inputs

**Table 18: Read multiple command for inputs information**

Register	7	6	5	4	3	2	1	0
Features	Na							
Sector Count	Sector Count							
LBA Low	LBA(7:0)							
LBA Mid	LBA(15:8)							

LBA High	LBA(23:16)				
Device	obs	Na	obs	DEV	LBA(27:24)
Command	C4h				

#### Sector Count-

Number of sectors to be transferred. A value of 00h specifies that 256 sectors are to be transferred.

#### LBA Low-

Starting LBA bits (7:0).

#### LBA Mid-

Starting LBA bits (15:8)

#### LBA High-

Starting LBA bits (23:16)

#### Device –

**DEV** shall specify the selected device.

Bit (3:0) starting LBA bits (27:24)

### 5.1.5.4 Normal Output

**Table 19: Read multiple command for normal output information**

Register	7	6	5	4	3	2	1	0
Error	Na							
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	obs	Na	obs	DEV	Na	Na	Na	Na
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

#### Device register-

**DEV** shall specify the selected device.

#### Status register

**BSY** will be cleared to zero indicating command completion

**DRDY** will be set to one.

**DF** (Device Fault) will be cleared to zero.

**DRQ** will be cleared to zero

**ERR** will be cleared to zero.

### 5.1.5.5 Error Outputs

An unrecoverable error encountered during the execution of this command results in the termination of the command. The Command Block registers contain the address of the sector where the first unrecoverable error occurred. The amount of data transferred is indeterminate.

**Table 20: Read multiple command for error output information**

Register	7	6	5	4	3	2	1	0
Error	Na	UNC	MC	IDNF	MCR	ABRT	NM	Obs
Sector Count	Na							
LBA Low	LBA(7:0)							
LBA Mid	LBA(15:8)							
LBA High	LBA(23:16)							
Device	obs	Na	obs	DEV	LBA(27:24)			
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Error register-

**UNC** shall be set to one if data is uncorrectable.

**IDNF** shall be set to one if a user-accessible address is requested could not be found.

LBA Low, LBA Mid, and LBA High, Device

Shall be written with the address of first unrecoverable error.

Status register

**BSY** will be cleared to zero indicating command completion

**DRDY** will be set to one.

**DF** (Device Fault) will be cleared to zero.

**DRQ** will be cleared to zero

**ERR** will be set to one if an Error register bit is set to one.

#### 5.1.5.6 Prerequisites

**DRDY** set to one.

#### 5.1.5.7 Description

This command reads the number of sectors specified in the sector Count register.

The number of sectors per block is defined by the content of word 59 in the IDENTIFY DEVICE response.

### 5.1.6 Read Sector(s)

#### 5.1.6.1 Command Code

20h

#### 5.1.6.2 Protocol

PIO data-in

#### 5.1.6.3 Inputs

**Table 21: Read sector command for inputs information**

Register	7	6	5	4	3	2	1	0
Features	Na							
Sector Count	Sector Count							
LBA Low	LBA(7:0)							
LBA Mid	LBA(15:8)							

LBA High	LBA(23:16)				
Device	obs	Na	obs	DEV	LBA(27:24)
Command	20h				

#### Sector Count-

Number of sectors to be transferred. A value of 00h specifies that 256 sectors are to be transferred.

#### LBA Low-

Starting LBA bits (7:0).

#### LBA Mid-

Starting LBA bits (15:8)

#### LBA High-

Starting LBA bits (23:16)

#### Device –

**DEV** shall specify the selected device.

Bit (3:0) starting LBA bits (27:24)

### 5.1.6.4 Normal Output

**Table 22: Read sector command for normal outputs information**

Register	7	6	5	4	3	2	1	0
Error	Na							
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	obs	Na	obs	DEV	Na	Na	Na	Na
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

#### Device register-

**DEV** shall specify the selected device.

#### Status register

**BSY** will be cleared to zero indicating command completion

**DRDY** will be set to one.

**DF** (Device Fault) will be cleared to zero.

**DRQ** will be cleared to zero

**ERR** will be cleared to zero.

### 5.1.6.5 Error Outputs

An unrecoverable error encountered during the execution of this command results in the termination of the command. The Command Block registers contain the address of the sector where the first unrecoverable error occurred. The amount of data transferred us

indeterminate.

**Table 23: Read sector command for error outputs information**

Register	7	6	5	4	3	2	1	0
Error	Na	UNC	MC	IDNF	MCR	ABRT	NM	Obs
Sector Count	Na							
LBA Low	LBA(7:0)							
LBA Mid	LBA(15:8)							
LBA High	LBA(23:16)							
Device	obs	Na	obs	DEV	LBA(27:24)			
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Error register-

**UNC** shall be set to one if data is uncorrectable.

**IDNF** shall be set to one if a user-accessible address is requested could not be found.

LBA Low, LBA Mid, and LBA High, Device

Shall be written with the address of first unrecoverable error.

Status register

**BSY** will be cleared to zero indicating command completion

**DRDY** will be set to one.

**DF** (Device Fault) will be cleared to zero.

**DRQ** will be cleared to zero

**ERR** will be set to one if an Error register bit is set to one.

#### 5.1.6.6 Prerequisites

**DRDY** set to one.

#### 5.1.6.7 Description

This command reads from 1 to 256 sectors as specified in the Sector Count register. A sector count of 0 requests 256 sectors. This transfer shall begin at the sector specified in the LBA Low, LBA Mid, LBA High, and Device registers. The DRQ bit is always set to one prior to data transfer regardless of the presence or absence of an error condition. The device shall interrupt for each DRQ block transferred.

### 5.1.7 Read Verify Sector

#### 5.1.7.1 Command Code

40h

#### 5.1.7.2 Protocol

Non-data

#### 5.1.7.3 Inputs

**Table 24: Read verify sector command for inputs information**

Register	7	6	5	4	3	2	1	0
Features	Na							
Sector Count	Sector Count							
LBA Low	LBA(7:0)							
LBA Mid	LBA(15:8)							
LBA High	LBA(23:16)							
Device	obs	Na	obs	DEV	LBA(27:24)			
Command	40h							

#### Sector Count-

Number of sectors to be transferred. A value of 00h specifies that 256 sectors are to be transferred.

#### LBA Low-

Starting LBA bits (7:0).

#### LBA Mid-

Starting LBA bits (15:8)

#### LBA High-

Starting LBA bits (23:16)

#### Device –

The LBA bit shall be set to one to specify the address is an LBA.

**DEV** shall specify the selected device.

**Bit** (3:0) starting LBA bits (27:24)

### 5.1.7.4 Normal Output

**Table 25: Read verify sector command for normal output information**

Register	7	6	5	4	3	2	1	0
Error	Na							
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	obs	Na	obs	DEV	Na	Na	Na	Na
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

#### Device register-

**DEV** shall specify the selected device.

#### Status register

**BSY** will be cleared to zero indicating command completion

**DRDY** will be set to one.

**DF** (Device Fault) will be cleared to zero.

**DRQ** will be cleared to zero

**ERR** will be cleared to zero.



### 5.1.7.5 Error Outputs

An unrecoverable error encountered during the execution of this command results in the termination of the command. The Command Block registers contain the address of the sector where the first unrecoverable error occurred.

**Table 26: Read verify sector command for normal output information**

Register	7	6	5	4	3	2	1	0
Error	Na	UNC	MC	IDNF	MCR	ABRT	NM	Obs
Sector Count	Na							
LBA Low	LBA(7:0)							
LBA Mid	LBA(15:8)							
LBA High	LBA(23:16)							
Device	obs	Na	obs	DEV	LBA(27:24)			
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Error register-

**UNC** shall be set to one if data is uncorrectable.

**IDNF** shall be set to one if a user-accessible address could not be found.

LBA Low, LBA Mid, and LBA High, Device

Shall be written with the address of first unrecoverable error.

Status register

**BSY** will be cleared to zero indicating command completion

**DRDY** will be set to one.

**DF** (Device Fault) will be cleared to zero.

**DRQ** will be cleared to zero

**ERR** will be set to one if an Error register bit is set to one.

### 5.1.7.6 Prerequisites

**DRDY** set to one.

### 5.1.7.7 Description

This command is identical to the READ SECTOR(s) command, except that the device shall have read the data from the SSD, the DRQ bit is never set to one, and no data is transferred to the host.

## 5.1.8 Read DMA

### 5.1.8.1 Command Code

C8h

### 5.1.8.2 Protocol

DMA

### 5.1.8.3 Inputs

**Table 27: Read DMA command for inputs information**

Register	7	6	5	4	3	2	1	0
Features	Na							
Sector Count	Sector Count							
LBA Low	LBA(7:0)							
LBA Mid	LBA(15:8)							
LBA High	LBA(23:16)							
Device	obs	Na	obs	DEV	LBA(27:24)			
Command	C4h							

#### Sector Count-

Number of sectors to be transferred. A value of 00h specifies that 256 sectors are to be transferred.

#### LBA Low-

Starting LBA bits (7:0).

#### LBA Mid-

Starting LBA bits (15:8)

#### LBA High-

Starting LBA bits (23:16)

#### Device –

**DEV** shall specify the selected device.

Bit (3:0) starting LBA bits (27:24)

### 5.1.8.4 Normal Output

**Table 28: Read DMA command for normal output information**

Register	7	6	5	4	3	2	1	0
Error	Na							
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	obs	Na	obs	DEV	Na	Na	Na	Na
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

#### Device register-

**DEV** shall specify the selected device.

#### Status register

**BSY** will be cleared to zero indicating command completion

**DRDY** will be set to one.

**DF** (Device Fault) will be cleared to zero.

**DRQ** will be cleared to zero

**ERR** will be cleared to zero.

### 5.1.8.5 Error Outputs

An unrecoverable error encountered during the execution of this command results in the termination of the command. The Command Block registers contain the address of the sector where the first unrecoverable error occurred. The amount of data transferred is indeterminate.

**Table 29: Read DMA command for error output information**

Register	7	6	5	4	3	2	1	0
Error	ICRC	UNC	MC	IDNF	MCR	ABRT	NM	Obs
Sector Count	Na							
LBA Low	LBA(7:0)							
LBA Mid	LBA(15:8)							
LBA High	LBA(23:16)							
Device	Obs	Na	obs	DEV	LBA(27:24)			
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Error register-

**ICRC** shall be set to one if an interface CRC error has occurred during an Ultra DMA data transfer. The content of this bit is not applicable for Multiword DMA transfers.

**UNC** shall be set to one if data is uncorrectable.

**IDNF** shall be set to one if a user-accessible address could not be found.

LBA Low, LBA Mid, and LBA High, Device

Shall be written with the address of first unrecoverable error.

Status register

**BSY** will be cleared to zero indicating command completion

**DRDY** will be set to one.

**DF** (Device Fault) will be cleared to zero.

**DRQ** will be cleared to zero

**ERR** will be set to one if an Error register bit is set to one.

#### 5.1.8.6 Prerequisites

**DRDY** set to one. The host shall initialize the DMA channel.

#### 5.1.8.7 Description

The READ DMA command allows the host to read data using the DMA data transfer protocol.

### 5.1.9 Set Feature

#### 5.1.9.1 Command Code

EFh

#### 5.1.9.2 Feature set

General feature set

- Mandatory for all devices.
- Set transfer mode subcommand is mandatory.
- Enable/disable write cache subcommands are mandatory when a write cache is implemented.
- Enable/disable Media Status Notification sub commands are mandatory if the Removable Media feature set is implemented.

– All other subcommands are optional.

#### 5.1.9.3 Protocol

##### Non-data

#### 5.1.9.4 Inputs

Table 30 defines the value of the subcommand in the Feature register. Some subcommands use other registers, such as the Sector Count register to pass additional information to the device.

**Table 30: Subcommand value of Feature register**

Register	7	6	5	4	3	2	1	0
Features	Subcommand code							
Sector Count	Subcommand specific							
LBA Low	Subcommand specific							
LBA Mid	Subcommand specific							
LBA High	Subcommand specific							
Device	Obs	Na	obs	DEV	na			
Command	EFh							

Device register -

DEV shall specify the selected device.

#### 5.1.9.5 Normal outputs

See the subcommand descriptions.

#### 5.1.9.6 Error outputs

If any subcommand input value is not supported or is invalid, the device shall return command aborted.

**Table 31: Set Features command for error output information**

Register	7	6	5	4	3	2	1	0
Error	na	na	na	na	na	ABRT	na	na
Sector Count	na							
LBA Low	na							
LBA Mid	na							
LBA High	na							
Device	obs	na	obs	DEV	na			
Status	BSY	DRDY	DF	na	DRQ	na	na	ERR

Error register -

ABRT shall be set to one if this subcommand is not supported or if the value is invalid. ABRT may be set to one if the device is not able to complete the action requested by the command.

Device register -

DEV shall indicate the selected device.

Status register -

BSY shall be cleared to zero indicating command completion.

DRDY shall be set to one.

DF (Device Fault) shall be set to one if a device fault has occurred.

DRQ shall be cleared to zero.

ERR shall be set to one if an Error register bit is set to one.

#### 5.1.9.7 Prerequisites

DRDY shall be set to one.

#### 5.1.9.8 Description

This command is used by the host to establish parameters that affect the execution of certain device features. Table 32 defines these features.

At power-on, or after a hardware reset, the default settings of the functions specified by the subcommands are vendor specific

**Table 32: SET FEATURES register definitions**

Value (See note)	
02h	Enable write cache
03h	Set transfer mode based on value in Sector Count register. Table 42 defines values.
55h	Disable read look-ahead feature
82h	Disable write cache
AAh	Enable read look-ahead feature

#### 5.1.9.9 Enable/ disable write cache

Subcommand codes 02h and 82h allow the host to enable or disable write cache in devices that implement write cache. When the subcommand disable write cache is issued, the device shall initiate the sequence to flush cache to non-volatile memory before command completion. This subcommand does not apply to commands that have a Flush to Disk bit.

#### 5.1.9.10 Set transfer mode

A host selects the transfer mechanism by Set Transfer Mode, subcommand code 03h, and specifying a value in the Sector Count register. The upper 5 bits define the type of transfer and the low order 3 bits encode the mode value. The host may change the selected modes by the SET FEATURES command.

**Table 33: Transfer mode values**

Mode	Bits (7:3)	Bits (2:0)
PIO default mode	00000b	000b
PIO default mode, disable IORDY	00000b	001b
PIO flow control transfer mode	00001b	Mode
Retired	00010b	Na

Multiword DMA mode	00100b	Mode
Reserved	01000b	Mode
Mode = transfer mode number	10000b	na
Mode = transfer mode number		

#### 5.1.9.11 Enable/disable read look-ahead

Subcommand codes AAh and 55h allow the host to request the device to enable or disable read look-ahead.

Error recovery performed by the device is vendor specific.

### 5.1.10 Set Multiple Mode

#### 5.1.10.1 Command Code

C6h

#### 5.1.10.2 Protocol

Non-data

#### 5.1.10.3 Inputs

If the content of the Sector Count Register is not zero, then the Sector Count register contains the number of sectors per block for the device to be used on all following READ/WRITE MULTIPLE commands. The content of the Sector Count register shall be less than or equal to the value in bits (7:0) in word 47 in the IDENTIFY DEVICE information. The host should set the content of the Sector Count register to 1.

**Table 34: Set multiple mode command for inputs information**

Register	7	6	5	4	3	2	1	0
Features	Na							
Sector Count	Sector per block							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	obs	Na	obs	DEV	Na			
Command	C6h							

#### 5.1.10.4 Normal Output

**Table 35: Set multiple mode command for normal output information**

Register	7	6	5	4	3	2	1	0
Error	Na							
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							

LBA High	Na							
Device	obs	Na	obs	DEV	Na	Na	Na	Na
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Device register-

**DEV** shall specify the selected device.

Status register

**BSY** will be cleared to zero indicating command completion

**DRDY** will be set to one.

**DF** (Device Fault) will be cleared to zero.

**DRQ** will be cleared to zero

**ERR** will be cleared to zero.

#### 5.1.10.5 Error Outputs

**Table 36: Set multiple mode command for error outputs information**

Register	7	6	5	4	3	2	1	0
Error	Na	Na	obs	Na	Na	ABRT	Na	Na
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	Obs	Na	obs	DEV	Na			
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Status register

**BSY** will be cleared to zero indicating command completion

**DRDY** will be set to one.

**DF** (Device Fault) will be cleared to one if a device fault has occurred.

**DRQ** will be cleared to zero

**ERR** will be set to one if an Error register bit is set to one.

#### 5.1.10.6 Prerequisites

**DRDY** set to one.

#### 5.1.10.7 Description

This command establishes the block count for READ MULTIPLE, READ MULTI EXT, WRITE MULTIPLE.

SSD can only support 1 sector per block.

### 5.1.11 Set Sleep Mode

#### 5.1.11.1 Command Code

E6h

## 5.1.11.2 Protocol

Non-data

## 5.1.11.3 Inputs

Table 37: Set sleep mode for inputs information

Register	7	6	5	4	3	2	1	0
Features	Na							
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	obs	Na	obs	DEV	Na			
Command	E6h							

Device register–

**DEV** shall specify the selected device.

## 5.1.11.4 Normal Output

Table 38: Set sleep mode for normal output information

Register	7	6	5	4	3	2	1	0
Error	Na							
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	obs	Na	obs	DEV	Na	Na	Na	Na
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Device register–

**DEV** shall specify the selected device.

Status register

**BSY** will be cleared to zero indicating command completion**DRDY** will be set to one.**DF** (Device Fault) will be cleared to zero.**DRQ** will be cleared to zero**ERR** will be cleared to zero.

## 5.1.11.5 Error Outputs

Table 39: Set sleep mode for error output information

Register	7	6	5	4	3	2	1	0
Error	Na	Na	Na	Na	Na	ABRT	Na	Na



Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	Obs	Na	obs	DEV	Na			
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Status register

**BSY** will be cleared to zero indicating command completion

**DRDY** will be set to one.

**DF** (Device Fault) will be set to one if a device fault has occurred.

**DRQ** will be cleared to zero

**ERR** will be set to one if an Error register bit is set to one.

#### 5.1.11.6 Prerequisites

**DRDY** set to one.

#### 5.1.11.7 Description

This command is the only way to cause the device to enter Sleep mode.

### 5.1.12 Flush Cache

#### 5.1.12.1 Command Code

E7h

#### 5.1.12.2 Protocol

Non-data

#### 5.1.12.3 Inputs

**Table 40: Flush cache command for inputs information**

Register	7	6	5	4	3	2	1	0
Features	Na							
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	obs	Na	obs	DEV	Na			
Command	E7h							

Device register–

**DEV** shall specify the selected device.

#### 5.1.12.4 Normal Output

**Table 41: Flush cache command for normal output information**

Register	7	6	5	4	3	2	1	0
Error	Na							

Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	obs	Na	obs	DEV	Na	Na	Na	Na
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Device register-

**DEV** shall specify the selected device.

Status register

**BSY** will be cleared to zero indicating command completion

**DRDY** will be set to one.

**DF** (Device Fault) will be cleared to zero.

**DRQ** will be cleared to zero

**ERR** will be cleared to zero.

#### 5.1.12.5 Error Outputs

**Table 42: Flush cache command for error output information**

Register	7	6	5	4	3	2	1	0
Error	Na	Na	Na	Na	Na	ABRT	Na	Na
Sector Count	Na							
LBA Low	LBA(7:0)							
LBA Mid	LBA(15:8)							
LBA High	LBA(23:16)							
Device	Obs	Na	obs	DEV	LBA(27:24)			
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Error register-

**ABRT** may be set to one if the device is not able to complete the action requested by the command.

LBA Low, LBA Mid, and LBA High, Device

Shall be written with the address of first unrecoverable error.

Status register

**BSY** will be cleared to zero indicating command completion

**DRDY** will be set to one.

**DF** (Device Fault) will be cleared to one if a device fault has occurred.

**DRQ** will be cleared to zero

**ERR** will be set to one if an Error register bit is set to one.

#### 5.1.12.6 Prerequisites

**DRDY** set to one.

#### 5.1.12.7 Description

This command is used by the host to request the device to flush the write cache. If there is data in write cache, that data shall be written to the SSD. The BSY bit shall remain set to one until all data has been successfully written or an error occurs.

### 5.1.13 Standby

#### 5.1.13.1 Command Code

E2h

#### 5.1.13.2 Protocol

Non-data

#### 5.1.13.3 Inputs

The value in the Sector Count register when the STANDBY command is issued shall determine the time period programmed into the Standby timer.

**Table 43: Standby command for inputs information**

Register	7	6	5	4	3	2	1	0
Features	Na							
Sector Count	Time period value							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	obs	Na	obs	DEV	Na			
Command	E2h							

Device register–

**DEV** shall specify the selected device.

#### 5.1.13.4 Normal Output

**Table 44: Standby command for normal output information**

Register	7	6	5	4	3	2	1	0
Error	Na							
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	obs	Na	obs	DEV	Na	Na	Na	Na
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Device register–

**DEV** shall specify the selected device.

Status register

**BSY** will be cleared to zero indicating command completion

**DRDY** will be set to one.

**DF** (Device Fault) will be cleared to zero.

**DRQ** will be cleared to zero

**ERR** will be cleared to zero.

#### 5.1.13.5 Error Outputs

**Table 45: Standby command for error output information**

Register	7	6	5	4	3	2	1	0
Error	Na	Na	Na	Na	Na	ABRT	Na	Na
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	Obs	Na	obs	DEV	Na			
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Error register-

**ABRT** may be set to one if the device is not able to complete the action requested by the command.

Status register

**BSY** will be cleared to zero indicating command completion

**DRDY** will be set to one.

**DF** (Device Fault) will be set to one if a device fault has occurred.

**DRQ** will be cleared to zero

**ERR** will be set to one if an Error register bit is set to one.

#### 5.1.13.6 Prerequisites

**DRDY** set to one.

#### 5.1.13.7 Description

This command causes the device to enter the Standby mode.

If the Sector Count register is non-zero then Standby timer shall be enabled. The value in the Sector Count register shall be used determine the time programmed into the Standby timer. If the Sector Count register is zero then the Standby timer is disabled.

### 5.1.14 Standby Immediate

#### 5.1.14.1 Command Code

E0h

#### 5.1.14.2 Protocol

Non-data

#### 5.1.14.3 Inputs

**Table 46: Standby immediate command for inputs information**

Register	7	6	5	4	3	2	1	0
Features	Na							
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	obs	Na	obs	DEV	Na			
Command	E0h							

Device register–

**DEV** shall specify the selected device.

#### 5.1.14.4 Normal Output

**Table 47: Standby immediate command for normal output information**

Register	7	6	5	4	3	2	1	0
Error	Na							
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	obs	Na	obs	DEV	Na	Na	Na	Na
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Device register–

**DEV** shall specify the selected device.

Status register

**BSY** will be cleared to zero indicating command completion

**DRDY** will be set to one.

**DF** (Device Fault) will be cleared to zero.

**DRQ** will be cleared to zero

**ERR** will be cleared to zero.

#### 5.1.14.5 Error Outputs

**Table 48: Standby immediate command for error output information**

Register	7	6	5	4	3	2	1	0
Error	Na	Na	Na	Na	Na	ABRT	Na	Na
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							

LBA High	Na							
Device	Obs	Na	obs	DEV	Na			
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Error register-

**ABRT** may be set to one if the device is not able to complete the action requested by the command.

Status register

**BSY** will be cleared to zero indicating command completion

**DRDY** will be set to one.

**DF** (Device Fault) will be set to one if a device fault has occurred.

**DRQ** will be cleared to zero

**ERR** will be set to one if an Error register bit is set to one.

#### 5.1.14.6 Prerequisites

**DRDY** set to one.

#### 5.1.14.7 Description

This command causes the device to immediately enter the Standby mode.

### 5.1.15 Write Multiple

#### 5.1.15.1 Command Code

C5h

#### 5.1.15.2 Protocol

PIO data-out

#### 5.1.15.3 Inputs

The LBA mid, LBA High, Device, and LBA Low specify the starting sector address to be written. The Sector Count register specifies the number of sectors to be transferred.

**Table 49: Write multiple command for inputs information**

Register	7	6	5	4	3	2	1	0
Features	Na							
Sector Count	Sector Count							
LBA Low	LBA(7:0)							
LBA Mid	LBA(15:8)							
LBA High	LBA(23:16)							
Device	obs	Na	obs	DEV	LBA(27:24)			
Command	C5h							

Sector Count-

Number of sectors to be transferred. A value of 00h specifies that 256 sectors shall be transferred.

LBA Low-

Starting LBA bits (7:0)

LBA Mid-

Starting LBA bits (15:8)

LBA High-

Starting LBA bits (23:16)

Device –

The LBA bit shall be set to one to specify the address is an LBA.

**DEV** shall specify the selected device.

Bits(3:0) starting LBA bits (27:24)

#### 5.1.15.4 Normal Output

**Table 50: Write multiple command for normal output information**

Register	7	6	5	4	3	2	1	0
Error	Na							
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	obs	Na	obs	DEV	Na	Na	Na	Na
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Device register-

**DEV** shall specify the selected device.

Status register

**BSY** will be cleared to zero indicating command completion

**DRDY** will be set to one.

**DF** (Device Fault) will be cleared to zero.

**DRQ** will be cleared to zero

**ERR** will be cleared to zero.

#### 5.1.15.5 Error Outputs

An unrecoverable error encountered during the execution of this command results in the termination of the command. The Command Block register contain the address of the sector where the first unrecoverable error occurred. The amount of data transferred is indeterminate.

**Table 51: Write multiple command for normal output information**

Register	7	6	5	4	3	2	1	0
Error	Na	WP	MC	IDNF	MCR	ABRT	NM	Na
Sector Count	Na							
LBA Low	LBA(7:0)							
LBA Mid	LBA(15:8)							
LBA High	LBA(23:16)							

Device	Obs	Na	obs	DEV	LBA(27:24)			
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Error register-

**IDNF** shall be set to one if a user-accessible address could not be found. IDNF shall be set to one if an address outside of the range user-accessible address is requested if command aborted is not returned.

**ABRT** shall be set to one if an error, include an ICRC error, has occurred during an Ultra DMA data transfer. ABRT shall be set to one if an address outside of the range of user-accessible address is requested if IDNF is not set to one.

LBA Low, LBA Mid, and LBA High, Device -

Shall be written with the address of first unrecoverable error.

Status register

**BSY** will be cleared to zero indicating command completion

**DRDY** will be set to one.

**DF** (Device Fault) will be set to one if a device fault has occurred.

**DRQ** will be cleared to zero

**ERR** will be set to one if an Error register bit is set to one.

#### 5.1.15.6 Prerequisites

DRDY set to one. If bit 8 of IDENTIFY DEVICE word 59 is cleared to zero, a successful SET MULTIPLE MODE command shall proceed a WRITE MULTIPLE command.

#### 5.1.15.7 Description

This command writes the number of sectors specified in the Sector Count register.

The number of sectors per block is defined by the content of word 59 of the IDENTIFY DEVICE response.

When the WRITE MULTIPLE command is issued, the SECTOR Count register contains the number of sectors (not the number of blocks) requested. The device shall interrupt for each DRQ block transferred.

IF the number of requested sectors is not evenly divisible by the block count, as many full blocks as possible are transferred, followed by a final, partial block transfer. The partial block transfer is for n sectors, where:

$N = \text{Remainder} (\text{sector count} / \text{block count})$ .

If the WRITE MULTIPLE command is received when WRITE MULTIPLE commands are disabled, the Write Multiple operation shall be rejected with command aborted.

Device errors encountered during WRITE MULTIPLE commands are posted after the attempted device write of the block or partial block transferred. The command ends with the



sector in error, even if the error was in the middle of a block. Subsequent blocks are not transferred in the event of an error.

The contents of the Command Block Registers following the transfer of a data block that had a sector in error are undefined. The host should retry the transfer as individual requests to obtain valid error information. Interrupt pending is set when the DRQ bit is set to one at the beginning of each block or partial block.

### 5.1.16 Write Sector

#### 5.1.16.1 Command Code

30h

#### 5.1.16.2 Protocol

PIO data-out

#### 5.1.16.3 Inputs

The LBA mid, LBA High, Device, and LBA Low specify the starting sector address to be written. The Sector Count register specifies the number of sectors to be transferred.

**Table 52: Write sector command for inputs information**

Register	7	6	5	4	3	2	1	0
Features	Na							
Sector Count	Sector Count							
LBA Low	LBA(7:0)							
LBA Mid	LBA(15:8)							
LBA High	LBA(23:16)							
Device	obs	LBA	obs	DEV	LBA(27:24)			
Command	30h							

Sector Count-

Number of sectors to be transferred. A value of 00h specifies that 256 sectors shall be transferred.

LBA Low-

Starting LBA bits (7:0)

LBA Mid-

Starting LBA bits (15:8)

LBA High-

Starting LBA bits (23:16)

Device –

The LBA bit shall be set to one to specify the address is an LBA.

**DEV** shall specify the selected device.

Bits(3:0) starting LBA bits (27:24)

#### 5.1.16.4 Normal Output

**Table 53: Write sector command for inputs information**

Register	7	6	5	4	3	2	1	0
Error	Na							
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	obs	Na	obs	DEV	Na	Na	Na	Na
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Device register-

**DEV** shall specify the selected device.

Status register

**BSY** will be cleared to zero indicating command completion

**DRDY** will be set to one.

**DF** (Device Fault) will be cleared to zero.

**DRQ** will be cleared to zero

**ERR** will be cleared to zero.

#### 5.1.16.5 Error Outputs

An unrecoverable error encountered during the execution of this command results in the termination of the command. The Command Block registers contain the address of the sector where the first unrecoverable error occurred. The amount of data transferred is indeterminate.

**Table 54: Write sector command for error outputs information**

Register	7	6	5	4	3	2	1	0
Error	Na	WP	MC	IDNF	MCR	ABRT	NM	Na
Sector Count	Na							
LBA Low	LBA(7:0)							
LBA Mid	LBA(15:8)							
LBA High	LBA(23:16)							
Device	Obs	Na	obs	DEV	LBA(27:24)			
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Error register-

**IDNF** shall be set to one if a user-accessible address could not be found. IDNF shall be set to one if an address outside of the range of user-accessible addresses is requested if command aborted is not returned.

**ABRT** shall be set to one if an error, including an ICRC error, has occurred during an Ultra DMA data transfer. ABRT shall be set to one if the device is not able to complete the action requested by the command. ABRT shall be set to one if an address outside of the range of user-accessible addresses is requested if IDNF is not set to one.

LBA Low, LBA Mid, and LBA High, Device

Shall be written with the address of first unrecoverable error.

## Status register

**BSY** will be cleared to zero indicating command completion

**DRDY** will be set to one.

**DF** (Device Fault) will be set to one if a device fault has occurred.

**DRQ** will be cleared to zero

**ERR** will be set to one if an Error register bit is set to one.

## 5.1.16.6 Prerequisites

**DRDY** set to one.

## 5.1.16.7 Description

This command writes from 1 to 256 sectors as specified in the Sector Count register. A sector count of 0 requests 256 sectors. The device shall interrupt for each DRQ block transferred.

## 5.1.17 Write DMA

## 5.1.17.1 Command Code

CAh

## 5.1.17.2 Protocol

DMA

## 5.1.17.3 Inputs

The LBA Mid, LBA High, Device, and LBA Low specify the starting sector address to be written. The Sector Count register specifies the number of sectors to be transferred.

**Table 55: Write DMA command for input information**

Register	7	6	5	4	3	2	1	0
Features	Na							
Sector Count	Sector Count							
LBA Low	LBA(7:0)							
LBA Mid	LBA(15:8)							
LBA High	LBA(23:16)							
Device	obs	LBA	obs	DEV	LBA(27:24)			
Command	CAh							

## Sector Count-

Number of sectors to be transferred. A value of 00h specifies that 256 sectors shall be transferred.

## LBA Low-

Starting LBA bits (7:0)

## LBA Mid-

Starting LBA bits (15:8)

## LBA High-

Starting LBA bits (23:16)

## Device –

The LBA bit shall be set to one to specify the address is an LBA.

**DEV** shall specify the selected device.

Bits (3:0) starting LBA bits (27:24)

Normal Output

**Table 56: Write DMA command for normal output information**

Register	7	6	5	4	3	2	1	0
Error	Na							
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	obs	Na	obs	DEV	Na	Na	Na	Na
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Device register-

**DEV** shall specify the selected device.

Status register

**BSY** will be cleared to zero indicating command completion

**DRDY** will be set to one.

**DF** (Device Fault) will be cleared to zero.

**DRQ** will be cleared to zero

**ERR** will be cleared to zero.

#### 5.1.17.4 Error Outputs

**Table 57: Write DMA command for error outputs information**

Register	7	6	5	4	3	2	1	0
Error	ICRC	WP	MC	IDNF	MCR	ABRT	NM	Obs
Sector Count	Na							
LBA Low	LBA(7:0)							
LBA Mid	LBA(15:8)							
LBA High	LBA(23:16)							
Device	Obs	Na	obs	DEV	LBA(27:24)			
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Error register-

**ICRC** shall be set to one if an interface CRC error has occurred during an Ultra DMA data transfer. The content of this bit is not applicable for Multiword DMA transfers.

**IDNF** shall be set to one if a user-accessible address could not be found. INDF shall be set to one if an address outside of the range of user-accessible address is requested if command aborted is not returned.

**ABRT** shall be set to one if an error, including an ICRC error, has occurred during an Ultra DMA data transfer. ABRT shall be set to one if the device is not able to complete the action requested by the command. ABRT shall be set to one if an address outside of the range of user-accessible addresses is requested if IDNF is not set to one.

LBA Low, LBA Mid, and LBA High, Device

Shall be written with the address of first unrecoverable error.

Status register

**BSY** will be cleared to zero indicating command completion

**DRDY** will be set to one.

**DF** (Device Fault) will be set to one if a device fault has occurred.

**DRQ** will be cleared to zero

**ERR** will be set to one if an Error register bit is set to one.

#### 5.1.17.5 Prerequisites

DRDY set to one. The host shall initialize the DMA channel.

#### 5.1.17.6 Description

The Write DMA command allows the host to write data using the DMA data transfer protocol.

### 5.1.18 Execute Device Diagnostic

#### 5.1.18.1 Command Code

90h

#### 5.1.18.2 Feature Set

General feature set

#### 5.1.18.3 Protocol

Device diagnostic

#### 5.1.18.4 Inputs

Only the command code (90h). All other registers shall be ignored.

**Table 58: Execute device diagnostic command for inputs information**

Register	7	6	5	4	3	2	1	0
Features	Na							
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	obs	Na	obs	Na	Na			
Command	90h							

Device –

DEV shall be ignored.

## Normal Outputs

The diagnostic code written into the Error register is an 8-bit code.

**Table 59: Execute device diagnostic command for normal outputs information**

Register	7	6	5	4	3	2	1	0
Error	Diagnostic Code							
Sector Count	Signature							
LBA Low	Signature							
LBA Mid	Signature							
LBA High	Signature							
Device	Signature							
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Error register-

Diagnostic Code

Sector Count, LBA Low, LBA Mid, LBA High, Device registers

Device signature

Device register

DEV shall be cleared to zero.

Status register

TBD

**Table 60: Execute device diagnostic command for status register information**

Code	Description
01h	Device passed
Others	Device failed

### 5.1.18.5 Error Outputs

Table 9 shows the error information that is returned as a diagnostic code in the Error register.

### 5.1.18.6 Prerequisites

This command shall be accepted regardless of the state of DRDY.

### 5.1.18.7 Description

This command shall cause the devices to perform the internal diagnostic tests.

## 5.1.19 Security Set Password

### 5.1.19.1 Command Code

F1h

### 5.1.19.2 Feature Set

Security Mode feature set

## 5.1.19.3 Protocol

PIO data-out

## 5.1.19.4 Inputs

Table 61: Security set password command for inputs information

Register	7	6	5	4	3	2	1	0
Features	Na							
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	obs	Na	obs	Na	Na			
Command	F1h							

Device –

DEV shall specify the selected device.

Normal Outputs

Table 62: Security set password command for normal outputs information

Register	7	6	5	4	3	2	1	0
Error	Na							
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	obs	Na	obs	DEV	Na			
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Device register

DEV shall indicate the selected device.

Status register

**BSY** will be cleared to zero indicating command completion**DRDY** will be set to one.**DF** (Device Fault) will be set to zero.**DRQ** will be cleared to zero**ERR** will be set to zero.

## 5.1.19.5 Error Outputs

Table 63: Security set password command for error outputs information

Register	7	6	5	4	3	2	1	0
Error	Na	Na	Na	Na	Na	ABRT	Na	Na
Sector Count	Na							

LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	obs	Na	obs	DEV	Na			
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

#### Error Register

ABRT may be set to one if the device is not able to complete the action requested by the command

#### Device register

DEV shall indicate the selected device.

#### Status register

**BSY** will be cleared to zero indicating command completion

**DRDY** will be set to one.

**DF** (Device Fault) should be set to one if a device fault has occurred.

**DRQ** will be cleared to zero

**ERR** will be set to one if an Error register bit is set to one.

#### 5.1.19.6 Prerequisites

DRDY set to one.

#### 5.1.19.7 Description

This command transfer 512 byte of data from the host. Table 10 defines the content of this information. The data transferred controls the function of this command. Table 11 defines the interaction of the identifier and security level bits.

The revision code field shall be returned in the IDENTIFY DEVICE word 92. The valid revision codes are 0001h through FFFEh. A value of 0000h or FFFFh indicates that the Master Password Revision Code is not supported.

**Table 64: Security set password command's data content**

Word	Content
0	Control Word Bit 0      Identifier      0=set User password 1=set Master password Bits (7:1)   Reserved Bit(8)      Security level   0=High 1=Maximum Bits(15:9)   Reserved
1-16	Password(32 bytes)
17	Master Password Revision Code()
18-255	Reserved



**Table 65: Security Set password command's identifier and security level bit interaction**

Identifier	Level	Command result
User	High	The password supplied with the command shall be saved as the new User password. The Lock mode shall be enabled from the next power-on or hardware reset. The device shall then be unlocked by either the User password or the previously set Master password.
User	Maximum	The password supplied with the command shall be saved as the new User password. The lock mode shall be enabled from the next power-on or hardware reset. The device shall then be unlocked by only the User password. The Master password previously set is still stored in the device but shall not be unlock
Master	High or Maximum	This combination shall set a Master password but shall not enable or disable the Lock mode. The security level is not changed. Master password revision code set to the value in Master Password Revision Code field.

## 5.1.20 Security Unlock

### 5.1.20.1 Command Code

F2h

### 5.1.20.2 Feature Set

Security Mode feature set

### 5.1.20.3 Protocol

PIO data-out

### 5.1.20.4 Inputs

**Table 66: Security unlock command for inputs information**

Register	7	6	5	4	3	2	1	0
Features	Na							
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	obs	Na	obs	Na	Na			
Command	F2h							

Device register–

DEV shall specify the selected device.

Normal Outputs

**Table 67: Security unlock command for inputs information**

Register	7	6	5	4	3	2	1	0
Error	Na							
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	obs	Na	obs	DEV	Na			
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Device register

DEV shall indicate the selected device.

Status register

**BSY** will be cleared to zero indicating command completion

**DRDY** will be set to one.

**DF** (Device Fault) will be set to zero.

**DRQ** will be cleared to zero

**ERR** will be set to zero.

#### 5.1.20.5 Error Outputs

The device shall return aborted if the device is in Frozen mode.

**Table 68: Security unlock command for inputs information**

Register	7	6	5	4	3	2	1	0
Error	Na	Na	Na	Na	Na	ABRT	Na	Na
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	obs	Na	obs	DEV	Na			
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Error Register

ABRT may be set to one if the device is not able to complete the action requested by the command

Device register

DEV shall indicate the selected device.

Status register

**BSY** will be cleared to zero indicating command completion

**DRDY** will be set to one.

**DF** (Device Fault) should be set to one if a device fault has occurred.

**DRQ** will be cleared to zero

**ERR** will be set to one if an Error register bit is set to one.

#### 5.1.20.6 Prerequisites

DRDY set to one.

#### 5.1.20.7 Description

This command transfers 512 bytes of data from the host. Table13 defines the content of this information. If the Identifier bit is set to Master and the device is in high security level, then the password supplied shall be compared with the stored Master password. If the device is in maximum security level then the unlock shall be rejected.

If the Identifier bit is set to user then the device shall compare the supplied password with the stored User password. If the password compare fails then the device shall return command aborted to the host and decrements the unlock counter. This counter shall be initially set to five and shall decremented for each password mismatch when SECURITY UNLOCK and SECURITY ERASE UNIT commands shall be command aborted until a power-on reset or a hardware reset. SECURITY UNLOCK commands issued when the device is unlocked have no effect on the unlock counter.

### 5.1.21 Security Erase Prepare

#### 5.1.21.1 Command Code

F3h

#### 5.1.21.2 Feature Set

Security Mode feature set

#### 5.1.21.3 Protocol

Non-data

#### 5.1.21.4 Inputs

**Table 69: Security erase prepare command for inputs information**

Register	7	6	5	4	3	2	1	0
Features	Na							
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	obs	Na	obs	Na	Na			
Command	F3h							

Device register–

DEV shall specify the selected device.

Normal Outputs

**Table 70: Security erase prepare command for normal outputs information**

Register	7	6	5	4	3	2	1	0
Error	Na							
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	obs	Na	obs	DEV	Na	Na	Na	Na
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Device register

DEV shall indicate the selected device.

Status register

**BSY** will be cleared to zero indicating command completion

**DRDY** will be set to one.

**DF** (Device Fault) will be set to zero.

**DRQ** will be cleared to zero

**ERR** will be set to zero.

#### 5.1.21.5 Error Outputs

The device shall return aborted if the device is in Frozen mode.

**Table 71: Security erase prepare command for error outputs information**

Register	7	6	5	4	3	2	1	0
Error	Na	Na	Na	Na	Na	ABRT	Na	Na
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	obs	Na	obs	DEV	Na			
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Error Register

ABRT shall be set to one if the device is in Frozen mode. ABRT may be set to one if the device is not able to complete the action requested by the command

Device register

DEV shall indicate the selected device.

Status register

**BSY** will be cleared to zero indicating command completion

**DRDY** will be set to one.

**DF** (Device Fault) should be set to one if a device fault has occurred.

**DRQ** will be cleared to zero

**ERR** will be set to one if an Error register bit is set to one.

#### 5.1.21.6 Prerequisites

DRDY set to one.

#### 5.1.21.7 Description

The SECURITY ERASE PREPARE command shall be issued immediately before the SECURITY ERASE UNIT command to enable device erasing and unlocking. This command prevents accidental loss of data on the device.

### 5.1.22 Security Erase Unit

#### 5.1.22.1 Command Code

F4h

#### 5.1.22.2 Feature Set

Security Mode feature set

#### 5.1.22.3 Protocol

PIO data-out.

#### 5.1.22.4 Inputs

**Table 72: Security erase unit command for inputs information**

Register	7	6	5	4	3	2	1	0
Features	Na							
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	obs	Na	obs	Na	Na	Na	Na	Na
Command	F4h							

Device register–

DEV shall specify the selected device.

Normal Outputs

**Table 73: Security erase unit command for normal outputs information**

Register	7	6	5	4	3	2	1	0
Error	Na							
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	obs	Na	obs	DEV	Na	Na	Na	Na
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Device register

DEV shall indicate the selected device.

## Status register

**BSY** shall be cleared to zero indicating command completion

**DRDY** shall be set to one.

**DF** (Device Fault) will be set to zero.

**DRQ** shall be cleared to zero

**ERR** shall be cleared to zero.

## 5.1.22.5 Error Outputs

The device shall return aborted if the device is in Frozen mode, not preceded by a SECURITY ERASE PREPARE command, if Enhance Erase is specified but not supported, or if the data area is not successfully overwritten.

**Table 74: Security erase unit command for error outputs information**

Register	7	6	5	4	3	2	1	0
Error	Na	Na	Na	Na	Na	ABRT	Na	Na
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	obs	Na	obs	DEV	Na			
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

## Error Register

ABRT shall be set to one if the device is in Frozen mode, not preceded by a SECURITY ERASE PREPARE command, or if the data area is not successfully overwritten. ABRT may be set to one if the device is not able to complete the action requested by the command.

## Device register

DEV shall indicate the selected device.

## Status register

**BSY** will be cleared to zero indicating command completion

**DRDY** will be set to one.

**DF** (Device Fault) should be set to one if a device fault has occurred.

**DRQ** will be cleared to zero

**ERR** will be set to one if an Error register bit is set to one.

## 5.1.22.6 Prerequisites

DRDY set to one. This command shall be immediately preceded by a SECURITY ERASE PREPARE command.

## 5.1.22.7 Description

This command transfer 512 bytes of data from the host. Table12 defines the content of this information. If the password does not match the password previously saved by the device, the device shall reject the command with command aborted.

The SECURITY ERASE PREPARE command shall be completed immediately prior to the SECURITY ERASE UNIT command. If the device receives a SECURITY ERASE UNIT command without an immediately prior SECURITY ERASE PREPARE command, the device shall command abort the SECURITY ERASE UNIT command.

When Normal Erase mode is specified, the SECURITY ERASE UNIT command shall write binary zeroes to all user data areas. The Enhanced Erase mode is optional. When Enhanced Erase Mode is specified, the device shall write predetermined data patterns to all user areas. In Enhanced Erase mode, all previously written user data shall be overwritten, including sectors that are no longer in use due to reallocation.

This command shall disable the device Lock mode, however, the Master password shall still be stored internally within the device and may be reactivated later a new User password is set.

**Table 75: Security erase unit password information**

Word	Content
0	Control Word Bit 0      Identifier      0=Compare User password 1= Compare Master password Bit 1      Erase mode      0=Normal Erase 1=Enhanced Erase Bit(15:2)   Reserved
1-16	Password (32 Bytes)
17-255	Reserved

### 5.1.23 Security Freeze Lock

#### 5.1.23.1 Command Code

F5h

#### 5.1.23.2 Feature Set

Security Mode feature set

#### 5.1.23.3 Protocol

Non-data.

#### 5.1.23.4 Inputs

**Table 76: Security freeze lock for inputs information**

Register	7	6	5	4	3	2	1	0
Features	Na							
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							

LBA High	Na							
Device	Obs	Na	obs	Na	Na	Na	Na	Na
Command	F5h							

Device register–

DEV shall specify the selected device.

#### Normal Outputs

**Table 77: Security freeze lock for normal outputs information**

Register	7	6	5	4	3	2	1	0
Error	Na							
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	Obs	Na	obs	DEV	Na	Na	Na	Na
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Device register

DEV shall indicate the selected device.

Status register

**BSY** shall be cleared to zero indicating command completion

**DRDY** shall be set to one.

**DF** (Device Fault) will be set to zero.

**DRQ** shall be cleared to zero

**ERR** shall be cleared to zero.

#### 5.1.23.5 Error Outputs

The device shall return aborted if the device is in Frozen mode, not preceded by a SECURITY ERASE PREPARE command, if Enhance Erase is specified but not supported, or if the data area is not successfully overwritten.

**Table 78: Security freeze lock for error outputs information**

Register	7	6	5	4	3	2	1	0
Error	Na	Na	Na	Na	Na	ABRT	Na	Na
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	Obs	Na	obs	DEV	Na			
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Error Register



ABRT shall be set to one if the device is in locked mode. ABRT may be set to one if the device is not able to complete the action requested by the command.

Device register

DEV shall indicate the selected device.

Status register

**BSY** will be cleared to zero indicating command completion

**DRDY** will be set to one.

**DF** (Device Fault) should be set to one if a device fault has occurred.

**DRQ** will be cleared to zero

**ERR** will be set to one if an Error register bit is set to one.

#### 5.1.23.6 Prerequisites

DRDY set to one.

#### 5.1.23.7 Description

The SECURITY FREEZE LOCK command shall set the device to Frozen mode. After command completion any other commands that update the device Lock mode shall be command aborted. Frozen mode shall be disabled by power-off or hardware reset. If SECURITY FREEZE LOCK shall be issued when the device in Frozen mode, the command executes and the device shall remain in Frozen mode.

Command disabled by SECURITY FREEZE LOCK are:

- SECUIRTY SET PASSWORD
- SECURITY UNLOCK
- SECURITY DISABLE PASSWORD
- SECURITY ERASE PREPARE
- SECURITY ERASE UNIT

### 5.1.24 Security Disable Password

#### 5.1.24.1 Command Code

F6h

#### 5.1.24.2 Feature Set

Security Mode feature set

#### 5.1.24.3 Protocol

PIO data-out.

#### 5.1.24.4 Inputs

**Table 79: Security disable password command for inputs information**

Register	7	6	5	4	3	2	1	0
Features	Na							
Sector Count	Na							
LBA Low	Na							

LBA Mid	Na							
LBA High	Na							
Device	obs	Na	obs	Na	Na	Na	Na	Na
Command	F6h							

Device register–

DEV shall specify the selected device.

Normal Outputs

**Table 80: Security disable password command for normal outputs information**

Register	7	6	5	4	3	2	1	0
Error	Na							
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	obs	Na	obs	DEV	Na	Na	Na	Na
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Device register

DEV shall indicate the selected device.

Status register

**BSY** shall be cleared to zero indicating command completion

**DRDY** shall be set to one.

**DF** (Device Fault) will be set to zero.

**DRQ** shall be cleared to zero

**ERR** shall be cleared to zero.

#### 5.1.24.5 Error Outputs

The device shall return aborted if the device is in Locked mode, or device is in Frozen mode.

**Table 81: Security disable password command for error outputs information**

Register	7	6	5	4	3	2	1	0
Error	Na	Na	Na	Na	Na	ABRT	Na	Na
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	obs	Na	obs	DEV	Na			
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Error Register

ABRT may be set to one if the device is not able to complete the action requested by the command.

## Device register

DEV shall indicate the selected device.

## Status register

**BSY** will be cleared to zero indicating command completion

**DRDY** will be set to one.

**DF** (Device Fault) should be set to one if a device fault has occurred.

**DRQ** will be cleared to zero

**ERR** will be set to one if an Error register bit is set to one.

## 5.1.24.6 Prerequisites

DRDY set to one. Device shall be in Unlocked mode.

## 5.1.24.7 Description

The SECURITY DISABLE PASSWORD command transfer 512 bytes of data from the host. Table 13 defines the content of this information. If the password selected by word 0 matches the password previously saved by the device, the device shall disable the Lock mode. This command shall not change the Master password. The Master password shall be reactivated when a User password if set.

**Table 82: Security disable password command content**

Word	Content
0	Control Word Bit 0      Identifier      0=Compare User password 1= Compare Master password Bit(15:1)   Reserved
1-16	Password (32 Bytes)
17-255	Reserved

## 5.1.25 Read Buffer

## 5.1.25.1 Command Code

E4h

## 5.1.25.2 Protocol

PIO data-in

## 5.1.25.3 Inputs

**Table 83: Read Buffer command for inputs information**

Register	7	6	5	4	3	2	1	0
Features	Na							
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							

LBA High	Na				
Device	obs	Na	obs	DEV	Na
Command	E4h				

Device –

**DEV** shall specify the selected device.

#### 5.1.25.4 Normal Output

**Table 84: Read Buffer command for normal output information**

Register	7	6	5	4	3	2	1	0
Error	Na							
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	obs	Na	obs	DEV	Na	Na	Na	Na
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Device register-

**DEV** shall specify the selected device.

Status register

**BSY** will be cleared to zero indicating command completion

**DRDY** will be set to one.

**DF** (Device Fault) will be cleared to zero.

**DRQ** will be cleared to zero

**ERR** will be cleared to zero.

#### 5.1.25.5 Error Outputs

The device shall return command aborted if the command is not supported.

**Table 85: Read Buffer command for error output information**

Register	7	6	5	4	3	2	1	0
Error	Na	Na	Na	Na	Na	ABRT	Na	Na
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	Obs	Na	obs	DEV	Na			
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Error register-

ABRT shall be set to one if this command is not supported. ABRT may be set to one if the device is not able to complete the action requested by the command.

Device register -

DEV shall indicate the selected device.

Status register

**BSY** will be cleared to zero indicating command completion

**DRDY** will be set to one.

**DF** (Device Fault) will be cleared to zero.

**DRQ** will be cleared to zero

**ERR** will be set to one if an Error register bit is set to one.

#### 5.1.25.6 Prerequisites

**DRDY** set to one. The command prior to a READ BUFFER command shall be a WRITE BUFFER command.

#### 5.1.25.7 Description

The READ BUFFER command enables the host to read the current contents of the device's sector buffer.

The READ BUFFER and WRITE BUFFER commands shall be synchronized such that sequential WRITE BUFFER and READ BUFFER commands access the same 512 bytes within the buffer.

### 5.1.26 Write Buffer

#### 5.1.26.1 Command Code

E8h

#### 5.1.26.2

General feature set

- Optional for devices not implementing the PACKET Command feature set.
- Use prohibited for devices implementing the PACKET Command feature set.

#### 5.1.26.3 Protocol

PIO data-out

#### 5.1.26.4 Inputs

**Table 86: Write Buffer command for inputs information**

Register	7	6	5	4	3	2	1	0
Features	Na							
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	obs	Na	obs	DEV	Na			
Command	E8h							

Device register –

**DEV** shall specify the selected device.

#### 5.1.26.5 Normal Output

**Table 87: Write Buffer command for normal output information**

Register	7	6	5	4	3	2	1	0
Error	Na							
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	obs	Na	obs	DEV	Na	Na	Na	Na
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Device register-

**DEV** shall specify the selected device.

Status register

**BSY** will be cleared to zero indicating command completion

**DRDY** will be set to one.

**DF** (Device Fault) will be cleared to zero.

**DRQ** will be cleared to zero

**ERR** will be cleared to zero.

#### 5.1.26.6 Error Outputs

The device shall return command aborted if the command is not supported.

**Table 88: Write Buffer command for error output information**

Register	7	6	5	4	3	2	1	0
Error	Na	Na	Na	Na	Na	ABRT	Na	Na
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	Obs	Na	obs	DEV	Na			
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Error register-

ABRT shall be set to one if this command is not supported. ABRT may be set to one if the device is not able to complete the action requested by the command.

Device register -

DEV shall indicate the selected device.

Status register

**BSY** will be cleared to zero indicating command completion

**DRDY** will be set to one.

**DF** (Device Fault) will be cleared to zero.

**DRQ** will be cleared to zero

**ERR** will be set to one if an Error register bit is set to one.

---

#### 5.1.26.7 Prerequisites

**DRDY** set to one.

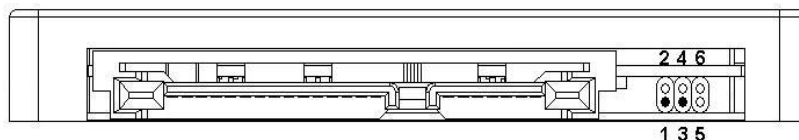
#### 5.1.26.8 Description

This command enables the host to write the contents of one sector in the device's buffer.

The READ BUFFER and WRITE BUFFER commands shall be synchronized within the device such that sequential WRITE BUFFER and READ BUFFER commands access the same 512 bytes within the buffer.

## 5. InnoRobust II 2.5" SATA SSD Security Function

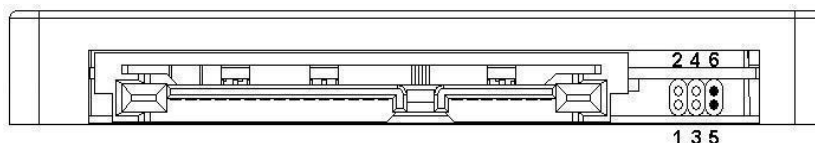
### Default



InnoRobust II 2.5" SATA SSD has several security functions, including QEraser, SEraser and Write Protect, which can be triggered by shorting different pin configuration or by ATA command. Please ensure jumper insert on default setting (pin1 and pin3), when security function is not required.

### 6.1 QEraser (Quick Erase)/Destroy Function

QEraser function is designed for emergency data erase in few seconds. QEraser can be triggered by shorting QEraser Pins (pin5 and pin6) with an external jumper or by sending ATA Command. All data Block of flash chip will be erased after executing QEraser .



**Attention:** Once QEraser/Destroy is triggered, jumper must remove from QEraser pins (pin 5 and pin 6) immediately, otherwise erase command would be execute continually.

Innodisk Destroy function implements an ultimate data erase of the SSD. Once Destroy is triggered, beside all the user data and SSD information, also SSD firmware will be erased and which is UNRECOVERABLE. InnoRobust II SATA SSD pin 5, 6 are set for QEraser. Destroy is optional and available for customization.

Innodisk provides the following Quick Erase for options\*:

- Destroy
- Quick Erase

\*See details in Table 91

#### 6.1.1 QEraser Command

##### 6.1.1.1 Command Code

82h

##### 6.1.1.2 Feature Set

General feature set



### 6.1.1.3 Protocol

Non Data Command

### 6.1.1.4 Inputs

**Table 89: Execute Quick Erase command for inputs information**

Register	7	6	5	4	3	2	1	0
Features	21h							
Sector Count	41h							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	1	1	1	0	Na			
Command	82h							

### 6.1.1.5 Normal Outputs

**Table 90: Quick Erase command for normal output information**

Register	7	6	5	4	3	2	1	0
Error	Na							
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	obs	Na	obs	DEV	Na	Na	Na	Na
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Device register-

**DEV** shall specify the selected device.

Status register

**BSY** will be cleared to zero indicating command completion

**DRDY** will be set to one.

**DF** (Device Fault) will be cleared to zero.

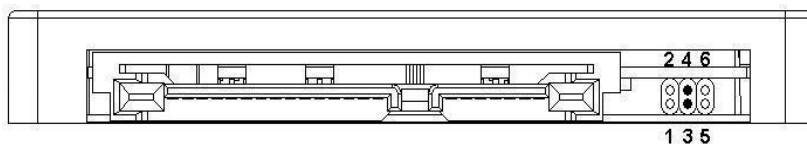
**DRQ** will be cleared to zero

**ERR** will be cleared to zero.

## 6.2 SEraser (Security Erase) Function

Security Erase function is designed for emergency data erase to comply with military standard. Erase functions can be triggered by shorting Security Erase Pins (SE) or by sending ATA Command. All Data Block of flash chip will be erased by sending flash erase command. SE Pin can be set as one military Security Erase standards.

SEraser



Attention: Once SEraser is triggered, jumper must remove from SEraser pins (pin 3 and pin 4)

immediately, otherwise erase command would be execute continually.

Innodisk provides the following Security Erase for options:

- AFFSI 5020
- DoD 5220.22-M
- USA Navy NAVSO P-5239-26
- NSA Manual 130-2
- USA-Army 380-19
- NISPOMSUP Chap 8, Sect. 8-501
- NSA Manual 9-12
- IRIG 106

Word 159 of Identify Table shows the SE pin's function. Identify Table can be read by sending ECh ATA command.

Table 91: Identify Information

154	Secure Function Support		
	7-15	Reserved	0
	6	1= Secure Erase ATA Vendor Command Supported	X
	5	Reserved	0
	4	1=Quick Erase ATA Vendor Command Supported	X
	3	1=Destroy ATA Vendor Command Supported	X
		1=Jumper Secure Erase Supported	X
	1	1=Jumper Write Protect Supported	X
	0	1=Jumper Quick Erase Supported	X
155	Secure Function Status(Enable/Disable)		
	2-15	Reserved	
	1	Write Protect Enabled	X
	0	Reserved	0
156-158	Vendor Specific		
159	8~15 Function of Jumper "QE" 0x20: Destroy 0x21 or Others: Quick Erase		XXXXh

0~7	
Secure Erase Function of Jumper "SE"	
0x22: AFFSI 5020	
0x23: DoD 5220.22-M	
0x24: USA Navy NAVSO P-5239-26	
0x25: NSA Manual 130-2	
0x26: USA-Army 380-19	
0x27: NISPOMSUP Chap 8, Sect. 8-501	
0x28: NSA Manual 9-12	
0x29: IRIG106	
0x19: Get System Bad Block Data	

## 6.2.1 AFFSI 5020

This function is compliant with AFFSI 5020 specification.

Steps:

- 1 The whole disk is erased using Flash Erase Command.
- 2 The whole disk is filled with random data.

### 6.2.1.1 Command Code

82h

### 6.2.1.2 Feature Set

General feature set

### 6.2.1.3 Protocol

Non Data Command

### 6.2.1.4 Inputs

**Table 92: Execute AFFSI 5020 command for inputs information**

Register	7	6	5	4	3	2	1	0
Features	22h							
Sector Count	41h							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	1	1	1	0	Na			
Command	82h							

### 6.2.1.5 Normal Outputs

**Table 93: AFFSI 5020 command for normal output information**

Register	7	6	5	4	3	2	1	0
Error	Na							

Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	obs	Na	obs	DEV	Na	Na	Na	Na
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Device register-

**DEV** shall specify the selected device.

Status register

**BSY** will be cleared to zero indicating command completion

**DRDY** will be set to one.

**DF** (Device Fault) will be cleared to zero.

**DRQ** will be cleared to zero

**ERR** will be cleared to zero.

## 6.2.2 DoD 5220.22-M

This function is compliant with DoD 5220.22-M specification.

Steps:

- 1 The whole disk is filled with fixed character pattern 0x55.
- 2 The whole disk is erased using Flash Erase Command.

### 6.2.2.1 Command Code

82h

### 6.2.2.2 Feature Set

General feature set

### 6.2.2.3 Protocol

Non Data Command

### 6.2.2.4 Inputs

**Table 94: Execute DoD 5220.22-M command for inputs information**

Register	7	6	5	4	3	2	1	0
Features	23h							
Sector Count	41h							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	1	1	1	0	Na			
Command	82h							

### 6.2.2.5 Normal Outputs

**Table 95: DoD 5220.22-M command for normal output information**

Register	7	6	5	4	3	2	1	0
Error	Na							
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	obs	Na	obs	DEV	Na	Na	Na	Na
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Device register-

**DEV** shall specify the selected device.

Status register

**BSY** will be cleared to zero indicating command completion

**DRDY** will be set to one.

**DF** (Device Fault) will be cleared to zero.

**DRQ** will be cleared to zero

**ERR** will be cleared to zero.

### 6.2.3 USA Navy NAVSO P-5239-26

This function is compliant with USA Navy NAVSO P-5239-26 specification.

Steps:

- 1 The whole disk is erased using Flash Erase Command.
- 2 The whole disk is filled with random data.
- 3 The whole disk is erased using Flash Erase Command.

#### 6.2.3.1 Command Code

82h

#### 6.2.3.2 Feature Set

General feature set

#### 6.2.3.3 Protocol

Non Data Command

#### 6.2.3.4 Inputs

**Table 96: Execute USA Navy NAVSO P-5239-26 command for inputs information**

Register	7	6	5	4	3	2	1	0
Features	24h							
Sector Count	41h							
LBA Low	Na							
LBA Mid	Na							

LBA High	Na				
Device	1	1	1	0	Na
Command	82h				

#### 6.2.3.5 Normal Outputs

**Table 97: USA Navy NAVSO P-5239-26 command for normal output information**

Register	7	6	5	4	3	2	1	0
Error	Na							
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	obs	Na	obs	DEV	Na	Na	Na	Na
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Device register-

**DEV** shall specify the selected device.

Status register

**BSY** will be cleared to zero indicating command completion

**DRDY** will be set to one.

**DF** (Device Fault) will be cleared to zero.

**DRQ** will be cleared to zero

**ERR** will be cleared to zero.

### 6.2.4 NSA Manual 130-2

This function is compliant with NSA Manual 130-2 specification.

Steps:

- 1 The whole disk is erased using Flash Erase Command.
- 2 The whole disk is filled with random data.
- 3 The whole disk is filled with random data again.
- 4 The whole disk is erased using Flash Erase Command.
- 5 The whole disk is filled with fixed character pattern 0x55.

#### 6.2.4.1 Command Code

82h

#### 6.2.4.2 Feature Set

General feature set

#### 6.2.4.3 Protocol

Non Data Command

#### 6.2.4.4 Inputs

**Table 98: Execute NSA Manual 130-2 command for inputs information**

Register	7	6	5	4	3	2	1	0
Features	25h							
Sector Count	41h							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	1	1	1	0	Na			
Command	82h							

#### 6.2.4.5 Normal Outputs

**Table 99: NSA Manual 130-2 command for normal output information**

Register	7	6	5	4	3	2	1	0
Error	Na							
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	obs	Na	Obs	DEV	Na	Na	Na	Na
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Device register-

**DEV** shall specify the selected device.

Status register

**BSY** will be cleared to zero indicating command completion

**DRDY** will be set to one.

**DF** (Device Fault) will be cleared to zero.

**DRQ** will be cleared to zero

**ERR** will be cleared to zero

### 6.2.5 USA-Army 380-19

This function is compliant with USA-Army 380-19 specification.

Step:

- 1 The whole disk is erased using Flash Erase Command.
- 2 The whole disk is filled with random data.
- 3 The whole disk is filled with fixed character pattern 0x55.
- 4 The whole disk is filled with fixed character pattern 0xAA.

#### 6.2.5.1 Command Code

82h

#### 6.2.5.2 Feature Set

General feature set

## 6.2.5.3 Protocol

Non Data Command

## 6.2.5.4 Inputs

**Table 100: Execute USA Army 380-19 command for inputs information**

Register	7	6	5	4	3	2	1	0
Features	26h							
Sector Count	41h							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	1	1	1	0	Na			
Command	82h							

## 6.2.5.5 Normal Outputs

**Table 101: USA Navy NAVSO P-5239-26 command for normal output information**

Register	7	6	5	4	3	2	1	0
Error	Na							
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	obs	Na	Obs	DEV	Na	Na	Na	Na
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Device register-

**DEV** shall specify the selected device.

Status register

**BSY** will be cleared to zero indicating command completion**DRDY** will be set to one.**DF** (Device Fault) will be cleared to zero.**DRQ** will be cleared to zero.**ERR** will be cleared to zero.

## 6.2.6 NISPOMSUP Chap 8, Sect. 8-501

This function is compliant with NISPOMSUP Chap 8, Sect. 8-501 specification.

Steps:

- 1 The whole disk is filled with fixed character pattern 0x55.
- 2 The whole disk is filled with fixed character pattern 0xAA.
- 3 The whole disk is filled with random data.



### 6.2.6.1 Command Code

82h

### 6.2.6.2 Feature Set

General feature set

### 6.2.6.3 Protocol

Non Data Command

### 6.2.6.4 Inputs

**Table 102: Execute NISPOMSUP Chap 8, Sect. 8-501 command for inputs information**

Register	7	6	5	4	3	2	1	0
Features	27h							
Sector Count	41h							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	1	1	1	0	Na			
Command	82h							

### 6.2.6.5 Normal Outputs

**Table 103: NISPOMSUP Chap 8, Sect. 8-501 command for normal output information**

Register	7	6	5	4	3	2	1	0
Error	Na							
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	obs	Na	obs	DEV	Na	Na	Na	Na
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Device register-

**DEV** shall specify the selected device.

Status register

**BSY** will be cleared to zero indicating command completion

**DRDY** will be set to one.

**DF** (Device Fault) will be cleared to zero.

**DRQ** will be cleared to zero.

**ERR** will be cleared to zero.

## 6.2.7 NSA Manual 9-12

This function is compliant with NSA Manual 9-12 specification.

Step:

1. The whole disk is erased using Flash Erase Command.
2. The whole disk is filled with unclassified pattern.
3. Verify the overwrite procedure by randomly rereading the overwritten information.

#### 6.2.7.1 Command Code

82h

#### 6.2.7.2 Feature Set

General feature set

#### 6.2.7.3 Protocol

Non Data Command

#### 6.2.7.4 Inputs

**Table 104: Execute NSA Manual 9-12 command for inputs information**

Register	7	6	5	4	3	2	1	0
Features	28h							
Sector Count	41h							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	1	1	1	0	Na			
Command	82h							

#### 6.2.7.5 Normal Outputs

**Table 105: NSA Manual 9-12 command for normal output information**

Register	7	6	5	4	3	2	1	0
Error	Na							
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	obs	Na	obs	DEV	Na	Na	Na	Na
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Device register-

**DEV** shall specify the selected device.

Status register

**BSY** will be cleared to zero indicating command completion

**DRDY** will be set to one.

**DF** (Device Fault) will be cleared to zero.

**DRQ** will be cleared to zero

**ERR** will be cleared to zero

## 6.2.8 IRIG106

This function is compliant with IRIG106 specification.

Step:

1. The whole disk is erased using Flash Erase Command.
2. The whole disk is filled with pattern 0x55, and read back to verify.
3. The whole disk is erased using Flash Erase Command.
4. The whole disk is filled with pattern 0xAA, and read back to verify.
5. The whole disk is erased using Flash Erase Command.
6. Write 0x00 to all bad blocks. If there is any bit is still 1, the page is re-written 0 again. This procedure this repeated up to 16 times.
7. Erase all bad blocks and checked to determine if any zero are found. If any zeros are found, erase this block again. This procedure this repeated up to 16 times.
8. Write "Secure Erase" string to all blocks.

### 6.2.8.1 Command Code

82h

### 6.2.8.2 Feature Set

General feature set

### 6.2.8.3 Protocol

Non Data Command

### 6.2.8.4 Inputs

**Table 106: Execute IRIG106 command for inputs information**

Register	7	6	5	4	3	2	1	0
Features	29h							
Sector Count	41h							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	1	1	1	0	Na			
Command	82h							

### 6.2.8.5 Normal Outputs

**Table 107: IRIG106 command for normal output information**

Register	7	6	5	4	3	2	1	0
Error	Na							
Sector Count	Secure Erase Failure Block Number							
LBA Low	Na							
LBA Mid	Na							

LBA High	Na							
Device	obs	Na	obs	DEV	Na	Na	Na	Na
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Device register-

**DEV** shall specify the selected device.

Status register

**BSY** will be cleared to zero indicating command completion

**DRDY** will be set to one.

**DF** (Device Fault) will be cleared to zero.

**DRQ** will be cleared to zero

**ERR** will be cleared to zero

**Sector Count:** The number of Erase Failure Block.

## 6.2.9 Get System Bad Block Data

This function is used to get SSD system bad block data .

Step:

1. This is 28-bit command for InnoRobust SSD.
2. The Get Bad Block Data command allows the host to read data using the DMA data transfer protocol.
3. Bad Block Data transfer size is fixed to 65 sectors (33280 bytes).
4. An individual Bad Block Data Entry is represented by 4 bytes.

The Ch number is expressed by the Bad Block Data Entry 's first byte and the Bank number is expressed by the Bad Block Data Entry 's Second byte. The Block number is expressed by the remaining two bytes. If the four bytes data of the Bad Block Data Entry is all FFFF\_FFFFh, then the Bad Block Data Entry shall be discarded as padding.

The following are two examples"

- 1) If the Bad Block Data Entry data is 0102\_1030h, it means Ch: 01h, Bank :02h ,Block:3010h.
- 2) If the Bad Block Data Entry data is FFFF\_FFFF, it is an invalid entry.

### 6.2.9.1 Command Code

82h

### 6.2.9.2 Feature Set

General feature set

### 6.2.9.3 Protocol

DMA data transfer protocol.

### 6.2.9.4 Inputs

**Table 108: Execute Get Bad Block Data command for inputs information**

Register	7	6	5	4	3	2	1	0
Features	19h							
Sector Count	41h							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	1	1	1	0	Na			
Command	82h							

#### 6.2.9.5 Normal Outputs

**Table 109: IRIG106 command for normal output information**

Register	7	6	5	4	3	2	1	0
Error	Na							
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	obs	Na	obs	DEV	Na	Na	Na	Na
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Device register-

**DEV** shall specify the selected device.

Status register

**BSY** will be cleared to zero indicating command completion

**DRDY** will be set to one.

**DF** (Device Fault) will be cleared to zero.

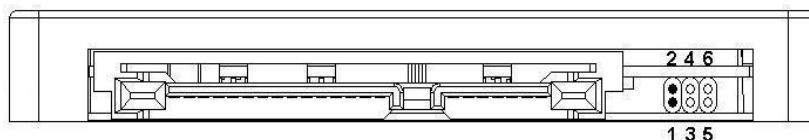
**DRQ** will be cleared to zero

**ERR** will be cleared to zero

### 6.3 Power Failure Issue

InnoRobust series is designed with a real time power detection circuit and with auto recovery mechanism. During data erasing, if power failure happens, the erase function will be discontinued. Once the power is resupplied, erase function would be automatically resumed till whole the function is completed.

### 6.4 Write Protect



When Write Protect pins (pin1 and pin2) are shorted, Write Protect function would be enabled, and ATA write command would be aborted, which can prevent the disk from data modification or data deletion. Write-protected data in disk is read-only, that is, users could not write to it, edit it, append data to it, or delete it.

InnoRobust II SATA SSD has real time detect function, it detects Write Protect pins (pin1 and pin2) every 1ms, once Write Protect pins (pin1 and pin2) are shorted, ATA write command would be aborted and Write Protect function would be enabled. On the contrary, Write Protect function would be disabled, when jumper removes from Write Protect pins (pin1 and pin2)

In addition, Write Protect function can coexist with SEraser and QEraser functions.

### 6.4.1 Enable Write Protect

This command enable SSD into write protect mode, which is read-only. The SSD under write protect will overpass any write command.

#### 6.4.1.1 Command Code

82h

#### 6.4.1.2 Feature Set

General feature set

#### 6.4.1.3 Protocol

Non Data Command

#### 6.4.1.4 Inputs

**Table 110: Execute Enable Write Protect command for inputs information**

Register	7	6	5	4	3	2	1	0
Features	17h							
Sector Count	41h							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	1	1	1	0	Na			
Command	82h							

#### 6.4.1.5 Normal Outputs

**Table 111: Enable Write Protect command for normal output information**

Register	7	6	5	4	3	2	1	0
Error	Na							
Sector Count	Na							
LBA Low	Na							

LBA Mid	Na							
LBA High	Na							
Device	obs	Na	obs	DEV	Na	Na	Na	Na
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Device register-

**DEV** shall specify the selected device.

Status register

**BSY** will be cleared to zero indicating command completion

**DRDY** will be set to one.

**DF** (Device Fault) will be cleared to zero.

**DRQ** will be cleared to zero.

**ERR** will be cleared to zero.

## 6.4.2 Disable Write Protect

This command disable SSD's write protect feature.

### 6.4.2.1 Command Code

82h

### 6.4.2.2 Feature Set

General feature set

### 6.4.2.3 Protocol

Non Data Command

### 6.4.2.4 Inputs

**Table 112: Execute Disable Write Protect command for inputs information**

Register	7	6	5	4	3	2	1	0
Features	18h							
Sector Count	41h							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	1	1	1	0	Na			
Command	82h							

### 6.4.2.5 Normal Outputs

**Table 113: Disable Write Protect command for normal output information**

Register	7	6	5	4	3	2	1	0
Error	Na							
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							

LBA High	Na							
Device	obs	Na	obs	DEV	Na	Na	Na	Na
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Device register-

**DEV** shall specify the selected device.

Status register

**BSY** will be cleared to zero indicating command completion

**DRDY** will be set to one.

**DF** (Device Fault) will be cleared to zero.

**DRQ** will be cleared to zero.

**ERR** will be cleared to zero.



## 6. Part Number Rule

CODE	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
	D	2	S	N	-	B	5	6	J	2	1	A	C	2	E	B				
Description	Disk	InnoRobust II 2.5" SATA SSD			-	Capacity			Category			FW	Operation Temp.	Internal Control	Ch.	Flash	-	Customized Code		
Definition																				
Code 1 <sup>st</sup> (Disk)									Code 13 <sup>th</sup> (Operation Temperature)											
D : Disk									C: Standard Grade (0℃ ~ +70℃)											
Code 2 <sup>nd</sup> ~ 4 <sup>th</sup> (Form Factor)									W: Industrial Grade (-40℃ ~ +85℃)											
2SN: InnoRobust II 2.5" SATA SSD									E: Extended Grade (-20℃ ~ +85℃)											
Code 6 <sup>th</sup> ~8 <sup>th</sup> (Capacity)									K: Standard Grade with coating											
08G: 8GB									T: Extended/Industrial Grade with coating*											
16G: 16GB									*Extended Grade: MLC only; Industrial Grade: SLC only											
32G: 32GB																				
64G: 64GB									Code 14 <sup>th</sup> (Internal control)											
A28: 128GB									Code 15 <sup>th</sup> (Channel of data transfer)											
B56: 256GB									E: Eight Channels											
C12:512GB																				
Code 9 <sup>th</sup> ~11 <sup>th</sup> (Series)									Code 16 <sup>th</sup> (Flash Type)											
J21: InnoRobust II 2.5" SATA SSD									B: Toshiba SLC											
Code 12 <sup>th</sup> (Firmware version)									N: Micron MLC											
A: Standard F/W version																				

## Verification of Compliance

Product Name : FiD 2.5" SATA 25000/EverGreen 2.5" SATA SSD/  
EverGreen Plus 2.5" SATA SSD/ InnoRobust II 2.5" SATA SSD

Model Number : D2SN-XXXJ20AC1#N/D2SL- XXXJ2\*\*%#&\$  
(XXX:02G,04G,08G,16G,32G,64G,A28,B56,C12 ),  
(#:S,D,Q,E (Single,Dual,Quad,Eight) (%:C,W),  
D2SN-XXXJ2\*\*%#&\$ (X=A-Z ; 0-9 or Blank, \* =FW Version%=  
C/W, K/T(Coating), # =PCB Version, & =channel, \$ =internal code)

Applicant : InnoDisk Corporation

Address : 9F., No.100, Sec. 1Xintai5<sup>th</sup> Rd., Xizhi Dist., New Taipei City  
221, Taiwan

Report Number : S2C-U070-1009-372

Issue Date : October 21, 2011

Applicable Standards : EN 55022:2006+A1:2007 Class B ITE  
EN 55024:1998+A1:2001+A2:2003  
EN 61000-4-2:1995+A1:1998+A2:2001  
EN 61000-4-3:2006+A1:2008  
EN 61000-4-4:2004

Based on the EMC Directive 2004/108/EC and the specifications of the customer, one sample of the designated product has been tested in our laboratory and found to be in compliance with the EMC standards cited above.



TAF 0905  
FCC CAB Code TW1053  
NVLAP Lab Code 200575-0  
IC Code 4699A  
VCCI Accep. No. R-1527, C-1609, T-1441, G-10



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(Tsun-Yu Shih/ General Manager)

Date: October 21, 2011

## Verification of Compliance

Product Name : FiD 2.5" SATA 25000/EverGreen 2.5" SATA SSD/  
EverGreen Plus 2.5" SATA SSD/ InnoRobust II 2.5" SATA SSD

Model Number : D2SN-XXXJ20AC1#N/D2SL- XXXJ2\*\*%#&\$  
(XXX:02G,04G,08G,16G,32G,64G,A28,B56,C12 ),  
(#:S,D,Q,E (Single,Dual,Quad,Eight) (%:C,W),  
D2SN-XXXJ2\*\*%#&\$ (X=A-Z ; 0-9 or Blank, \* =FW Version%=  
C/W, K/T(Coating), # =PCB Version, & = channel, \$ =internal code)

Applicant : InnoDisk Corporation

Address : 9F., No.100, Sec. 1Xintai5<sup>th</sup> Rd., Xizhi Dist., New Taipei City  
221, Taiwan

Report Number : S2F-U070-1009-372

Issue Date : October 21, 2011

Applicable Standards : FCC Part 15, Subpart B Class B ITE  
ANSI C63.4:2003  
Industry Canada ICES-003 Issue 4  
CSA-IEC CISPR22: 02 Class B ITE

One sample of the designated product has been tested in our laboratory and found to be in compliance with the FCC rules cited above.



NVLAP LAB CODE 200575-0

TAF 0905

FCC CAB Code TW1053

IC Code 4699A

VCCI Accep. No. R-1527, C-1609, T-1441, G-10



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Date: October 21, 2011