

InnoLite II 2.5" SATA SSD

Datasheet-Full

Rev 1.1

Table of contents

LIST OF TABLES	5
LIST OF FIGURES	7
1. PRODUCT OVERVIEW	8
1.1 INTRODUCTION OF INNO-lite II 2.5" SATA SSD	8
1.2 PRODUCT VIEW	8
1.3 PRODUCT MODELS	8
1.4 SATA INTERFACE	9
1.5 2.5-INCH FORM FACTOR	9
1.6 CAPACITY	9
2. THEORY OF OPERATION	10
2.1 OVERVIEW	10
2.2 SATA II CONTROLLER	11
2.3 ERROR DETECTION AND CORRECTION	11
2.4 WEAR-LEVELING	11
2.5 BAD BLOCKS MANAGEMENT	11
3. INSTALLATION REQUIREMENTS	12
3.1 FiD 2.5 INNO-lite II 2.5" SATA SSD PIN DIRECTIONS	12
3.2 ELECTRICAL CONNECTIONS FOR INNO-lite II 2.5" SATA SSD	12
3.3 FORM FACTOR	12
3.4 DEVICE DRIVE	13
4. SPECIFICATIONS	14
4.1 CE AND FCC COMPATIBILITY	14
4.2 ROHS COMPLIANCE	14
4.3 ENVIRONMENTAL SPECIFICATIONS	14
4.3.1 Temperature Ranges	14
4.3.2 Humidity	14
4.3.3 Shock and Vibration	14
4.3.4 Mean Time between Failures (MTBF)	14
4.4 ENDURANCE	15
4.5 TRANSFER MODE	15
4.6 PIN ASSIGNMENT	15
4.7 MECHANICAL DIMENSIONS	16
4.8 ASSEMBLY WEIGHT	16

4.9 PERFORMANCE.....	17
4.10 SEEK TIME	17
4.11 HOT PLUG	17
4.12 NAND FLASH MEMORY	17
4.13 ELECTRICAL SPECIFICATIONS.....	18
4.13.1 Power Requirement	18
4.13.2 Power Consumption	18
4.14 DEVICE PARAMETERS.....	19
5. SUPPORTED ATA COMMANDS.....	20
5.1 SUPPORTED ATA COMMANDS	20
5.1.1 Check Power Mode	21
5.1.2 IDENTIFY DEVICE	21
5.1.3 IDLE	32
5.1.4 Idle Immediate	33
5.1.5 SMART	35
5.1.6 Read Multiple	39
5.1.7 Read Sector(s).....	41
5.1.8 Read Verify Sector	43
5.1.9 Read DMA.....	45
5.1.10 Set Feature	47
5.1.11 Set Multiple Mode	47
5.1.12 Set Sleep Mode	49
5.1.13 Flush Cache.....	50
5.1.14 Standby	52
5.1.15 Standby Immediate	54
5.1.16 Write Multiple.....	55
5.1.17 Write Sector	58
5.1.18 Write DMA	60
5.1.19 Execute Device Diagnostic	63
5.1.20 Read Buffer	64
5.1.21 Write Buffer	66
6. PART NUMBER RULE.....	69

REVISION HISTORY

Revision	Description	Date
Rev 1.0	First Released	10/20/2011
Rev. 1.1	Add 512GB informtion	01/05/2012
Rev. 1.2	Modify the introduction of InnoLite II 2.5" SATA SSD	04/06/2012

List of Tables

TABLE 1: SHOCK/VIBRATION TESTING FOR INNO-lite II 2.5" SATA SSD	14
TABLE 2: INNO-lite II 2.5" SATA SSD MTBF	15
TABLE 3: INNO-lite II 2.5" SATA SSD PIN ASSIGNMENT	15
TABLE 4: INNO-lite II 2.5" SATA SSD POWER REQUIREMENT	18
TABLE 5: POWER CONSUMPTION	18
TABLE 6: DEVICE PARAMETERS	19
TABLE 7: ATA COMMANDS	20
TABLE 8: CHECK POWER MODE COMMAND FOR INPUTS INFORMATION	21
TABLE 9: IDENTIFY DEVICE COMMAND FOR INPUTS INFORMATION	22
TABLE 10: IDENTIFY DEVICE COMMAND FOR NORMAL OUTPUTS INFORMATION	22
TABLE 11: IDENTIFY DEVICE COMMAND PARAMETERS	23
TABLE 12: IDLE COMMAND FOR INPUTS INFORMATION	32
TABLE 13: IDLE COMMAND SECTOR COUNT REGISTER CONTENTS INFORMATION	32
TABLE 14: IDLE COMMAND FOR NORMAL OUTPUTS INFORMATION	32
TABLE 15: IDLE COMMAND FOR ERROR OUTPUTS INFORMATION	33
TABLE 16: IDLE IMMEDIATE COMMAND FOR INPUTS INFORMATION	34
TABLE 17: IDLE IMMEDIATE COMMAND FOR NORMAL OUTPUTS INFORMATION	34
TABLE 18: SMART FEATURE REGISTER VALUES	35
TABLE 19: SMART COMMAND FOR INPUTS INFORMATION	35
TABLE 20: SMART COMMAND FOR NORMAL OUTPUTS INFORMATION	35
TABLE 21: ID OF SMART DATA STRUCTURE	36
TABLE 22: SMART COMMAND FOR BAD BLOCK COUNT INFORMATION	36
TABLE 23: SMART COMMAND FOR AVERAGE/MAX ERASE COUNT INFORMATION	36
TABLE 24: SMART COMMAND FOR AVERAGE/ MAX ERASE COUNT INFORMATION	37
TABLE 25: SMART ENABLE COMMAND FOR INPUTS INFORMATION	37
TABLE 26: SMART COMMAND FOR NORMAL OUTPUTS INFORMATION	37
TABLE 27: SMART DISABLE COMMAND FOR INPUTS INFORMATION	38
TABLE 28: SMART COMMAND FOR NORMAL OUTPUTS INFORMATION	38
TABLE 29: READ MULTIPLE COMMAND FOR INPUTS INFORMATION	39
TABLE 30: READ MULTIPLE COMMAND FOR NORMAL OUTPUT INFORMATION	40
TABLE 31: READ MULTIPLE COMMAND FOR ERROR OUTPUT INFORMATION	40
TABLE 32: READ SECTOR COMMAND FOR INPUTS INFORMATION	41
TABLE 33: READ SECTOR COMMAND FOR NORMAL OUTPUTS INFORMATION	42
TABLE 34: READ SECTOR COMMAND FOR ERROR OUTPUTS INFORMATION	42
TABLE 35: READ VERIFY SECTOR COMMAND FOR INPUTS INFORMATION	43
TABLE 36: READ VERIFY SECTOR COMMAND FOR NORMAL OUTPUT INFORMATION	44
TABLE 37: READ VERIFY SECTOR COMMAND FOR NORMAL OUTPUT INFORMATION	45
TABLE 38: READ DMA COMMAND FOR INPUTS INFORMATION	45
TABLE 39: READ DMA COMMAND FOR NORMAL OUTPUT INFORMATION	46

TABLE 40: READ DMA COMMAND FOR ERROR OUTPUT INFORMATION	47
TABLE 41: SET MULTIPLE MODE COMMAND FOR INPUTS INFORMATION	48
TABLE 42: SET MULTIPLE MODE COMMAND FOR NORMAL OUTPUT INFORMATION	48
TABLE 43: SET MULTIPLE MODE COMMAND FOR ERROR OUTPUTS INFORMATION	48
TABLE 44: SET SLEEP MODE FOR INPUTS INFORMATION	49
TABLE 45: SET SLEEP MODE FOR NORMAL OUTPUT INFORMATION	49
TABLE 46: SET SLEEP MODE FOR ERROR OUTPUT INFORMATION	50
TABLE 47: FLUSH CACHE COMMAND FOR INPUTS INFORMATION	51
TABLE 48: FLUSH CACHE COMMAND FOR NORMAL OUTPUT INFORMATION	51
TABLE 49: FLUSH CACHE COMMAND FOR ERROR OUTPUT INFORMATION	51
TABLE 50: STANDBY COMMAND FOR INPUTS INFORMATION	52
TABLE 51: STANDBY COMMAND FOR NORMAL OUTPUT INFORMATION	53
TABLE 52: STANDBY COMMAND FOR ERROR OUTPUT INFORMATION	53
TABLE 53: STANDBY IMMEDIATE COMMAND FOR INPUTS INFORMATION	54
TABLE 54: STANDBY IMMEDIATE COMMAND FOR NORMAL OUTPUT INFORMATION	54
TABLE 55: STANDBY IMMEDIATE COMMAND FOR ERROR OUTPUT INFORMATION	55
TABLE 56: WRITE MULTIPLE COMMAND FOR INPUTS INFORMATION	56
TABLE 57: WRITE MULTIPLE COMMAND FOR NORMAL OUTPUT INFORMATION	56
TABLE 58: WRITE MULTIPLE COMMAND FOR NORMAL OUTPUT INFORMATION	57
TABLE 59: WRITE SECTOR COMMAND FOR INPUTS INFORMATION	59
TABLE 60: WRITE SECTOR COMMAND FOR INPUTS INFORMATION	59
TABLE 61: WRITE SECTOR COMMAND FOR ERROR OUTPUTS INFORMATION	60
TABLE 62: WRITE DMA COMMAND FOR INPUT INFORMATION	61
TABLE 63: WRITE DMA COMMAND FOR NORMAL OUTPUT INFORMATION	61
TABLE 64: WRITE DMA COMMAND FOR ERROR OUTPUTS INFORMATION	62
TABLE 65: EXECUTE DEVICE DIAGNOSTIC COMMAND FOR INPUTS INFORMATION	63
TABLE 66: EXECUTE DEVICE DIAGNOSTIC COMMAND FOR NORMAL OUTPUTS INFORMATION	63
TABLE 67: EXECUTE DEVICE DIAGNOSTIC COMMAND FOR STATUS REGISTER INFORMATION	64
TABLE 68: READ BUFFER COMMAND FOR INPUTS INFORMATION	64
TABLE 69: READ BUFFER COMMAND FOR NORMAL OUTPUT INFORMATION	65
TABLE 70: READ BUFFER COMMAND FOR ERROR OUTPUT INFORMATION	65
TABLE 71: WRITE BUFFER COMMAND FOR INPUTS INFORMATION	66
TABLE 72: WRITE BUFFER COMMAND FOR NORMAL OUTPUT INFORMATION	66
TABLE 73: WRITE BUFFER COMMAND FOR ERROR OUTPUT INFORMATION	67

List of Figures

FIGURE 1: INNO-lite II 2.5" SATA SSD	8
FIGURE 2: INNO-lite II 2.5" SATA SSD BLOCK DIAGRAM FROM 32GB TO 256GB	10
FIGURE 3: INNO-lite II 2.5" SATA SSD BLOCK DIAGRAM FROM 8GB TO 32GB	10
FIGURE 4: SIGNAL SEGMENT AND POWER SEGMENT	12

1. Product Overview

1.1 Introduction of InnoLite II 2.5" SATA SSD

InnoLite II 2.5" SATA SSD products provide high capacity flash memory Solid State Drive (SSD) that electrically complies with Serial ATA (SATA) standard. It supports SATA II standard (3.0GHz) with high performance. The sustain read is at 240 MB per second (max.), and sustain write is at 220 MB per second (max); Except sequential read/ write performance, InnoLite II 2.5" SATA SSD also enhances random data access for small files. It designed with standard 2.5-inch form factor, which can be used in laptop. InnoLite II 2.5" SATA SSD is designed for industrial field. The SSD have good performance, no latency time and small seek time. It effectively reduces the booting time of operation system and the power consumption is less than hard disk drive (HDD). InnoLite II 2.5" SATA SSD can work in harsh environment. The SSD is vibration resistance, and can work in lower or higher temperature than HDD. InnoLite II 2.5" SATA SSD complies with ATA protocol, no additional drives are required, and the SSD can be configured as a boot device or data storage device.

1.2 Product View



Figure 1: InnoLite II 2.5" SATA SSD

1.3 Product Models

InnoLite II 2.5" SATA SSD is available in follow capacities.

- 4 Channels

InnoLite II 2.5" SATA SSD 8GB

InnoLite II 2.5" SATA SSD 16GB

InnoLite II 2.5" SATA SSD 32GB

- 8 Channels

InnoLite II 2.5" SATA SSD 64GB

InnoLite II 2.5" SATA SSD 128GB

InnoLite II 2.5" SATA SSD 256GB

InnoLite II 2.5" SATA SSD 512GB

1.4 SATA Interface

InnoLite II 2.5" SATA SSD support SATA II interface, and compliant with SATA I. SATA II interface can work with Serial Attached SCSI (SAS) host system, which is used in server computer. InnoLite II 2.5" SATA SSD is compliant with Serial ATA Gen 1 and Gen 2 specification (Gen2 supports 1.5Gbps /3.0Gbps data rate). SATA connector uses a 7-pin signal segment and a 15-pin power segment.

1.5 2.5-inch form factor

Industry 2.5-inch standard form factor design with metal material case is easy for installation because 2.5-inch is a popular form factor in industrial field. 2.5-inch is most laptop's hard disk's form factor. InnoLite II 2.5" SATA SSD can easy install in laptop. InnoLite II 2.5" SATA SSD has a compact design 99.88mm (L) x 69.63mm (W) x 9.3mm (H).

1.6 Capacity

InnoLite II 2.5" SATA SSD provides unformatted 8GB, 16GB, 32GB, 64GB, 128GB, 256GB and 512GB capacities within MLC flash ICs.

2. Theory of operation

2.1 Overview

Figure 2 and Figure 3 show the different operation of InnoLite II 2.5" SATA SSD from the system level which separate by 32GB, including the major hardware blocks.

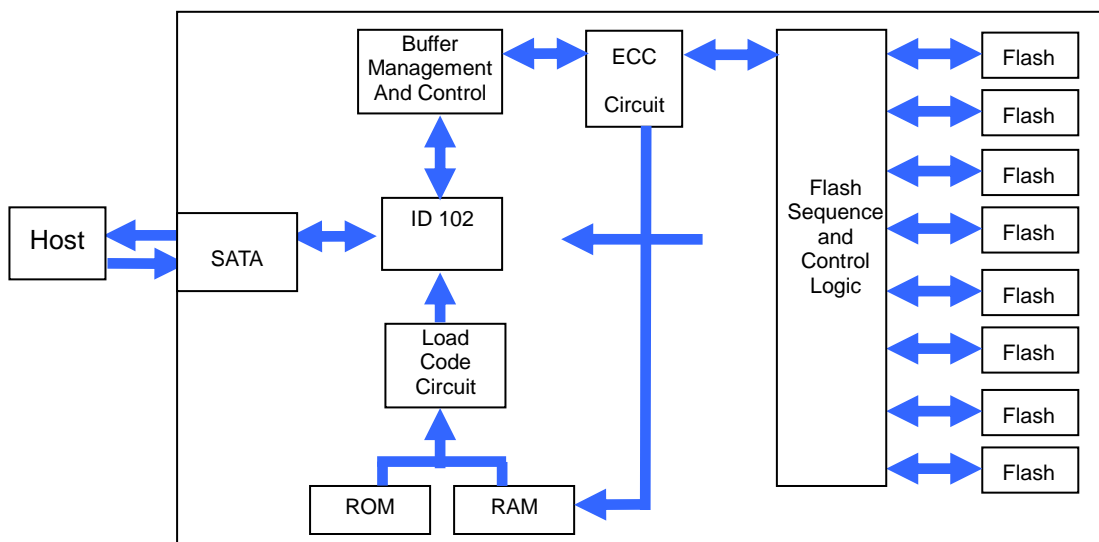


Figure 2: InnoLite II 2.5" SATA SSD Block Diagram From 32GB to 256GB

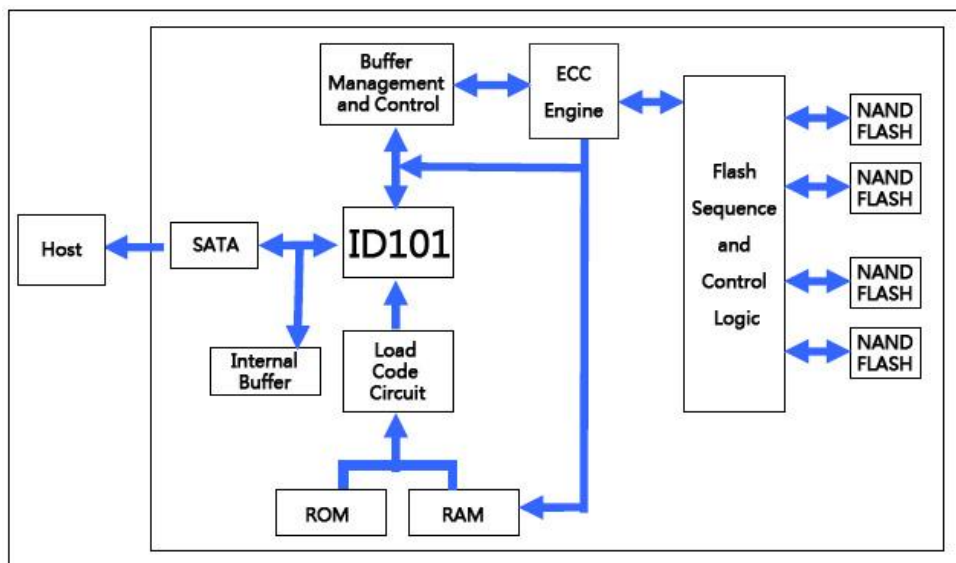


Figure 3: InnoLite II 2.5" SATA SSD Block Diagram From 8GB to 32GB

InnoLite II 2.5" SATA SSD integrates a SATA II controller and NAND flash memories. Communication with the host occurs through the host interface, using the standard ATA protocol. Communication with the flash device(s) occurs through the flash interface.

2.2 SATA II Controller

InnoLite II 2.5" SATA SSD is designed with ID 102 and ID101, a SATA II 3.0 Gbps (Gen. 2) controller, which supports hot-plug. The Serial ATA physical, link and transport layers are compliant with Serial ATA Gen 1 and Gen 2 specification (Gen 2 supports 1.5Gbps/3.0Gbps data rate). The controller has 8 channels/4 channels for flash interface.

2.3 Error Detection and Correction

Highly sophisticated Error Correction Code algorithms are implemented. The ECC unit consists of the Parity Unit (parity-byte generation) and the Syndrome Unit (syndrome-byte computation). This unit implements an algorithm that can correct 16 bits per 1024 bytes in an ECC block. Code-byte generation during write operations, as well as error detection during read operation, is implemented on the fly without any speed penalties.

2.4 Wear-Leveling

Flash memory can be erased within a limited number of times. This number is called the **erase cycle limit** or **write endurance limit** and is defined by the flash array vendor. The erase cycle limit applies to each individual erase block in the flash device.

InnoLite II 2.5" SATA SSD uses a static wear-leveling algorithm to ensure that consecutive writes of a specific sector are not written physically to the same page/block in the flash. This spreads flash media usage evenly across all pages, thereby extending flash lifetime.

2.5 Bad Blocks Management

Bad Blocks are blocks that contain one or more invalid bits whose reliability are not guaranteed. The Bad Blocks may be presented while the SSD is shipped, or may develop during the life time of the SSD. When the Bad Blocks is detected, it will be flagged, and not be used anymore. The SSD implement Bad Blocks management, Bad Blocks replacement, Error Correct Code to avoid data error occurred. The functions will be enabled automatically to transfer data from Bad Blocks to spare blocks, and correct error bit.

3. Installation Requirements

3.1 InnoLite II 2.5" SATA SSD Pin Directions

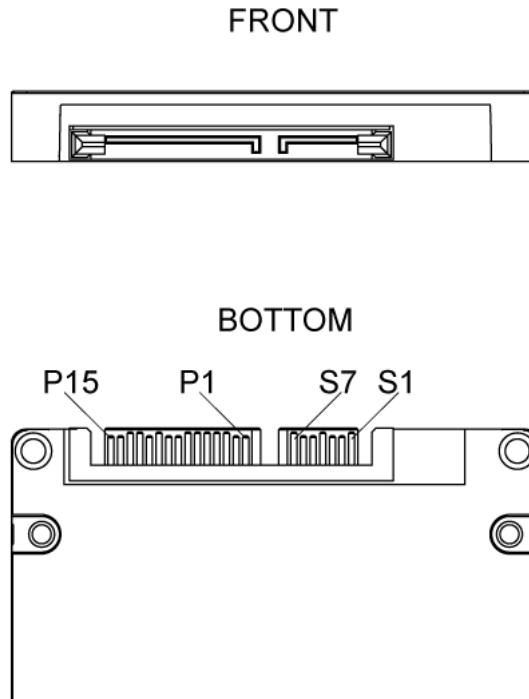


Figure 4: Signal Segment and Power Segment

3.2 Electrical Connections for InnoLite II 2.5" SATA SSD

A Serial ATA device may be either directly connected to a host or connected to a host through a cable. For connection via cable, the cable should be no longer than 1 meter. The SATA interface has a separate connector for the power supply. Please refer to the pin description for further details.

3.3 Form Factor

Please prepare following things:

- Screw driver.
- Four M3 screws.
- SATA single cable (7-pin, Maximum length 1 meter).
- SATA power cable (15-pin).

Please turn off your computer, and open your computer's case. Find one of available 2.5-inch slot, and plug the SSD in. To use the screws fix the SSD. Plug in the SATA single cable, and power cable.

Please boot the installation Operation System from CD-ROM, and install Operation System into SSD.

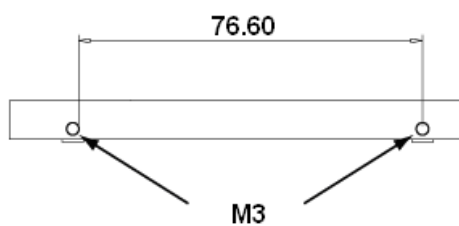


Figure 5: InnoLite II 2.5" SATA SSD Mechanical Screw Hole

3.4 Device drive

No additional device drives are required. The InnoLite II 2.5" SATA SSD can be configured as a boot device.

4. Specifications

4.1 CE and FCC Compatibility

InnoLite II 2.5" SATA SSD conforms to CE and FCC requirements.

4.2 RoHS Compliance

InnoLite II 2.5" SATA SSD is fully compliant with RoHS directive.

4.3 Environmental Specifications

4.3.1 Temperature Ranges

Operating Temperature Range:

- Standard Grade: 0°C to +70°C
- Industrial Grade: -40°C to +85°C

Storage Temperature Range: -55°C to +95°C

4.3.2 Humidity

Relative Humidity: 10-95%, non-condensing

4.3.3 Shock and Vibration

Table 1: Shock/Vibration Testing for InnoLite II 2.5" SATA SSD

Reliability	Test Conditions	Reference Standards
Vibration	7 Hz to 2K Hz, 20G, 3 axes	IEC 68-2-6
Mechanical Shock	Duration: 0.5ms, 1500 G, 3 axes	IEC 68-2-27

4.3.4 Mean Time between Failures (MTBF)

Table 2 summarizes the MTBF prediction results for various InnoLite II 2.5" SATA SSD configurations. The analysis was performed using a RAM Commander™ failure rate prediction.

- **Failure Rate:** The total number of failures within an item population, divided by the total number of life units expended by that population, during a particular measurement interval under stated condition.
- **Mean Time between Failures (MTBF):** A basic measure of reliability for repairable items: The mean number of life units during which all parts of the item perform within their specified limits, during a particular measurement interval under stated conditions.
-

Table 2: InnoLite II 2.5" SATA SSD MTBF

Product	Condition	MTBF (Hours)
InnoLite II 2.5" SATA SSD	Telcordia SR-332 GB, 25°C	>4,000,000

4.4 Endurance

Read Cycles: Unlimited Read Cycles.

Data Retention: 10 years.

Wear-Leveling Algorithm: Support.

Bad Blocks Management: Support

Error Correct Code: Support

4.5 Transfer Mode

InnoLite II 2.5" SATA SSD support following transfer mode:

PIO Mode 0~4

Ultra DMA 0~6

Serial ATA I 1.5Gbps

Serial ATA II 3.0Gbps

4.6 Pin Assignment

InnoLite II 2.5" SATA SSD uses a standard SATA pin-out. See Table 3 for InnoLite II 2.5" SATA SSD pin assignments.

Table 3: InnoLite II 2.5" SATA SSD Pin Assignment

Name	Type	Description
S1	GND	NA
S2	A+	Differential Signal Pair A
S3	A-	
S4	GND	NA
S5	B-	Differential Signal Pair B
S6	B+	
S7	GND	NA
Key and Spacing separate signal and power segments		
P1	NC	NA
P2	NC	NA
P3	NC	NA
P4	GND	NA
P5	GND	NA
P6	GND	NA

P7	V5	5V Power, Pre-Charge
P8	V5	5V Power
P9	V5	5V Power
P10	GND	NA
P11	DAS/DSS	Device Activity Signal / Disable Staggered Spinup
P12	GND	NA
P13	NC	NA
P14	NC	NA
P15	NC	NA

4.7 Mechanical Dimensions

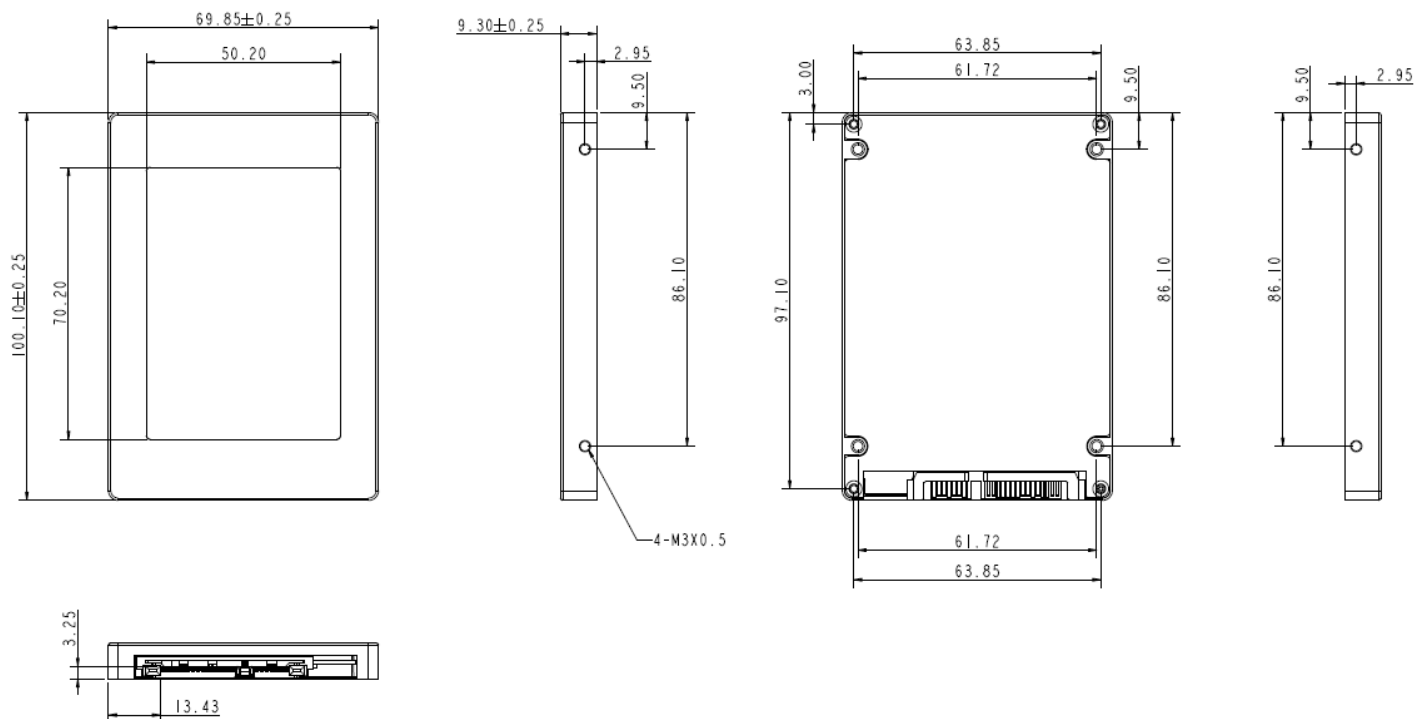


Figure 6: InnoLite II 2.5" SATA SSD mechanical dimensions

4.8 Assembly weight

An InnoLite II 2.5" SATA SSD within MLC flash ICs, 16GB's weight is 90 grams approx. If the capacity is different, the flash chip's weight needs to be added. However, the total weight of SSD will be less than 95 grams.

4.9 Performance

Burst Transfer Rate: 3.0 Gbps

◆ 256GB and 512GB

Sustained Read : 240MB/sec (max.)

Sustained Write : 220MB/sec (max.)

◆ 128GB

Sustained Read : 210MB/sec (max.)

Sustained Write : 145MB/sec (max.)

◆ 64GB

Sustained Read : 210MB/sec (max.)

Sustained Write : 100MB/sec (max.)

◆ 32GB

Sustained Read : 120MB/sec (max.)

Sustained Write : 50MB/sec (max.)

◆ 16GB

Sustained Read : 120MB/sec (max.)

Sustained Write : 25MB/sec (max.)

◆ 8GB

Sustained Read : 60MB/sec (max.)

Sustained Write : 12MB/sec (max.)

4.10 Seek Time

InnoLite II 2.5" SATA SSD is not a magnetic rotating design. There is no seek or rotational latency required.

4.11 Hot Plug

The SSD support hot plug function and can be removed or plugged-in during operation. User has to avoid hot plugging the SSD which is configured as boot device and installed operation system.

Surprise hot plug : The insertion of a SATA device into a backplane (combine signal and power) that has power present. The device powers up and initiates an OOB sequence.

Surprise hot removal: The removal of a SATA device from a powered backplane, without first being placed in a quiescent state.

4.12 NAND Flash Memory

InnoLite II 2.5" SATA SSD uses Multi Level Cell (MLC) NAND flash memory, which is non-volatility, and high reliability which has 3,000 program/erase times and high speed memory storage. There are four statuses, including 00, 01, 10, and 11, of one cell. Read or Write data to flash memory for SSD is control by microprocessor.

4.13 Electrical Specifications

4.13.1 Power Requirement

Table 4: InnoLite II 2.5" SATA SSD Power Requirement

Item	Symbol	Rating	Unit
Input voltage	V _{IN}	+5DC +- 5%	V

4.13.2 Power Consumption

Table 5: Power Consumption

Mode	Power Consumption (mA)
Read	450
Write	560
Idle	200

4.14 Device Parameters

InnoLite II 2.5" SATA SSD device parameters are shown in Table 6.

Table 6: Device parameters

Capacity	LBA	Cylinders	Heads	Sectors	User capacity(MB)
8GB	15649200	16383	16	63	7641.21
16GB	31277232	16383	16	63	15272.08
32GB	62533296	16383	16	63	30533.84
64GB	125045424	16383	16	63	61057.34
128GB	250069680	16383	16	63	122104.34
256GB	TBD	TBD	TBD	TBD	TBD

5. Supported ATA Commands

5.1 Supported ATA Commands

InnoLite II 2.5" SATA SSD supports the commands listed in Table 7.

Table 7: ATA Commands

Command Name	Code	PARAMETERS USED					
		SC	SN	CY	DR	HD	FT
CHECK POWER MODE	E5h	X	X	X	O	X	X
IDENTIFY DEVICE	ECh	X	X	X	O	X	X
IDLE	E3h	O	X	X	O	X	X
IDLE IMMEDIATE	E1h	X	X	X	O	X	X
SMART	B0h	X	X	O	O	X	O
READ MULTIPLE	C4h	O	O	O	O	O	X
READ SECTOR(S)	20h or 21h	O	O	O	O	O	X
READ VERIFY SECTOR(S)	40h or 41h	O	O	O	O	O	X
READ DMA	C8h or C9h	O	O	O	O	O	X
SET FEATURES	Efh	O	X	X	O	X	O
SET MULTIPLE MODE	C6h	O	X	X	O	X	X
SLEEP	E6h	X	X	X	O	X	X
FLUSH CACHE	E7h	X	X	X	O	O	X
STANDBY	E2h	X	X	X	O	X	X
STANDBY IMMEDIATE	E0h	X	X	X	O	X	X
WRITE MULTIPLE	C5h	O	O	O	O	O	X
WRITE SECTOR(S)	30h or 31h	O	O	O	O	O	X
WRITE DMA	Cah or CBh	O	O	O	O	O	X
EXECUTE DIAGNOSTICS	90h	X	X	X	O	X	X
INITIALIZE DEVICE PARAMETERS	91h	O	X	X	O	O	X
SEEK	7xh	X	X	O	O	O	X
RECALIBRATE	10h	X	X	X	O	X	X

Note:

O = Valid,

X = Don't care

SC = Sector Count Register

SN = Sector Number Register

CY = Cylinder Low/High Register

DR = DEVICE SELECT Bit (DEVICE/HEAD Register Bit 4)

HD = HEAD SELECT Bit (DEVICE/HEAD Register Bit 3-0)

FT = Features Register

5.1.1 Check Power Mode

5.1.1.1 Command Code

E5h

5.1.1.2 Feature Set

Power Management feature set.

- This command is mandatory for devices.

-This command is mandatory when the Power Management feature set is implemented.

5.1.1.3 Protocol

Non-data command

5.1.1.4 Inputs

Table 8: Check power mode command for inputs information

Register	7	6	5	4	3	2	1	0
Features	Na							
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	obs	Na	Obs	DEV	Na	Na	Na	Na
Command	E5h							

Device register

DEV shall specify the selected device.

5.1.2 IDENTIFY DEVICE

5.1.2.1 Command Code

Ech

5.1.2.2 Feature Set

General feature set

-Mandatory for all devices.

-Devices implementing the PACKET Command feature set

5.1.2.3 Protocol

PIO data-in

5.1.2.4 Inputs

Table 9: Identify device command for inputs information

Register	7	6	5	4	3	2	1	0
Features	Na							
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	obs	Na	Obs	DEV	Na	Na	Na	Na
Command	Ech							

Device register

DEV shall specify the selected device.

5.1.2.5 Outputs

5.1.2.5.1 Normal outputs

Table 10: Identify device command for normal outputs information

Register	7	6	5	4	3	2	1	0
Error	Na							
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	obs	Na	obs	DEV	Na	Na	Na	Na
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Device register

DEV shall indicate the selected device.

Status register

BSY shall be cleared to zero indicating command completion.

DRDY shall be set to one.

DF (Device Fault) shall be cleared to zero.

DRQ shall be cleared to zero.

ERR shall be cleared to zero.

5.1.2.6 Prerequisites

DRDY set to one.

5.1.2.7 Description

The IDENTIFY DEVICE command enables the host to receive parameter information from the device. When the command is issued, the device sets the BSY bit to one, prepares to transfer the 256 words of device identification data to the host, sets the DRQ bit to one, clears the BSY bit to zero, and asserts INTRQ if nIEN is cleared to zero. The host may then transfer the data by reading

the Data register. Table 8 defines the arrangement and meaning of the parameter words in the buffer. All reserved bits or words shall be zero.

Some parameters are defined as a 16-bit value. A word that is defined as a 16-bit value places the most significant bit of the value on signal line DD15 and the least significant bit on signal line DD0. Some parameters are defined as 32-bit values (e.g. words (61:60)). Such fields are transfer using two successive word transfers. The device will first transfer the least significant bits, bits (15:0) of the value, on signal lines DD(15:0) respectively. After the least significant bits have been transferred, the most significant bits, bits(31:16) of the value, shall be transferred on DD(15:0) respectively.

Some parameters are defined as a string of ASCII characters.

Table 11: Identify device command parameters

Word	Description	Value
0	General configuration bit-significant information: 15 0 = ATA device 14-8 Retired 7 1 = removable media device 6 Obsolete 5-3 Retired 2 Response incomplete 1 Retired 0 Reserved	0040h
1	Obsolete	XXXXh
2	Specific configuration	C837h
3	Obsolete	0010h
4-5	Retired	0000h
6	Obsolete	003Fh
7-8	Reserved for assignment by the CompactFlash™ Association	0000h
9	Retired	0000h
10-19	Serial number (20 ASCII characters)	20 ASCII characters
20-21	Retired	0000h
22	Obsolete	0000h
23-26	Firmware revision (8 ASCII characters)	8 ASCII characters
27-46	Model number (40 ASCII characters)	40 ASCII characters
47	15-8 80h 7-0 00h = Reserved	8001h

	01h-FFh = Maximum number of sectors that shall be transferred per interrupt on READ/WRITE MULTIPLE commands	
48	Reserved	0000h
49	Capabilities 15-14 Reserved for the IDENTIFY PACKET DEVICE command. 13 1 = Standby timer values as specified in this standard are supported 0 = Standby timer values shall be managed by the device 12 Reserved for the IDENTIFY PACKET DEVICE command. 11 1 = IORDY supported 0 = IORDY may be supported 10 1 = IORDY may be disabled 9 1 = LBA supported 8 1 = DMA supported. 7-0 Retired	2F00h
50	Capabilities 15 Shall be cleared to zero 14: Shall be set to one 13-2 Reserved 1 Obsolete 0 Shall be set to one to indicate a device specific Standby timer value minimum.	4000h
51-52	Obsolete	0000h
53	15-3 Reserved 2 1 = the fields reported in word 88 are valid Reserved 0 = the fields reported in word 88 are not valid 1 1 = the fields reported in words (70:64) are valid 0 = the fields reported in words (70:64) are not valid 0 Obsolete	0007h
54	Number of current logical cylinders	XXXXh
55	Number of current logical heads	XXXXh
56	Number of current logical sectors per logical track	XXXXh
57-58	Current capacity in sectors	XXXXh
59	15-9 Reserved 8 1 = Multiple sector setting is valid 7-0 xxh = Current setting for number of sectors that shall be transferred per interrupt on R/W Multiple command	0101h
60-61	Total number of user addressable sectors	XXXXXXXXh
62	Obsolete	0000h
63	15-11 Reserved 10 1 = Multiword DMA mode 2 is selected	XX07h

	0 = Multiword DMA mode 2 is not selected 9 1 = Multiword DMA mode 1 is selected 0 = Multiword DMA mode 1 is not selected 8 1 = Multiword DMA mode 0 is selected 0 = Multiword DMA mode 0 is not selected 7-3 Reserved 2 1 = Multiword DMA mode 2 and below are supported 1 1 = Multiword DMA mode 1 and below are supported 0 1 = Multiword DMA mode 0 is supported	
64	15-8 Reserved 7-0 PIO modes supported	0003h
65	Minimum Multiword DMA transfer cycle time per word 15-0 Cycle time in nanoseconds	0078h
66	Manufacturer's recommended Multiword DMA transfer cycle time 15-0 Cycle time in nanoseconds	0078h
67	Minimum PIO transfer cycle time without flow control 15-0 Cycle time in nanoseconds	0078h
68	Minimum PIO transfer cycle time with IORDY flow control 15-0 Cycle time in nanoseconds	0078h
69-70	Reserved (for future command overlap and queuing)	0000h
71-74	Reserved for the IDENTIFY PACKET DEVICE command.	0000h
75	Queue depth 15-5 Reserved 4-0 Maximum queue depth - 1	001Fh
76-79	Reserved for Serial ATA	0006h
80	Major version number 0000h or FFFFh = device does not report version 15 Reserved 14 Reserved for ATA/ATAPI-14 13 Reserved for ATA/ATAPI-13 12 Reserved for ATA/ATAPI-12 11 Reserved for ATA/ATAPI-11 10 Reserved for ATA/ATAPI-10 9 Reserved for ATA/ATAPI-9 8 Reserved for ATA/ATAPI-8 7 1 = supports ATA/ATAPI-7 6 1 = supports ATA/ATAPI-6 5 1 = supports ATA/ATAPI-5 4 1 = supports ATA/ATAPI-4	01F0h

	3 Obsolete 2 Obsolete 1 Obsolete 0 Reserved	
81	Minor version number 0000h or FFFFh = device does not report version 0001h-FFFEh = See 6.17.41	0000h
82	Command set supported. 15 Obsolete 14 1 = NOP command supported 13 1 = READ BUFFER command supported 12 1 = WRITE BUFFER command supported 11 Obsolete 10 1 = Host Protected Area feature set supported 9 1 = DEVICE RESET command supported 8 1 = SERVICE interrupt supported 7 1 = release interrupt supported 6 1 = look-ahead supported 5 1 = write cache supported 4 Shall be cleared to zero to indicate that the PACKET Command feature set is not supported. 3 1 = mandatory Power Management feature set supported 2 1 = Removable Media feature set supported 1 1 = Security Mode feature set supported 0 1 = SMART feature set supported	7069h
83	Command sets supported. 15 Shall be cleared to zero 14 Shall be set to one 13 1 = FLUSH CACHE EXT command supported 12 1 = mandatory FLUSH CACHE command supported 11 1 = Device Configuration Overlay feature set supported 10 1 = 48-bit Address feature set supported 9 1 = Automatic Acoustic Management feature set supported 8 1 = SET MAX security extension supported 7 See Address Offset Reserved Area Boot, INCITS TR27:2001 6 1 = SET FEATURES subcommand required to spinup after power-up 5 1 = Power-Up In Standby feature set supported 4 1 = Removable Media Status Notification feature set supported	7C08h

	3 1 = Advanced Power Management feature set supported 2 1 = CFA feature set supported 1 1 = READ/WRITE DMA QUEUED supported 0 1 = DOWNLOAD MICROCODE command supported	
84	Command set/feature supported extension 15 Shall be cleared to zero 14 Shall be set to one 13 1 = IDLE IMMEDIATE with UNLOAD FEATURE supported 12 Reserved for technical report 11 Reserved for technical report 10 1 = URG bit supported for WRITE STREAM DMA EXT and WRITE STREAM EXT 9 1 = URG bit supported for READ STREAM DMA EXT and READ STREAM EXT 8 1 = 64-bit World wide name supported 7 1 = WRITE DMA QUEUED FUA EXT command supported 6 1 = WRITE DMA FUA EXT and WRITE MULTIPLE FUA EXT commands supported 5 1 = General Purpose Logging feature set supported 4 1 = Streaming feature set supported 3 1 = Media Card Pass Through Command feature set supported 2 1 = Media serial number supported 1 1 = SMART self-test supported 0 1 = SMART error logging supported	4040h
85	Command and feature sets supported or enabled 15 Obsolete 14 1 = NOP command enabled 13 1 = READ BUFFER command enabled 12 1 = WRITE BUFFER command enabled 11 Obsolete 10 1 = Host Protected Area feature set enabled 9 1 = DEVICE RESET command enabled 8 1 = SERVICE interrupt enabled 7 1 = release interrupt enabled 6 1 = look-ahead enabled 5 1 = Write Cache enabled 4 Shall be cleared to zero to indicate that the PACKET Command feature set is not supported. 3 1 = Power Management feature set enabled 2 1 = Removable Media feature set enabled 1 1 = Security Mode feature set enabled	7069h

	0 1 = SMART feature set enabled	
86	Command set/feature enabled 15-14 0 = Reserved 13 1 = FLUSH CACHE EXT command supported 12 1 = FLUSH CACHE command supported 11 1 = Device Configuration Overlay supported 10 1 = 48-bit Address features set supported 9 1 = Automatic Acoustic Management feature set enabled 8 1 = SET MAX security extension enabled by SET MAX SET PASSWORD 7 See Address Offset Reserved Area Boot, INCITS TR27:2001 6 1 = SET FEATURES subcommand required to spin-up after power-up 5 1 = Power-Up In Standby feature set enabled 4 1 = Removable Media Status Notification feature set enabled 3 1 = Advanced Power Management feature set enabled 2 1 = CFA feature set enabled 1 1 = READ/WRITE DMA QUEUED command supported 0 1 = DOWNLOAD MICROCODE command supported	BC00h
87	Command and feature sets supported or enabled 15 Shall be cleared to zero 14 Shall be set to one 13 1 = IDLE IMMEDIATE with UNLOAD FEATURE supported 12 Reserved for technical report- 11 Reserved for technical report- 10 1 = URG bit supported for WRITE STREAM DMA EXT and WRITE STREAM EXT 9 1 = URG bit supported for READ STREAM DMA EXT and READ STREAM EXT 8 1 = 64 bit World wide name supported 7 1 = WRITE DMA QUEUED FUA EXT command supported 6 1 = WRITE DMA FUA EXT and WRITE MULTIPLE FUA EXT commands supported 5 1 = General Purpose Logging feature set supported 4 1 = Valid CONFIGURE STREAM command has been executed 3 1 = Media Card Pass Through Command feature set enabled 2 1 = Media serial number is valid 1 1 = SMART self-test supported 0 1 = SMART error logging supported	4040h
88	15 Reserved 14 1 = Ultra DMA mode 6 is selected 0 = Ultra DMA mode 6 is not selected 13 1 = Ultra DMA mode 5 is selected 0 = Ultra DMA mode 5 is not selected	XX7Fh

	12 1 = Ultra DMA mode 4 is selected 0 = Ultra DMA mode 4 is not selected 11 1 = Ultra DMA mode 3 is selected 0 = Ultra DMA mode 3 is not selected 10 1 = Ultra DMA mode 2 is selected 0 = Ultra DMA mode 2 is not selected 9 1 = Ultra DMA mode 1 is selected 0 = Ultra DMA mode 1 is not selected 8 1 = Ultra DMA mode 0 is selected 0 = Ultra DMA mode 0 is not selected 7 Reserved 6 1 = Ultra DMA mode 6 and below are supported 5 1 = Ultra DMA mode 5 and below are supported 4 1 = Ultra DMA mode 4 and below are supported 3 1 = Ultra DMA mode 3 and below are supported 2 1 = Ultra DMA mode 2 and below are supported 1 1 = Ultra DMA mode 1 and below are supported 0 1 = Ultra DMA mode 0 is supported	
89	Time required for security erase unit completion	0000h
90	Time required for Enhanced security erase completion	0000h
91	Current advanced power management value	0000h
92	Master Password Revision Code	0000h
93	Hardware reset result. The contents of bits (12:0) of this word shall change only during the execution of a hardware reset. 15 Shall be cleared to zero. 14 Shall be set to one. 13 1 = device detected CBLID- above ViH 0 = device detected CBLID- below ViL 12-8 Device 1 hardware reset result. Device 0 shall clear these bits to zero. Device 1 shall set these bits as follows: 12 Reserved. 11 0 = Device 1 did not assert PDIAG-. 1 = Device 1 asserted PDIAG-. 10-9 These bits indicate how Device 1 determined the device number: 00 = Reserved. 01 = a jumper was used. 10 = the CSEL signal was used. 11 = some other method was used or the method is unknown. 8 Shall be set to one.	XXXXh

	<p>7-0 Device 0 hardware reset result. Device 1 shall clear these bits to zero. Device 0 shall set these bits as follows:</p> <p>7 Reserved.</p> <p>6 0 = Device 0 does not respond when Device 1 is selected. 1 = Device 0 responds when Device 1 is selected.</p> <p>5 0 = Device 0 did not detect the assertion of DASP-. 1 = Device 0 detected the assertion of DASP-.</p> <p>4 0 = Device 0 did not detect the assertion of PDIAG-. 1 = Device 0 detected the assertion of PDIAG-.</p> <p>3 0 = Device 0 failed diagnostics. 1 = Device 0 passed diagnostics.</p> <p>2-1 These bits indicate how Device 0 determined the device number:</p> <p>00 = Reserved. 01 = a jumper was used. 10 = the CSEL signal was used. 11 = some other method was used or the method is unknown.</p> <p>0 Shall be set to one.</p>	
94	<p>15-8 Vendor's recommended acoustic management value.</p> <p>7-0 Current automatic acoustic management value.</p>	0000h
95	Stream Minimum Request Size	0000h
96	Streaming Transfer Time - DMA	0000h
97	Streaming Access Latency - DMA and PIO	0000h
98-99	Streaming Performance Granularity	0000h
100-103	Maximum user LBA for 48-bit Address feature set.	XXXXh
104	Streaming Transfer Time - PIO	0000h
105	Reserved	0000h
106	<p>Physical sector size / Logical Sector Size</p> <p>15 Shall be cleared to zero</p> <p>14 Shall be set to one</p> <p>13 1 = Device has multiple logical sectors per physical sector.</p> <p>12 1 = Device Logical Sector Longer than 256 Words</p> <p>11-4 Reserved</p> <p>3-0 2^x logical sectors per physical sector</p>	4000h
107	Inter-seek delay for ISO-7779 acoustic testing in microseconds	0000h
108	<p>15-12 NAA (3:0)</p> <p>11-0 IEEE OUI (23:12)</p>	0000h
109	<p>15-4 IEEE OUI (11:0)</p> <p>3-0 Unique ID (35:32)</p>	0000h
110	15-0 Unique ID (31:16)	0000h
111	15-0 Unique ID (15:0)	0000h

112-115	Reserved for world wide name extension to 128 bits	0000h
116	Reserved for technical report-	0000h
117-118	Words per Logical Sector	0000h
119-120	Reserved	4000h
121-126	Reserved	0000h
127	Removable Media Status Notification feature set support 15-2 Reserved 1-0 00 = Removable Media Status Notification feature set not supported 01 = Removable Media Status Notification feature supported 10 = Reserved 11 = Reserved	0000h
128	Security Status 15-9 Reserved 8 Security level 0 = high, 1 = Maximum 7-6 Reserved 5 1= Enhanced security erase supported 4 1= Security count expired 3 1 = Security frozen 2 1 = Security locked 1 1 = Security enabled 0 1 = Security supported	0 X 0 0 X X X X 0
129-159	Vendor specific	0000h
160	CFA power mode 1 15 Word 160 supported 14 Reserved 13 CFA power mode 1 is required for one or more commands implemented by the device 12 CFA power mode 1 disabled 11-0 Maximum current in ma	0000h
161-175	Reserved for assignment by the CompactFlash™ Association	0000h
176-205	Current media serial number	0000h
206-254	Reserved	0000h
255	Integrity word 15-8 Checksum 7-0 Signature	XXXXh

5.1.3 IDLE

5.1.3.1 Command Code

E3h

5.1.3.2 Feature Set

Power Management Feature Set.

5.1.3.3 Protocol

Non-Data

5.1.3.4 Inputs

Values other than zero in the Sector Count register when the IDLE command is issued shall determine the time period programmed into the Standby timer.

Table 12: Idle command for inputs information

Register	7	6	5	4	3	2	1	0
Features	Na							
Sector Count	Timer period value							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	Obs	Na	Obs	DEV	Na	Na	Na	Na
Command	E3h							

Device register-

DEV shall specify the selected device.

Table 13: Idle command sector count register contents information

Sector Count register contents	Corresponding timeout period
0 (00h)	Timeout disabled
1-240 (01h-F0h)	(value*5)s
241-251 (F1h-FBh)	((Value-240)*30)min
252 (FCh)	21min
253 (FDh)	Period between 8 and 12 hrs
254 (Feh)	Reserved
255 (FFh)	21 min 15 s
NOTE – Times are approximate	

5.1.3.5 Normal Outputs

Table 14: Idle command for normal outputs information

Register	7	6	5	4	3	2	1	0
Error	Na							

Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	obs	Na	obs	DEV	Na	Na	Na	Na
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Device Register-

DEV shall indicate the selected device.

Status register-

BSY will be cleared to zero indicating command completion.

DRDY will be set to one.

DF (Device Fault) will be cleared to zero.

DRQ shall be cleared to zero.

ERR shall be cleared to zero.

5.1.3.6 Error Outputs

Table 15: Idle command for error outputs information

Register	7	6	5	4	3	2	1	0
Error	Na	Na	Na	Na	Na	ABRT	Na	Na
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	obs	Na	obs	DEV	Na			
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

5.1.3.7 Prerequisites

DRDY set to one

5.1.3.8 Description

The IDLE command allows the host to place the device in the idle mode and also set the Standby timer.

5.1.4 Idle Immediate

5.1.4.1 Command Code

E1h

5.1.4.2 Feature Set

Power Management Feature Set.

5.1.4.3 Protocol

Non-Data

5.1.4.4 Inputs

Table 16: Idle immediate command for inputs information

Register	7	6	5	4	3	2	1	0
Features	Na							
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	obs	Na	obs	DEV	Na	Na	Na	Na
Command	E1h							

Device register-

DEV shall specify the selected device.

5.1.4.5 Normal Outputs

Table 17: Idle immediate command for normal outputs information

Register	7	6	5	4	3	2	1	0
Error	Na							
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	obs	Na	obs	DEV	Na	Na	Na	Na
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Device Register-

DEV shall indicate the selected device.

Status register-

BSY will be cleared to zero indicating command completion.

DRDY will be set to one.

DF (Device Fault) will be cleared to zero.

DRQ shall be cleared to zero.

ERR shall be cleared to zero.

5.1.4.6 Prerequisites

DRDY set to one

5.1.4.7 Description

The IDLE IMMEDIATE command allows the host to immediately place the device in the idle mode.

5.1.5 SMART

Individual SMART commands are identified by the value placed in the Feature register.

Table 18: SMART Feature register values

Value	Command
D0h	SMATR Read Data
D8h	SMART ENABLE OPERATIONS
D9h	SMART DISABLE OPERATIONS

5.1.5.1 SMART Read Data

5.1.5.1.1 Command Code

B0h with a Feature register value of D0h

5.1.5.1.2 Feature Set

Smart Feature Set

- Operation when the SMART feature set is implemented.

5.1.5.1.3 Protocol

PIO data-in

5.1.5.1.4 Inputs

Table 19: SMART command for inputs information

Register	7	6	5	4	3	2	1	0
Features	D0h							
Sector Count	Na							
LBA Low	Na							
LBA Mid	4Fh							
LBA High	C2h							
Device	Obs	Na	obs	DEV	Na	Na	Na	Na
Command	B0h							

Device register-

DEV shall specify the selected device.

5.1.5.1.5 Normal Outputs

Table 20: SMART command for normal outputs information

Register	7	6	5	4	3	2	1	0
Error	Na							
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	Obs	Na	obs	DEV	Na	Na	Na	Na

Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR
--------	-----	------	----	----	-----	----	----	-----

Device Register-

DEV shall indicate the selected device.

Status register-

BSY will be cleared to zero indicating command completion.

DRDY will be set to one.

DF (Device Fault) will be cleared to zero.

DRQ shall be cleared to zero.

ERR shall be cleared to zero.

5.1.5.1.6 Prerequisites

DRDY set to one. SMART enabled.

5.1.5.1.7 Description

This command returns the Device SMART data structure to the host.

Table 21: ID of SMART data structure

ID(Hex)	Description
AA	Total Bad Block Count, Later Bad Block Count
AD	Average Erase Count, Max Erase Count

ID: Aah

Table 22: Smart command for bad block count information

Byte	Function	Description
0	0x00	NA
1	0x00	NA
2	Total Bad Block Count byte 1	Total Bad blocks of SSD
3	Total Bad Block Count byte 0	
4	Later Bad Block Count byte 1	Later Bad blocks of SSD
5	Later Bad Block Count byte 0	
6	Reserved	NA
7	Reserved	NA

ID: Eah

Table 23: Smart command for average/max erase count information

Byte	Function	Description
0	Average Erase Count (High Byte)	Average erase count of all blocks.
1	Average Erase Count	
2	Average Erase Count (Low Byte)	
3	Max Erase Count (High Byte)	Indicate a block which's erase count is the largest.
4	Max Erase Count	
5	Max Erase Count (Low Byte)	
6	Reserved	NA
7	Reserved	NA

- When the Maximum erase count is 255 bigger than average erase count, the wear-leveling will be executed.

ID: Ebh

Table 24: Smart command for average/ max erase count information

Byte	Function	Description
0	Average Erase Count byte 1	Average erase count of all blocks.
1	Average Erase Count byte 0	
2	Max Erase Count byte 1	Indicate a block which's erase count is the largest.
3	Max Erase Count byte 0	
5	Average Erase Count byte 2	
	Max Erase Count byte 2	
6	Reserved	NA
7	Reserved	NA

When the Maximum erase count is 255 bigger than average erase count, the wear-leveling will be executed.

5.1.5.2 SMART ENABLE OPERATIONS

5.1.5.2.1 Command Code

B0h with a Feature register value of D8h

5.1.5.2.2 Feature Set

Smart Feature Set

5.1.5.2.3 Protocol

Non-data

5.1.5.2.4 Inputs

Table 25: SMART Enable command for inputs information

Register	7	6	5	4	3	2	1	0
Features	D8h							
Sector Count	Na							
LBA Low	Na							
LBA Mid	4Fh							
LBA High	C2h							
Device	Obs	Na	obs	DEV	Na	Na	Na	Na
Command	B0h							

Device register-

DEV shall specify the selected device.

5.1.5.2.5 Normal Outputs

Table 26: SMART command for normal outputs information

Register	7	6	5	4	3	2	1	0
Error	Na							
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							

Device	Obs	Na	obs	DEV	Na	Na	Na	Na
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Device Register-

DEV shall indicate the selected device.

Status register-

BSY will be cleared to zero indicating command completion.

DRDY will be set to one.

DF (Device Fault) will be cleared to zero.

DRQ shall be cleared to zero.

ERR shall be cleared to zero.

5.1.5.2.6 Prerequisites

DRDY set to one.

5.1.5.2.7 Description

This command enables access to all SMART capabilities within device.

5.1.5.3 SMART DISABLE OPERATIONS

5.1.5.3.1 Command Code

B0h with a Feature register value of D9h

5.1.5.3.2 Feature Set

Smart Feature Set

5.1.5.3.3 Protocol

Non-data

5.1.5.3.4 Inputs

Table 27: SMART DISABLE Command for inputs information

Register	7	6	5	4	3	2	1	0
Features	D9h							
Sector Count	Na							
LBA Low	Na							
LBA Mid	4Fh							
LBA High	C2h							
Device	Obs	Na	obs	DEV	Na	Na	Na	Na
Command	B0h							

Device register-

DEV shall specify the selected device.

5.1.5.3.5 Normal Outputs

Table 28: SMART command for normal outputs information

Register	7	6	5	4	3	2	1	0
Error	Na							

Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	Obs	Na	obs	DEV	Na	Na	Na	Na
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Device Register-

DEV shall indicate the selected device.

Status register-

BSY will be cleared to zero indicating command completion.

DRDY will be set to one.

DF (Device Fault) will be cleared to zero.

DRQ shall be cleared to zero.

ERR shall be cleared to zero.

5.1.5.3.6 Prerequisites

DRDY set to one. SMART enabled.

5.1.5.3.7 Description

This command disables all SMART capabilities within device.

5.1.6 Read Multiple

5.1.6.1 Command Code

C4h

5.1.6.2 Protocol

PIO data-in

5.1.6.3 Inputs

Table 29: Read multiple command for inputs information

Register	7	6	5	4	3	2	1	0
Features	Na							
Sector Count	Sector Count							
LBA Low	LBA(7:0)							
LBA Mid	LBA(15:8)							
LBA High	LBA(23:16)							
Device	obs	Na	obs	DEV	LBA(27:24)			
Command	C4h							

Sector Count-

Number of sectors to be transferred. A value of 00h specifies that 256 sectors are to be transferred.

LBA Low-

Starting LBA bits (7:0).

LBA Mid-

Starting LBA bits (15:8)

LBA High-

Starting LBA bits (23:16)

Device –

DEV shall specify the selected device.

Bit (3:0) starting LBA bits (27:24)

5.1.6.4 Normal Output

Table 30: Read multiple command for normal output information

Register	7	6	5	4	3	2	1	0
Error	Na							
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	obs	Na	obs	DEV	Na	Na	Na	Na
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Device register-

DEV shall specify the selected device.

Status register

BSY will be cleared to zero indicating command completion

DRDY will be set to one.

DF (Device Fault) will be cleared to zero.

DRQ will be cleared to zero

ERR will be cleared to zero.

5.1.6.5 Error Outputs

An unrecoverable error encountered during the execution of this command results in the termination of the command. The Command Block registers contain the address of the sector where the first unrecoverable error occurred. The amount of data transferred is indeterminate.

Table 31: Read multiple command for error output information

Register	7	6	5	4	3	2	1	0
Error	Na	UNC	MC	IDNF	MCR	ABRT	NM	Obs

Sector Count	Na							
LBA Low	LBA(7:0)							
LBA Mid	LBA(15:8)							
LBA High	LBA(23:16)							
Device	obs	Na	obs	DEV	LBA(27:24)			
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Error register-

UNC shall be set to one if data is uncorrectable.

IDNF shall be set to one if a user-accessible address is requested could not be found.

LBA Low, LBA Mid, and LBA High, Device

Shall be written with the address of first unrecoverable error.

Status register

BSY will be cleared to zero indicating command completion

DRDY will be set to one.

DF (Device Fault) will be cleared to zero.

DRQ will be cleared to zero

ERR will be set to one if an Error register bit is set to one.

5.1.6.6 Prerequisites

DRDY set to one.

5.1.6.7 Description

This command reads the number of sectors specified in the sector Count register.

The number of sectors per block is defined by the content of word 59 in the IDENTIFY DEVICE response.

5.1.7 Read Sector(s)

5.1.7.1 Command Code

20h

5.1.7.2 Protocol

PIO data-in

5.1.7.3 Inputs

Table 32: Read sector command for inputs information

Register	7	6	5	4	3	2	1	0
Features	Na							
Sector Count	Sector Count							
LBA Low	LBA(7:0)							
LBA Mid	LBA(15:8)							
LBA High	LBA(23:16)							
Device	obs	Na	obs	DEV	LBA(27:24)			
Command	20h							

Sector Count-

Number of sectors to be transferred. A value of 00h specifies that 256 sectors are to be transferred.

LBA Low-

Starting LBA bits (7:0).

LBA Mid-

Starting LBA bits (15:8)

LBA High-

Starting LBA bits (23:16)

Device –

DEV shall specify the selected device.

Bit (3:0) starting LBA bits (27:24)

5.1.7.4 Normal Output

Table 33: Read sector command for normal outputs information

Register	7	6	5	4	3	2	1	0
Error	Na							
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	obs	Na	obs	DEV	Na	Na	Na	Na
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Device register-

DEV shall specify the selected device.

Status register

BSY will be cleared to zero indicating command completion

DRDY will be set to one.

DF (Device Fault) will be cleared to zero.

DRQ will be cleared to zero

ERR will be cleared to zero.

5.1.7.5 Error Outputs

An unrecoverable error encountered during the execution of this command results in the termination of the command. The Command Block registers contain the address of the sector where the first unrecoverable error occurred. The amount of data transferred is indeterminate.

Table 34: Read sector command for error outputs information

Register	7	6	5	4	3	2	1	0
Error	Na	UNC	MC	IDNF	MCR	ABRT	NM	Obs
Sector Count	Na							
LBA Low	LBA(7:0)							
LBA Mid	LBA(15:8)							
LBA High	LBA(23:16)							
Device	obs	Na	obs	DEV	LBA(27:24)			
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Error register-

UNC shall be set to one if data is uncorrectable.

IDNF shall be set to one if a user-accessible address is requested could not be found.

LBA Low, LBA Mid, and LBA High, Device

Shall be written with the address of first unrecoverable error.

Status register

BSY will be cleared to zero indicating command completion

DRDY will be set to one.

DF (Device Fault) will be cleared to zero.

DRQ will be cleared to zero

ERR will be set to one if an Error register bit is set to one.

5.1.7.6 Prerequisites

DRDY set to one.

5.1.7.7 Description

This command reads from 1 to 256 sectors as specified in the Sector Count register. A sector count of 0 requests 256 sectors. This transfer shall begin at the sector specified in the LBA Low, LBA Mid, LBA High, and Device registers. The DRQ bit is always set to one prior to data transfer regardless of the presence or absence of an error condition. The device shall interrupt for each DRQ block transferred.

5.1.8 Read Verify Sector

5.1.8.1 Command Code

40h

5.1.8.2 Protocol

Non-data

5.1.8.3 Inputs

Table 35: Read verify sector command for inputs information

Register	7	6	5	4	3	2	1	0
----------	---	---	---	---	---	---	---	---

Features	Na				
Sector Count	Sector Count				
LBA Low	LBA(7:0)				
LBA Mid	LBA(15:8)				
LBA High	LBA(23:16)				
Device	obs	Na	obs	DEV	LBA(27:24)
Command	40h				

Sector Count-

Number of sectors to be transferred. A value of 00h specifies that 256 sectors are to be transferred.

LBA Low-

Starting LBA bits (7:0).

LBA Mid-

Starting LBA bits (15:8)

LBA High-

Starting LBA bits (23:16)

Device –

The LBA bit shall be set to one to specify the address is an LBA.

DEV shall specify the selected device.

Bit (3:0) starting LBA bits (27:24)

5.1.8.4 Normal Output

Table 36: Read verify sector command for normal output information

Register	7	6	5	4	3	2	1	0
Error	Na							
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	obs	Na	obs	DEV	Na	Na	Na	Na
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Device register-

DEV shall specify the selected device.

Status register

BSY will be cleared to zero indicating command completion

DRDY will be set to one.

DF (Device Fault) will be cleared to zero.

DRQ will be cleared to zero

ERR will be cleared to zero.

5.1.8.5 Error Outputs

An unrecoverable error encountered during the execution of this command results in the termination of the command. The Command Block registers contain the address of the sector where the first unrecoverable error occurred.

Table 37: Read verify sector command for normal output information

Register	7	6	5	4	3	2	1	0
Error	Na	UNC	MC	IDNF	MCR	ABRT	NM	Obs
Sector Count	Na							
LBA Low	LBA(7:0)							
LBA Mid	LBA(15:8)							
LBA High	LBA(23:16)							
Device	obs	Na	obs	DEV	LBA(27:24)			
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Error register-

UNC shall be set to one if data is uncorrectable.

IDNF shall be set to one if a user-accessible address could not be found.

LBA Low, LBA Mid, and LBA High, Device

Shall be written with the address of first unrecoverable error.

Status register

BSY will be cleared to zero indicating command completion

DRDY will be set to one.

DF (Device Fault) will be cleared to zero.

DRQ will be cleared to zero

ERR will be set to one if an Error register bit is set to one.

5.1.8.6 Prerequisites

DRDY set to one.

5.1.8.7 Description

This command is identical to the READ SECTOR(s) command, except that the device shall have read the data from the SSD, the DRQ bit is never set to one, and no data is transferred to the host.

5.1.9 Read DMA

5.1.9.1 Command Code

C8h

5.1.9.2 Protocol

DMA

5.1.9.3 Inputs

Table 38: Read DMA command for inputs information

Register	7	6	5	4	3	2	1	0
----------	---	---	---	---	---	---	---	---

Features	Na				
Sector Count	Sector Count				
LBA Low	LBA(7:0)				
LBA Mid	LBA(15:8)				
LBA High	LBA(23:16)				
Device	obs	Na	obs	DEV	LBA(27:24)
Command	C4h				

Sector Count-

Number of sectors to be transferred. A value of 00h specifies that 256 sectors are to be transferred.

LBA Low-

Starting LBA bits (7:0).

LBA Mid-

Starting LBA bits (15:8)

LBA High-

Starting LBA bits (23:16)

Device –

DEV shall specify the selected device.

Bit (3:0) starting LBA bits (27:24)

5.1.9.4 Normal Output

Table 39: Read DMA command for normal output information

Register	7	6	5	4	3	2	1	0
Error	Na							
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	obs	Na	obs	DEV	Na	Na	Na	Na
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Device register-

DEV shall specify the selected device.

Status register

BSY will be cleared to zero indicating command completion

DRDY will be set to one.

DF (Device Fault) will be cleared to zero.

DRQ will be cleared to zero

ERR will be cleared to zero.

5.1.9.5 Error Outputs

An unrecoverable error encountered during the execution of this command results in the termination

of the command. The Command Block registers contain the address of the sector where the first unrecoverable error occurred. The amount of data transferred is indeterminate.

Table 40: Read DMA command for error output information

Register	7	6	5	4	3	2	1	0
Error	ICRC	UNC	MC	IDNF	MCR	ABRT	NM	Obs
Sector Count	Na							
LBA Low	LBA(7:0)							
LBA Mid	LBA(15:8)							
LBA High	LBA(23:16)							
Device	Obs	Na	obs	DEV	LBA(27:24)			
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Error register-

ICRC shall be set to one if an interface CRC error has occurred during an Ultra DMA data transfer. The content of this bit is not applicable for Multiword DMA transfers.

UNC shall be set to one if data is uncorrectable.

IDNF shall be set to one if a user-accessible address could not be found.

LBA Low, LBA Mid, and LBA High, Device

Shall be written with the address of first unrecoverable error.

Status register

BSY will be cleared to zero indicating command completion

DRDY will be set to one.

DF (Device Fault) will be cleared to zero.

DRQ will be cleared to zero

ERR will be set to one if an Error register bit is set to one.

5.1.9.6 Prerequisites

DRDY set to one. The host shall initialize the DMA channel.

5.1.9.7 Description

The READ DMA command allows the host to read data using the DMA data transfer protocol.

5.1.10 Set Feature

TBD

5.1.11 Set Multiple Mode

5.1.11.1 Command Code

C6h

5.1.11.2 Protocol

Non-data

5.1.11.3 Inputs

If the content of the Sector Count Register is not zero, then the Sector Count register contains the number of sectors per block for the device to be used on all following READ/WRITE MULTIPLE

commands. The content of the Sector Count register shall be less than or equal to the value in bits (7:0) in word 47 in the IDENTIFY DEVICE information. The host should set the content of the Sector Count register to 1.

Table 41: Set multiple mode command for inputs information

Register	7	6	5	4	3	2	1	0
Features	Na							
Sector Count	Sector per block							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	obs	Na	obs	DEV	Na			
Command	C6h							

5.1.11.4 Normal Output

Table 42: Set multiple mode command for normal output information

Register	7	6	5	4	3	2	1	0
Error	Na							
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	obs	Na	obs	DEV	Na	Na	Na	Na
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Device register-

DEV shall specify the selected device.

Status register

BSY will be cleared to zero indicating command completion

DRDY will be set to one.

DF (Device Fault) will be cleared to zero.

DRQ will be cleared to zero

ERR will be cleared to zero.

5.1.11.5 Error Outputs

Table 43: Set multiple mode command for error outputs information

Register	7	6	5	4	3	2	1	0
Error	Na	Na	obs	Na	Na	ABRT	Na	Na
Sector Count	Na							

LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	Obs	Na	obs	DEV	Na			
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Status register

BSY will be cleared to zero indicating command completion

DRDY will be set to one.

DF (Device Fault) will be cleared to one if a device fault has occurred.

DRQ will be cleared to zero

ERR will be set to one if an Error register bit is set to one.

5.1.11.6 Prerequisites

DRDY set to one.

5.1.11.7 Description

This command establishes the block count for READ MULTIPLE, READ MULTI EXT, WRITE MULTIPLE.

SSD can only support 1 sector per block.

5.1.12 Set Sleep Mode

5.1.12.1 Command Code

E6h

5.1.12.2 Protocol

Non-data

5.1.12.3 Inputs

Table 44: Set sleep mode for inputs information

Register	7	6	5	4	3	2	1	0
Features	Na							
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	obs	Na	obs	DEV	Na			
Command	E6h							

Device register–

DEV shall specify the selected device.

5.1.12.4 Normal Output

Table 45: Set sleep mode for normal output information

Register	7	6	5	4	3	2	1	0
----------	---	---	---	---	---	---	---	---

Error	Na							
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	obs	Na	obs	DEV	Na	Na	Na	Na
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Device register-

DEV shall specify the selected device.

Status register

BSY will be cleared to zero indicating command completion

DRDY will be set to one.

DF (Device Fault) will be cleared to zero.

DRQ will be cleared to zero

ERR will be cleared to zero.

5.1.12.5 Error Outputs

Table 46: Set sleep mode for error output information

Register	7	6	5	4	3	2	1	0
Error	Na	Na	Na	Na	Na	ABRT	Na	Na
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	Obs	Na	obs	DEV	Na			
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Status register

BSY will be cleared to zero indicating command completion

DRDY will be set to one.

DF (Device Fault) will be set to one if a device fault has occurred.

DRQ will be cleared to zero

ERR will be set to one if an Error register bit is set to one.

5.1.12.6 Prerequisites

DRDY set to one.

5.1.12.7 Description

This command is the only way to cause the device to enter Sleep mode.

5.1.13 Flush Cache

5.1.13.1 Command Code

E7h

5.1.13.2 Protocol

Non-data

5.1.13.3 Inputs

Table 47: Flush cache command for inputs information

Register	7	6	5	4	3	2	1	0
Features	Na							
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	obs	Na	obs	DEV	Na			
Command	E7h							

Device register–

DEV shall specify the selected device.

5.1.13.4 Normal Output

Table 48: Flush cache command for normal output information

Register	7	6	5	4	3	2	1	0
Error	Na							
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	obs	Na	obs	DEV	Na	Na	Na	Na
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Device register–

DEV shall specify the selected device.

Status register

BSY will be cleared to zero indicating command completion

DRDY will be set to one.

DF (Device Fault) will be cleared to zero.

DRQ will be cleared to zero

ERR will be cleared to zero.

5.1.13.5 Error Outputs

Table 49: Flush cache command for error output information

Register	7	6	5	4	3	2	1	0
Error	Na	Na	Na	Na	Na	ABRT	Na	Na
Sector Count	Na							

LBA Low	LBA(7:0)							
LBA Mid	LBA(15:8)							
LBA High	LBA(23:16)							
Device	Obs	Na	obs	DEV	LBA(27:24)			
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Error register-

ABRT may be set to one if the device is not able to complete the action requested by the command.

LBA Low, LBA Mid, and LBA High, Device

Shall be written with the address of first unrecoverable error.

Status register

BSY will be cleared to zero indicating command completion

DRDY will be set to one.

DF (Device Fault) will be cleared to one if a device fault has occurred.

DRQ will be cleared to zero

ERR will be set to one if an Error register bit is set to one.

5.1.13.6 Prerequisites

DRDY set to one.

5.1.13.7 Description

This command is used by the host to request the device to flush the write cache. If there is data in write cache, that data shall be written to the SSD. The BSY bit shall remain set to one until all data has been successfully written or an error occurs.

5.1.14 Standby

5.1.14.1 Command Code

E2h

5.1.14.2 Protocol

Non-data

5.1.14.3 Inputs

The value in the Sector Count register when the STANDBY command is issued shall determine the time period programmed into the Standby timer.

Table 50: Standby command for inputs information

Register	7	6	5	4	3	2	1	0
Features	Na							
Sector Count	Time period value							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	obs	Na	obs	DEV	Na			

Command	E2h
---------	-----

Device register–

DEV shall specify the selected device.

5.1.14.4 Normal Output

Table 51: Standby command for normal output information

Register	7	6	5	4	3	2	1	0
Error	Na							
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	obs	Na	obs	DEV	Na	Na	Na	Na
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Device register–

DEV shall specify the selected device.

Status register

BSY will be cleared to zero indicating command completion

DRDY will be set to one.

DF (Device Fault) will be cleared to zero.

DRQ will be cleared to zero

ERR will be cleared to zero.

5.1.14.5 Error Outputs

Table 52: Standby command for error output information

Register	7	6	5	4	3	2	1	0
Error	Na	Na	Na	Na	Na	ABRT	Na	Na
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	Obs	Na	obs	DEV	Na			
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Error register–

ABRT may be set to one if the device is not able to complete the action requested by the command.

Status register

BSY will be cleared to zero indicating command completion

DRDY will be set to one.

DF (Device Fault) will be set to one if a device fault has occurred.

DRQ will be cleared to zero

ERR will be set to one if an Error register bit is set to one.

5.1.14.6 Prerequisites

DRDY set to one.

5.1.14.7 Description

This command causes the device to enter the Standby mode.

If the Sector Count register is non-zero then Standby timer shall be enabled. The value in the Sector Count register shall be used determine the time programmed into the Standby timer. If the Sector Count register is zero then the Standby timer is disabled.

5.1.15 Standby Immediate

5.1.15.1 Command Code

E0h

5.1.15.2 Protocol

Non-data

5.1.15.3 Inputs

Table 53: Standby immediate command for inputs information

Register	7	6	5	4	3	2	1	0
Features	Na							
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	obs	Na	obs	DEV	Na			
Command	E0h							

Device register—

DEV shall specify the selected device.

5.1.15.4 Normal Output

Table 54: Standby immediate command for normal output information

Register	7	6	5	4	3	2	1	0
Error	Na							
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							

Device	obs	Na	obs	DEV	Na	Na	Na	Na
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Device register-

DEV shall specify the selected device.

Status register

BSY will be cleared to zero indicating command completion

DRDY will be set to one.

DF (Device Fault) will be cleared to zero.

DRQ will be cleared to zero

ERR will be cleared to zero.

5.1.15.5 Error Outputs

Table 55: Standby immediate command for error output information

Register	7	6	5	4	3	2	1	0
Error	Na	Na	Na	Na	Na	ABRT	Na	Na
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	Obs	Na	obs	DEV	Na			
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Error register-

ABRT may be set to one if the device is not able to complete the action requested by the command.

Status register

BSY will be cleared to zero indicating command completion

DRDY will be set to one.

DF (Device Fault) will be set to one if a device fault has occurred.

DRQ will be cleared to zero

ERR will be set to one if an Error register bit is set to one.

5.1.15.6 Prerequisites

DRDY set to one.

5.1.15.7 Description

This command causes the device to immediately enter the Standby mode.

5.1.16 Write Multiple

5.1.16.1 Command Code

C5h

5.1.16.2 Protocol

PIO data-out

5.1.16.3 Inputs

The LBA mid, LBA High, Device, and LBA Low specify the starting sector address to be written. The Sector Count register specifies the number of sectors to be transferred.

Table 56: Write multiple command for inputs information

Register	7	6	5	4	3	2	1	0
Features	Na							
Sector Count	Sector Count							
LBA Low	LBA(7:0)							
LBA Mid	LBA(15:8)							
LBA High	LBA(23:16)							
Device	obs	Na	obs	DEV	LBA(27:24)			
Command	C5h							

Sector Count-

Number of sectors to be transferred. A value of 00h specifies that 256 sectors shall be transferred.

LBA Low-

Starting LBA bits (7:0)

LBA Mid-

Starting LBA bits (15:8)

LBA High-

Starting LBA bits (23:16)

Device –

The LBA bit shall be set to one to specify the address is an LBA.

DEV shall specify the selected device.

Bits(3:0) starting LBA bits (27:24)

5.1.16.4 Normal Output

Table 57: Write multiple command for normal output information

Register	7	6	5	4	3	2	1	0
Error	Na							
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							

Device	obs	Na	obs	DEV	Na	Na	Na	Na
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Device register-

DEV shall specify the selected device.

Status register

BSY will be cleared to zero indicating command completion

DRDY will be set to one.

DF (Device Fault) will be cleared to zero.

DRQ will be cleared to zero

ERR will be cleared to zero.

5.1.16.5 Error Outputs

An unrecoverable error encountered during the execution of this command results in the termination of the command. The Command Block register contain the address of the sector where the first unrecoverable error occurred. The amount of data transferred is indeterminate.

Table 58: Write multiple command for normal output information

Register	7	6	5	4	3	2	1	0
Error	Na	WP	MC	IDNF	MCR	ABRT	NM	Na
Sector Count	Na							
LBA Low	LBA(7:0)							
LBA Mid	LBA(15:8)							
LBA High	LBA(23:16)							
Device	Obs	Na	obs	DEV	LBA(27:24)			
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Error register-

IDNF shall be set to one if a user-accessible address could not be found. IDNF shall be set to one if an address outside of the range user-accessible address is requested if command aborted is not returned.

ABRT shall be set to one if an error, include an ICRC error, has occurred during an Ultra DMA data transfer. ABRT shall be set to one if an address outside of the range of user-accessible address is requested if IDNF is not set to one.

LBA Low, LBA Mid, and LBA High, Device -

Shall be written with the address of first unrecoverable error.

Status register

BSY will be cleared to zero indicating command completion

DRDY will be set to one.

DF (Device Fault) will be set to one if a device fault has occurred.

DRQ will be cleared to zero

ERR will be set to one if an Error register bit is set to one.

5.1.16.6 Prerequisites

DRDY set to one. If bit 8 of IDENTIFY DEVICE word 59 is cleared to zero, a successful SET MULTIPLE MODE command shall proceed a WRITE MULTIPLE command.

5.1.16.7 Description

This command writes the number of sectors specified in the Sector Count register.

The number of sectors per block is defined by the content of word 59 of the IDENTIFY DEVICE response.

When the WRITE MULTIPLE command is issued, the SECTOR Count register contains the number of sectors (not the number of blocks) requested. The device shall interrupt for each DRQ block transferred.

IF the number of requested sectors is not evenly divisible by the block count, as many full blocks as possible are transferred, followed by a final, partial block transfer. The partial block transfer is for n sectors, where:

$N = \text{Remainder (sector count / block count)}$.

If the WRITE MULTIPLE command is received when WRITE MULTIPLE commands are disabled, the Write Multiple operation shall be rejected with command aborted.

Device errors encountered during WRITE MULTIPLE commands are posted after the attempted device write of the block or partial block transferred. The command ends with the sector in error, even if the error was in the middle of a block. Subsequent blocks are not transferred in the event of an error.

The contents of the Command Block Registers following the transfer of a data block that had a sector in error are undefined. The host should retry the transfer as individual requests to obtain valid error information. Interrupt pending is set when the DRQ bit is set to one at the beginning of each block or partial block.

5.1.17 Write Sector

5.1.17.1 Command Code

30h

5.1.17.2 Protocol

PIO data-out

5.1.17.3 Inputs

The LBA mid, LBA High, Device, and LBA Low specify the starting sector address to be written. The Sector Count register specifies the number of sectors to be transferred.

Table 59: Write sector command for inputs information

Register	7	6	5	4	3	2	1	0
Features	Na							
Sector Count	Sector Count							
LBA Low	LBA(7:0)							
LBA Mid	LBA(15:8)							
LBA High	LBA(23:16)							
Device	obs	LBA	obs	DEV	LBA(27:24)			
Command	30h							

Sector Count-

Number of sectors to be transferred. A value of 00h specifies that 256 sectors shall be transferred.

LBA Low-

Starting LBA bits (7:0)

LBA Mid-

Starting LBA bits (15:8)

LBA High-

Starting LBA bits (23:16)

Device –

The LBA bit shall be set to one to specify the address is an LBA.

DEV shall specify the selected device.

Bits(3:0) starting LBA bits (27:24)

5.1.17.4 Normal Output

Table 60: Write sector command for inputs information

Register	7	6	5	4	3	2	1	0
Error	Na							
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	obs	Na	obs	DEV	Na	Na	Na	Na
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Device register-

DEV shall specify the selected device.

Status register

BSY will be cleared to zero indicating command completion

DRDY will be set to one.

DF (Device Fault) will be cleared to zero.

DRQ will be cleared to zero

ERR will be cleared to zero.

5.1.17.5 Error Outputs

An unrecoverable error encountered during the execution if this command results in the termination of the command. The Command Block registers contain the address of the sector where the first unrecoverable error occurred. The amount of data transferred is indeterminate.

Table 61: Write sector command for error outputs information

Register	7	6	5	4	3	2	1	0
Error	Na	WP	MC	IDNF	MCR	ABRT	NM	Na
Sector Count	Na							
LBA Low	LBA(7:0)							
LBA Mid	LBA(15:8)							
LBA High	LBA(23:16)							
Device	Obs	Na	obs	DEV	LBA(27:24)			
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Error register-

IDNF shall be set to one if a user-accessible address could not be found. IDNF shall be set to one if an address outside of the range of user-accessible addresses is requested if command aborted is not returned.

ABRT shall be set to one if an error, including an ICRC error, has occurred during an Ultra DMA data transfer. ABRT shall be set to one if the device is not able to complete the action requested by the command. ABRT shall be set to one if an address outside of the range of user-accessible addresses is requested if IDNF is not set to one.

LBA Low, LBA Mid, and LBA High, Device

Shall be written with the address of first unrecoverable error.

Status register

BSY will be cleared to zero indicating command completion

DRDY will be set to one.

DF (Device Fault) will be set to one if a device fault has occurred.

DRQ will be cleared to zero

ERR will be set to one if an Error register bit is set to one.

5.1.17.6 Prerequisites

DRDY set to one.

5.1.17.7 Description

This command writes from 1 to 256 sectors as specified in the Sector Count register. A sector count of 0 requests 256 sectors. The device shall interrupt for each DRQ block transferred.

5.1.18 Write DMA

5.1.18.1 Command Code

Cah

5.1.18.2 Protocol

DMA

5.1.18.3 Inputs

The LBA Mid, LBA High, Device, and LBA Low specify the starting sector address to be written. The Sector Count register specifies the number of sectors to be transferred.

Table 62: Write DMA command for input information

Register	7	6	5	4	3	2	1	0
Features	Na							
Sector Count	Sector Count							
LBA Low	LBA(7:0)							
LBA Mid	LBA(15:8)							
LBA High	LBA(23:16)							
Device	obs	LBA	obs	DEV	LBA(27:24)			
Command	Cah							

Sector Count-

Number of sectors to be transferred. A value of 00h specifies that 256 sectors shall be transferred.

LBA Low-

Starting LBA bits (7:0)

LBA Mid-

Starting LBA bits (15:8)

LBA High-

Starting LBA bits (23:16)

Device –

The LBA bit shall be set to one to specify the address is an LBA.

DEV shall specify the selected device.

Bits (3:0) starting LBA bits (27:24)

Normal Output

Table 63: Write DMA command for normal output information

Register	7	6	5	4	3	2	1	0
Error	Na							
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	obs	Na	obs	DEV	Na	Na	Na	Na
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Device register-

DEV shall specify the selected device.

Status register

BSY will be cleared to zero indicating command completion

DRDY will be set to one.

DF (Device Fault) will be cleared to zero.

DRQ will be cleared to zero

ERR will be cleared to zero.

5.1.18.4 Error Outputs

Table 64: Write DMA command for error outputs information

Register	7	6	5	4	3	2	1	0
Error	ICRC	WP	MC	IDNF	MCR	ABRT	NM	Obs
Sector Count	Na							
LBA Low	LBA(7:0)							
LBA Mid	LBA(15:8)							
LBA High	LBA(23:16)							
Device	Obs	Na	obs	DEV	LBA(27:24)			
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Error register-

ICRC shall be set to one if an interface CRC error has occurred during an Ultra DMA data transfer. The content of this bit is not applicable for Multiword DMA transfers.

IDNF shall be set to one if a user-accessible address could not be found. IDNF shall be set to one if an address outside of the range of user-accessible address is requested if command aborted is not returned.

ABRT shall be set to one if an error, including an ICRC error, has occurred during an Ultra DMA data transfer. ABRT shall be set to one if the device is not able to complete the action requested by the command. ABRT shall be set to one if an address outside of the range of user-accessible addresses is requested if IDNF is not set to one.

LBA Low, LBA Mid, and LBA High, Device

Shall be written with the address of first unrecoverable error.

Status register

BSY will be cleared to zero indicating command completion

DRDY will be set to one.

DF (Device Fault) will be set to one if a device fault has occurred.

DRQ will be cleared to zero

ERR will be set to one if an Error register bit is set to one.

5.1.18.5 Prerequisites

DRDY set to one. The host shall initialize the DMA channel.

5.1.18.6 Description

The Write DMA command allows the host to write data using the DMA data transfer protocol.

5.1.19 Execute Device Diagnostic

5.1.19.1 Command Code

90h

5.1.19.2 Feature Set

General feature set

5.1.19.3 Protocol

Device diagnostic

5.1.19.4 Inputs

Only the command code (90h). All other registers shall be ignored.

Table 65: Execute device diagnostic command for inputs information

Register	7	6	5	4	3	2	1	0
Features	Na							
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	obs	Na	obs	Na	Na			
Command	90h							

Device –

DEV shall be ignored.

Normal Outputs

The diagnostic code written into the Error register is an 8-bit code.

Table 66: Execute device diagnostic command for normal outputs information

Register	7	6	5	4	3	2	1	0
Error	Diagnostic Code							
Sector Count	Signature							
LBA Low	Signature							
LBA Mid	Signature							
LBA High	Signature							
Device	Signature							
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Error register-

Diagnostic Code

Sector Count, LBA Low, LBA Mid, LBA High, Device registers

Device signature

Device register

DEV shall be cleared to zero.

Status register

TBD

Table 67: Execute device diagnostic command for status register information

Code	Description
01h	Device passed
Others	Device failed

5.1.19.5 Error Outputs

Table 9 shows the error information that is returned as a diagnostic code in the Error register.

5.1.19.6 Prerequisites

This command shall be accepted regardless of the state of DRDY.

5.1.19.7 Description

This command shall cause the devices to perform the internal diagnostic tests.

5.1.20 Read Buffer

5.1.20.1 Command Code

E4h

5.1.20.2 Protocol

PIO data-in

5.1.20.3 Inputs

Table 68: Read Buffer command for inputs information

Register	7	6	5	4	3	2	1	0
Features	Na							
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	obs	Na	obs	DEV	Na			
Command	E4h							

Device –

DEV shall specify the selected device.

5.1.20.4 Normal Output

Table 69: Read Buffer command for normal output information

Register	7	6	5	4	3	2	1	0
Error	Na							
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	obs	Na	obs	DEV	Na	Na	Na	Na
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Device register-

DEV shall specify the selected device.

Status register

BSY will be cleared to zero indicating command completion

DRDY will be set to one.

DF (Device Fault) will be cleared to zero.

DRQ will be cleared to zero

ERR will be cleared to zero.

5.1.20.5 Error Outputs

The device shall return command aborted if the command is not supported.

Table 70: Read Buffer command for error output information

Register	7	6	5	4	3	2	1	0
Error	Na	Na	Na	Na	Na	ABRT	Na	Na
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	Obs	Na	obs	DEV	Na			
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Error register-

ABRT shall be set to one if this command is not supported. ABRT may be set to one if the device is not able to complete the action requested by the command.

Device register -

DEV shall indicate the selected device.

Status register

BSY will be cleared to zero indicating command completion

DRDY will be set to one.

DF (Device Fault) will be cleared to zero.

DRQ will be cleared to zero

ERR will be set to one if an Error register bit is set to one.

5.1.20.6 Prerequisites

DRDY set to one. The command prior to a READ BUFFER command shall be a WRITE BUFFER command.

5.1.20.7 Description

The READ BUFFER command enables the host to read the current contents of the device's sector buffer.

The READ BUFFER and WRITE BUFFER commands shall be synchronized such that sequential WRITE BUFFER and READ BUFFER commands access the same 512 bytes within the buffer.

5.1.21 Write Buffer

5.1.21.1 Command Code

E8h

5.1.21.2

General feature set

- Optional for devices not implementing the PACKET Command feature set.
- Use prohibited for devices implementing the PACKET Command feature set.

5.1.21.3 Protocol

PIO data-out

5.1.21.4 Inputs

Table 71: Write Buffer command for inputs information

Register	7	6	5	4	3	2	1	0
Features	Na							
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	obs	Na	obs	DEV	Na			
Command	E8h							

Device register –

DEV shall specify the selected device.

5.1.21.5 Normal Output

Table 72: Write Buffer command for normal output information

Register	7	6	5	4	3	2	1	0
Error	Na							

Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	obs	Na	obs	DEV	Na	Na	Na	Na
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Device register-

DEV shall specify the selected device.

Status register

BSY will be cleared to zero indicating command completion

DRDY will be set to one.

DF (Device Fault) will be cleared to zero.

DRQ will be cleared to zero

ERR will be cleared to zero.

5.1.21.6 Error Outputs

The device shall return command aborted if the command is not supported.

Table 73: Write Buffer command for error output information

Register	7	6	5	4	3	2	1	0
Error	Na	Na	Na	Na	Na	ABRT	Na	Na
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	Obs	Na	obs	DEV	Na			
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Error register-

ABRT shall be set to one if this command is not supported. ABRT may be set to one if the device is not able to complete the action requested by the command.

Device register -

DEV shall indicate the selected device.

Status register

BSY will be cleared to zero indicating command completion

DRDY will be set to one.

DF (Device Fault) will be cleared to zero.

DRQ will be cleared to zero

ERR will be set to one if an Error register bit is set to one.

5.1.21.7 Prerequisites

DRDY set to one.

5.1.21.8 Description

This command enables the host to write the contents of one sector in the device's buffer.

The READ BUFFER and WRITE BUFFER commands shall be synchronized within the device such that sequential WRITE BUFFER and READ BUFFER commands access the same 512 bytes within the buffer.

6. Part Number Rule

CODE	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
	D	2	S	T	2	-	3	2	G	J	2	0	A	C	1	E	N	-	X	X
Description	Disk	InnoLite II 2.5" SATA SSD					Capacity		Category			FW	Operation Temp.	Internal Control	CH	Flash		Customized Code		
Definition																				
Code 1 st (Disk)									Code 13 th (Operation Temperature)											
D : Disk									C: Standard Grade (0℃ ~ +70℃)											
Code 2 nd ~ 5 th (Form Factor)									W: Industrial Grade (-40℃ ~ +85℃)											
2ST2:InnoLite II 2.5" SATA SSD									Code 14 th (Internal control)											
Code 7 th ~9 th (Capacity)									1: 1 ST version PCB											
08G: 8GB									Code 15 th (Channel of data transfer)											
16G: 16GB									S: Single Channel											
32G: 32GB									D: Dual Channels											
64G: 64GB									Q: Quad Channels											
A28: 128GB									E: Eight Channels											
B56: 256GB									Code 16 th (Flash Type)											
C12: 512GB																				
Code 10 th ~12 th (Series)									N: Micron MLC											
J20: InnoLite II 2.5" SATA SSD(32GB to 256GB)																				
J30: InnoLite II 2.5" SATA SSD(8GB to 32GB)																				
Code 12 th (Firmware version)																				
A: Standard F/W version																				