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the total solution for
Industrial DRAM module

i-DIMM
INDUSTRIAL DRAM MODULE

Approval Sheet

Customer	
Product Number	M1SF-56SB3C03-J (256MB)
Module speed	**PC-3200**
Pin	**200 pin**
CAS Latency	**CL-3**
SDRAM Operating Temp	**0 ℃ ~ 85 ℃**
Date	**25th October 2010**

Approval by Customer

P/N:

Signature:

Date:

Sales:_____ **Sr. Mkt. Manager: John Hsieh**

i-DIMM

1. Features

Key Parameter

Industry Nomenclature	Speed Grade	Data Rate MT/s			tRCD (ns)	tRP (ns)	tRC (ns)
		CL=2	CL=2.5	CL=3			
PC-3200	F	266	333	400	15	15	55

- JEDEC Standard 200-pin Dual In-Line Memory Module
- Intend for 400 MHz applications
- Inputs and Outputs are SSTL-2 compatible
- VDD=VDDQ= 2.6 Volt ± 0.1 (PC-3200)
- Differential clock input
- DLL aligns DQ and DQS transition with CK transition
- Bi-Directional data strobe with one clock cycle
- 30um golden connector
- Built with 512Mb DDR SDRAMs in 400 mil TSOP II packages
- Auto Refresh (CBR) and Self Refresh Modes support.
- Serial Presence Detect with EEPROM
- Auto & self refresh 7.8μs ($T_A \leq +70°C$)
- SDRAM Operation Temperature
  - $0°C \leq T_A \leq +85°C$
- Programmable Device Operation:
  - Burst Type: Sequential or Interleave
  - Device CAS# Latency: 3
  - Burst Length: 2, 4 or 8
- RoHS Compliant *(section 13)*

2. SDRAM Environmental Requirements

iDIMM are intended for use in standard office environments that have limited capacity for heating and air conditioning.

Symbol	Parameter	Rating	Units	Notes
T_{OPR}	Operating Temperature (Ambient)	0 to +65	°C	1
T_{STG}	Storage Temperature	-50 to +100	°C	1

1. The component maximum case temperature (Tcase) shall not exceed the value specified in the DDR DRAM component specification.

3. Ordering Information

DDR SODIMM						
Part Number	Density	Speed	Organization	Number of DRAM	Number of rank	ECC
M1SF-56SB3C03-J	256MB	PC-3200	32M x16	4	1	N/A

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4. Pin Configurations (Front side/Back side)

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	VREF	67	DQ27	135	DQ34	2	VREF	68	DQ31	136	DQ38
3	VSS	69	VDD	137	VSS	4	VSS	70	VDD	138	VSS
5	DQ0	71	*CB0	139	DQ35	6	DQ4	72	*CB4	140	DQ39
7	DQ1	73	*CB1	141	DQ40	8	DQ5	74	*CB5	142	DQ44
9	VDD	75	VSS	143	VDD	10	VDD	76	VSS	144	VDD
11	DQS0	77	*DQS8	145	DQ41	12	DM0	78	*DM8	146	DQ45
13	DQ2	79	*CB2	147	DQS5	14	DQ6	80	*CB6	148	DM5
15	VSS	81	VDD	149	VSS	16	VSS	82	VDD	150	VSS
17	DQ3	83	*CB3	151	DQ42	18	DQ7	84	*CB7	152	DQ46
19	DQ8	85	DU	153	DQ43	20	DQ12	86	DU	154	DQ47
21	VDD	87	VSS	155	VDD	22	VDD	88	VSS	156	VDD
23	DQ9	89	*CK2	157	VDD	24	DQ13	90	VSS	158	/CK1
25	DQS1	91	*/CK2	159	VSS	26	DM1	92	VDD	160	CK1
27	VSS	93	VDD	161	VSS	28	VSS	94	VDD	162	VSS
29	DQ10	95	*CKE1	163	DQ48	30	DQ14	96	CKE0	164	DQ52
31	DQ11	97	DU	165	DQ49	32	DQ15	98	DU	166	DQ53
33	VDD	99	A12	167	VDD	34	VDD	100	A11	168	VDD
35	CK0	101	A9	169	DQS6	36	VDD	102	A8	170	DM6
37	/CK0	103	VSS	171	DQ50	38	VSS	104	VSS	172	DQ54
39	VSS	105	A7	173	VSS	40	VSS	106	A6	174	VSS
KEY		107	A5	175	DQ51	KEY		108	A4	176	DQ55
41	DQ16	109	A3	177	DQ56	42	DQ20	110	A2	178	DQ60
43	DQ17	111	A1	179	VDD	44	DQ21	112	A0	180	VDD
45	VDD	113	VDD	181	DQ57	46	VDD	114	VDD	182	DQ61
47	DQS2	115	A10/AP	183	DQS7	48	DM2	116	BA1	184	DM7
49	DQ18	117	BA0	185	VSS	50	DQ22	118	/RAS	186	VSS
51	VSS	119	/WE	187	DQ58	52	VSS	120	/CAS	188	DQ62
53	DQ19	121	/S0	189	DQ59	54	DQ23	122	*/S1	190	DQ63
55	DQ24	123	DU	191	VDD	56	DQ28	124	DU	192	VDD
57	VDD	125	VSS	193	SDA	58	VDD	126	VSS	194	SA0
59	DQ25	127	DQ32	195	SCL	60	DQ29	128	DQ36	196	SA1
61	DQS3	129	DQ33	197	VDDSPD	62	DM3	130	DQ37	198	SA2
63	VSS	131	VDD	199	*VDDID	64	VSS	132	VDD	200	DU
65	DQ26	133	DQS4			66	DQ30	134	DM4		

Note: *=Not Use ; DU=Don't Use

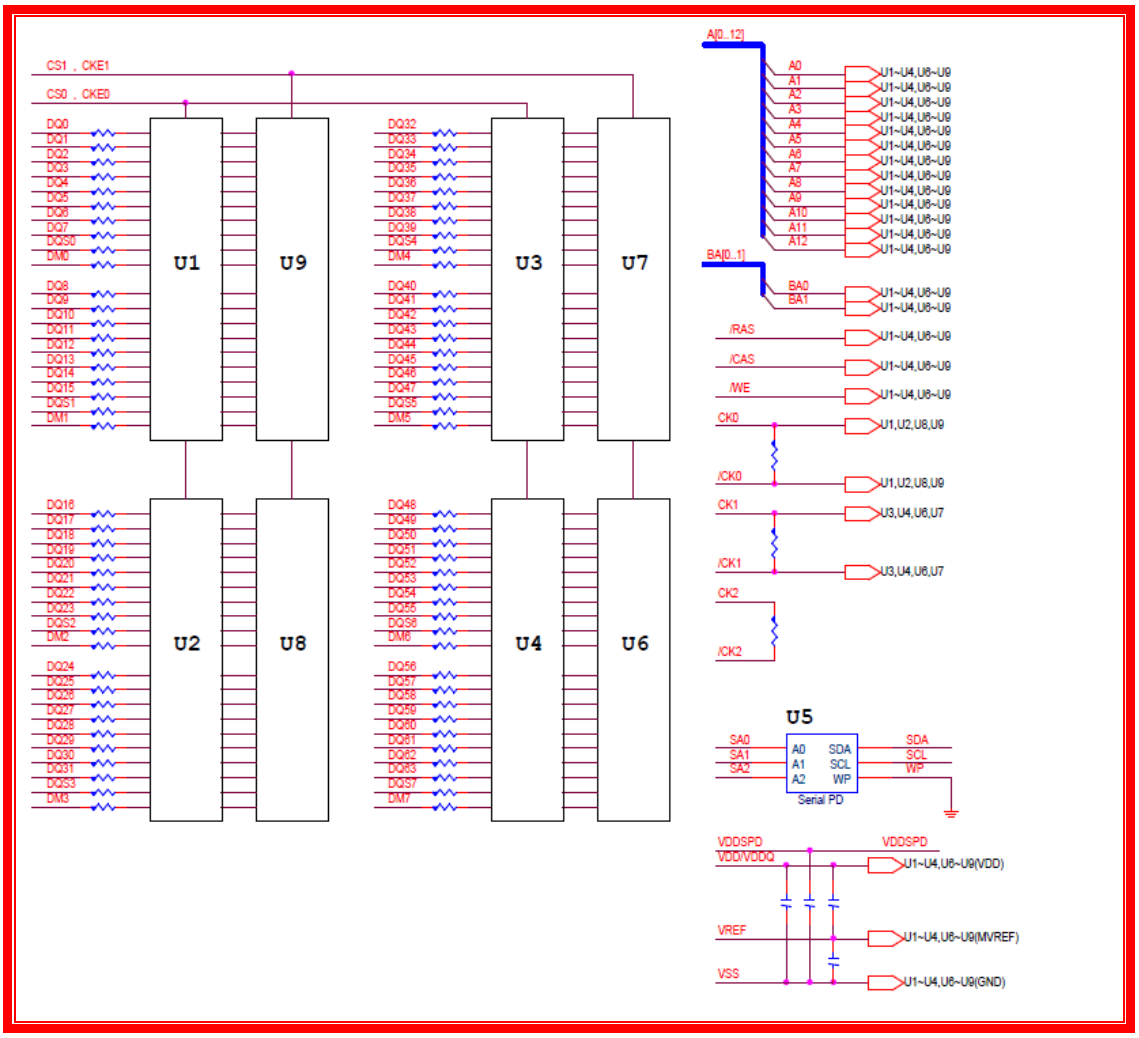
5. Architecture

Pin Definition

Pin Name	Description	Pin Name	Description
A0 - A13 (A14 or A15)	SDRAM address bus	CK0 – CK1 CK0# - CK1#	Differential SDRAM Clocks
BA0 - BA1 (or BA2)	SDRAM Bank Address Inputs	SCL	Serial Presence Detect Clock Input
RAS#	SDRAM row address strobe	SDA	Serial Presence Detect Data input/output
CAS#	SDRAM column address strobe	SA0 – SA2	Serial Presence Detect Address Inputs
WE#	SDRAM write enable	V_{DD}	Power Supply
S0# - S1#	DIMM Rank Select Lines	V_{DDID}	V_{DD} Identification Flag
CK0 – CKE1	SDRAM clock enable lines	V_{DDQ}	SDRAM I/O Driver power supply
DQ0 – DQ63	DIMM memory data bus	V_{REF}	SDRAM I/O Reference supply
CB0 – CB7	DIMM ECC check bit	V_{SS}	Ground
DQS0 – DQS17	SDRAM data strobes	V_{DDSPD}	Serial EEPROM positive power supply
DM0 – DM7	SDRAM data masks	Reset	Reset enable
NC	Spare Pin		

6. Function Block Diagram:

- (256MB, 1 Rank,32Mx64 DDR Unbuffered DIMM)



Note:U6~U9 is for 2Rank 32M16 base DDR modul

7. SDRAM Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
T_A	Operation Temperature	0 to 70	°C
T_{STG}	Storage Temperature	-55 to 150	°C
V_{INPUT}	Voltage input pins relative to Vss	-1.0 to +3.6	V
V_{IO}	Voltage on I/O pins relative to Vss	-0.5 to +3.6	V
V_{DD}	Voltage on VDD supply relative to Vss	-1.0 to +3.6	V
V_{DDQ}	Voltage on VDDQ supply relative to Vss	-1.0 to +3.6	V
I_{OS}	Output short Circuit Current	50	mA

Note: Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

8. AC & DC Operating Conditions

- AC Operating Conditions

(T_{CASE} = 0 °C ~ 70 °C; V_{SS}=0V)

Symbol	Parameter	Value		Units	Notes
		Min	Max		
V_{IH} (AC)	Input High (Logic1) Voltage	V_{REF} + 0.31	-	V	
V_{IL} (AC)	Input Low (Logic0) Voltage	-	V_{REF} + 0.31	V	
V_{ID} (AC)	Input differential Voltage: CK, /CK	0.7	V_{DDQ} + 0.6	V	1
V_{IX} (AC)	Input crossing point Voltage: CK, /CK	0.5* V_{DDQ} + 0.2	0.5* V_{DDQ} - 0.2	V	2

Note:

1. VID is the magnitude of the difference between the input level on CK and the input on /CK.
2. The value of VIX is expected to equal 0.5*V DDQ of the transmitting device and must track variations in the DC level of the same.

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- DC Electrical Characteristics and Operating Conditions

(T_{CASE} = 0 °C ~ 70 °C; V_{SS} = 0V)

Symbol	Parameter	Min	Typ.	Max	Units	Notes
V_{DD}	Supply Voltage (DDR266,333)	2.3	2.5	2.7	V	
	Supply Voltage (DDR400)	2.5	2.6	2.7	V	
V_{DDQ}	Supply Voltage (DDR266,333)	2.3	2.5	2.7	V	
	Supply Voltage (DDR400)	2.5	2.6	2.7	V	
$V_{IH\ (DC)}$	Input High (Logic1) Voltage	V_{REF} + 0.15	-	V_{DDQ} + 0.3	V	1
$V_{IL\ (DC)}$	Input Low (Logic0) Voltage	-0.3	-	V_{REF} - 0.15	V	1
V_{TT}	Termination Voltage	V_{REF}-0.04	V_{REF}	V_{REF}+0.04	V	3
V_{REF}	I/O Reference Voltage	0.49V_{DDQ}	0.5V_{DDQ}	0.51V_{DDQ}	V	2
$V_{IN(DC)}$	Input Voltage Level: CK, /CK	-0.3	-	V_{DDQ} + 0.3	V	
$V_{ID(DC)}$	Input Differential Voltage: CK, /CK	0.36	-	V_{DDQ} + 0.6	V	
$V_{I(RATIO)}$	V-I Matching	0.71	-	1.4	V	

Note:

1. Inputs are not recognized as valid until V_{REF} stabilizes.
2. V_{REF} is expected to be equal to 0.5 V_{DDQ} of the transmitting device, and to track variations in the DC level of the same. Peak-to-peak noise on V_{REF} may not exceed 2% of the DC value.
3. V_{TT} of transmitting device must track V_{REF} of receiving device.

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9. Operating, Standby, and Refresh Currents

- 256MB UDIMM (1 Rank, 32Mx16 DDR SDRAMs T_{CASE} = 0 °C ~ 70 °C)

Symbol	Parameter/Condition	PC-3200	Unit
I_{DD0}	One bank; Active - Precharge; tRC=tRC(min); tCK=tCK(min); DQ,DM and DQS inputs changing twice per clock cycle; address and control inputs changing once per clock cycle	750	mA
I_{DD1}	One bank; Active - Read - Precharge; Burst Length=2; tRC=tRC(min); tCK=tCK(min); address and control inputs changing once per clock cycle	1055	mA
I_{DD2P}	All banks idle; Power down mode; CKE=Low, tCK=tCK(min)	40	mA
I_{DD2F}	/CS=High, All banks idle; tCK=tCK(min); CKE= High; address and control inputs changing once per clock cycle.VIN=VREF for DQ, DQS and DM	215	mA
I_{DD3P}	One bank active ; Power down mode; CKE=Low, tCK=tCK(min)	315	mA
I_{DD3N}	/CS=HIGH; CKE=HIGH; One bank; Active-Precharge;tRC=tRAS(max); tCK=tCK(min); DQ, DM and DQS inputs changing twice per clock cycle; Address and other control inputs changing once per clock cycle	415	mA
I_{DD4R}	Burst=2; Reads; Continuous burst; One bank active; Address and control inputs changing once per clock cycle; tCK=tCK(min); IOUT=0mA	1275	mA
I_{DD4W}	Burst=2; Writes; Continuous burst; One bank active; Address and control inputs changing once per clock cycle; tCK=tCK(min); DQ, DM and DQS inputs changing twice per clock cycle	1335	mA
I_{DD5}	tRC=tRFC(min) - 8*tCK for DDR200 at 100Mhz, 10*tCK for DDR266A & DDR266B at 133Mhz; distributed refresh	1775	mA
I_{DD6}	CKE=<0.2V; External clock on; tCK=tCK(min)	20	mA
I_{DD7}	Four bank interleaving with BL=4 Refer to the following page for detailed test condition	2470	mA

10. AC Timing Specifications

(T_{CASE} = 0 °C ~ 70 °C; V_{DDQ} = V_{DD} , See AC Characteristics)

Symbol	Parameter	PC2-3200		Unit
		Min.	Max.	
tAC	DQ output access time from CK/CK#	-0.7	0.7	ns
tDQSCK	DQS output access time from CK/CK#	-0.55	0.55	ns
tCH	CK high-level width	0.45	0.55	tCK
tCL	CK low-level width	0.45	0.55	tCK
tHP	Minimum half clk period for any given cycle; defined by clk high (tCH) or clk low (tCL) time	Min (tCL,tCH)	-	ns
tCK	Clock Cycle Time	5	10	ns
tDS	DQ and DM input setup time(differential data strobe)	0.4	-	ns
tDH	DQ and DM input hold time(differential data strobe)	0.4	-	ns
tIPW	Input pulse width	2.2	-	ns
tDIPW	DQ and DM input pulse width (each input)	1.75	-	ns
tHZ	Data-out high-impedance time from CK/CK	-0.7	0.7	ns
tLZ(DQS)	DQS low-impedance time from CK/CK	-0.7	0.7	ns
tLZ(DQ)	DQ low-impedance time from CK/CK	-0.7	0.7	ns
tDQSQ	DQS-DQ skew (DQS & associated DQ signals)	-	0.4	ns
tQHS	Data hold Skew Factor	-	0.5	ns
tQH	Data output hold time from DQS	tHP –tQHS	-	ns
tDQSS	Write command to 1st DQS latching transition	0.72	1.25	tCK
tDQSL,(H)	DQS input low (high) pulse width (write cycle)	0.35	-	tCK
tDSS	DQS falling edge to CK setup time (write cycle)	0.35	-	tCK
tDSH	DQS falling edge hold time from CK (write cycle)	0.4	-	tCK
tMRD	Mode register set command cycle time	2	-	tCK
tWPST	Write postamble	0.4	0.6	tCK
tWPRE	Write preamble	0.9	1.1	tCK
tIH	Address and control input hold time	0.6	-	ns

tIS	Address and control input setup time	0.7	-	ns
tRPRE	Read preamble	0.9	1.1	tCK
tRPST	Read postamble	0.4	0.6	tCK
tRRD	Active bank A to Active bank B command	10	-	ns
tREFI	Average Periodic Refresh Interval ($85^oC < T_{CASE} \leq 95^oC$)	-	3.9	µs
	Average Periodic Refresh Interval ($0^oC \leq T_{CASE} \leq 85^oC$)	-	7.8	µs
tCCD	CAS# to CAS# delay	15	-	tCK
tWR	Write recovery time without Auto-Precharge	15		ns
tDAL	Auto precharge write recovery + precharge time	(tWR/tCK) +(tRP/tCK)	-	tCK
tWTR	Internal write to read command delay	2	-	ns
tXSNR	Exit self refresh to a Non-read command	75	-	ns
tXSRD	Exit self refresh to a Read command	200	-	tCK
tCKE	CKE minimum pulse width			tCK

11. SPD

Serial Presence Detect – (256MB)

32Mx64 1 RANK UNBUFFERED DDR SDRAM DIMM based on 32Mx16, 4Banks, 8K Refresh, 2.6V DDR SDRAMs with SPD

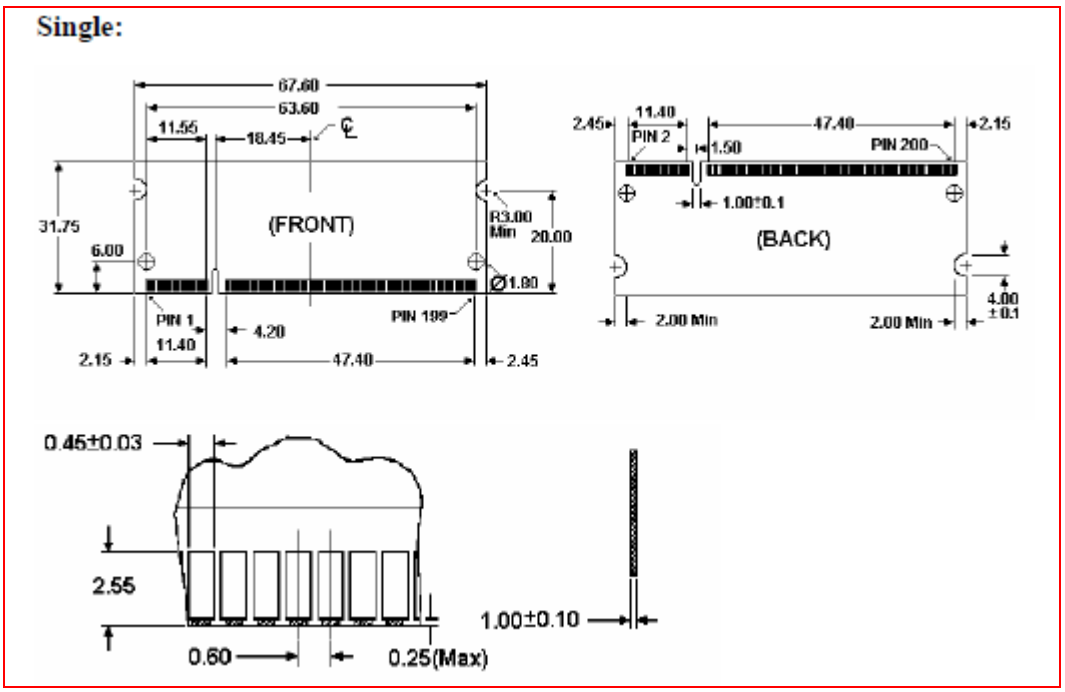
Byte	Description	Serial PD Data Entry (Hexadecimal)	Note
		M1SF-56SB3C03-J	
0	Number of Serial PD Bytes Written during Production	80	
1	Total Number of Bytes in Serial PD device	08	
2	Fundamental Memory Type	07	
3	Number of Row Addresses on Assembly	0D	
4	Number of Column Addresses on Assembly	0A	
5	Number of DIMM Bank, Package, and Height	01	
6	Data Width of this Assembly	40	
7	Reserved	00	
8	Voltage Interface Level of this Assembly	04	
9	DDR2 SDRAM Cycle Time at CL=5 (ns)	50	
10	DDR2 SDRAM Access Time from Clock at CL=5 (ns)	70	
11	DIMM Configuration Type	00	
12	Refresh Rate/Type	82	
13	Primary DDR2 SDRAM Width	10	
14	Error Checking DDR2 SDRAM Device Width	00	
15	Reserved	01	
16	DDR2 SDRAM Device Attributes: Burst Length Supported	0E	
17	DDR2 SDRAM Device Attributes: Number of Device Banks	04	
18	DDR2 SDRAM Device Attributes: ΧΑΣ Latencies Supported	1C	
19	Reserved	01	
20	DDR2 SDRAM DIMM Type Information	02	
21	DDR2 SDRAM Module Attributes:	20	
22	DDR2 SDRAM Device Attributes: General	C0	
23	Minimum Clock Cycle at CL=4	60	

24	Maximum Data Access Time (t_{ac}) from Clock at CL=4 (ns)	70	
25	Minimum Clock Cycle Time at CL=3 (ns)	75	
26	Maximum Data Access Time (t_{ac}) from Clock at CL=3 (ns)	75	
27	Minimum Row Precharge Time (t_{RP}) (ns)	3C	
28	Minimum Row Active to Row Active delay (t_{RRD})	28	
29	Minimum RAS to CAS delay (t_{RCD}) (ns)	3C	
30	Minimum RAS Pulse Width (t_{RAS})	28	
31	Module Bank Density	40	
32	Address and Command Setup Time Before Clock (t_{IS}) (ns)	60	
33	Address and Command Hold Time After Clock (t_{IH}) (ns)	60	
34	Data Input Setup Time Before Clock (t_{DS})	40	
35	Data Input Hold Time After Clock (t_{DH}) (ns)	40	
36	Write Recovery Time (t_{WR})	00	
37	Internal Write to Read Command delay (t_{WTR})	00	
38	Internal Read to Precharge delay (t_{RTP})	00	
39	Memory Analysis Probe Characteristics	00	
40	Extension of Byte 41 t_{RC} and Byte 42 t_{RFC}	00	
41	Minimum Core Cycle Time (t_{RC}) (ns)	37	
42	Min. Auto Refresh Command Cycle Time (t_{RFC})	46	
43	Maximum Clock Cycle Time (t_{CK})	28	
44	Max. DQS-DQ Skew Factor (t_{DQS}) (ns)	28	
45	Read Data Hold Skew Factor (t_{QHS}) (ns)	50	
46	PLL Relock Time	00	
47	Tcasemax DT4R4W Delta	00	
48	Thermal Resistance of DRAM Package from Top (Case) to Ambient (Psi-T-A DRAM)	00	
49	DRAM Case Temperature Rise from Ambient due to Activate-Precharge/Mode Bits (DT0/Mode Bits)	00	
50	DRAM Case Temperature Rise from Ambient due to Precharge/Quiet Standby (DT2N/DT2Q)	00	

51	DRAM Case Temperature Rise from Ambient due to Precharge Power-Down (DT2P)	00	
52	DRAM Case Temperature Rise from Ambient due to Active Standby (DT3N)	00	
53	DRAM Case Temperature Rise from Ambient due to Active Power-Down with Fast PDN Exit (DT3Pfast)	00	
54	DRAM Case Temperature Rise from Ambient due to Active Power-Down with Slow PDN Exit (DT3Pslow)	00	
55	DRAM Case Temperature Rise from Ambient due to Page Open Burst Read/DT4R4W Mode Bit (DT4R/DT4R4W Mode Bit)	00	
56	DRAM Case Temperature Rise from Ambient due to Burst Refresh (ST5B)	00	
57	DRAM Case Temperature Rise from Ambient due to Bank interleave Reads with Auto-Precharge (DT7)	00	
58	Thermal Resistance of PLL Package from Top (Case) to Ambient (Psi T-A PLL)	00	
59	Thermal Resistance of Register Package from Top (Case) to Ambient (Psi T-A Register)	00	
60	PLL Case Temperature Rise from Ambient due to PLL Active (DT PLL Active)	00	
61	Register Case Temperature Rise from Ambient due to Register Active/Mode Bit (DT Register Active/Mode Bit)	00	
62	SPD Reversion	11	
63	Checksum for byte 0-62	7F	
64-71	Manufacture's JEDEC ID Code	InnoDisk	
72	Module Manufacturing Location	Manufacturing Code	
73-91	Module Part number	Module Part Number in ASCII	
92-255	Reserved	Undefined	

12. PACKAGE DIMENSION

- (256MB, 1 Rank, 32Mx16 DDR SDRAMs)



Note: Device position is only for reference.

13. RoHS Declaration

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Declaration of Conformity

We, InnoDisk Co., Ltd, here declare the product M1SF-56SB1C03-G complies with the requirement of RoHS directives 2002/95/EC and 2006/122/EC.

Innodisk ensures the above product meets RoHS requirements of six restricted substances. This declaration is based on vendor supplied analysis/MSDS, material certifications, and/ or 3rd party test reports of the component/ raw materials used in the manufacture of products.

Name of hazardous substance	Limited of RoHS ppm（mg/kg）
Cd	< 100 ppm
Pb	< 1000 ppm
Hg	< 1000 ppm
Chromium VI（Cr+6）	< 1000 ppm
Polybromodiphenyl ether（PBDE）	< 1000 ppm
Polybrominated Biphenyls（PBB）	< 1000 ppm
Perfluorooctane Sulfonate (PFOS)	Not Contained

Date issued : 2010/10/23

Manufacturer: : InnoDisk Co., Ltd.
Address : 9F, No. 100, Sec.1 Xintai 5th Rd., Xizhi City, Taipei 221, Taiwan

Authorized Signature :

QA Dept. Director - Terry Hsu

Revision Log

Rev	Date	Modification
0.1	27th May 2010	Preliminary Edition
1.0	25th August 2010	Official Released.
1.1	25th October 2010	Added RoHS declaration.