

Model Name: P550HVN05.0

Issue Date : 2014/7/17

(*) Preliminary Specifications

() Final Specifications

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Record of Revision

Version	Date	Page	Description
00	2014/04/24		First Release
01	2014/6/24	6	Backlight power correct from typ:97.4,max:103 to typ.120.8, max 127.5
		18	Input current correct from typ.:4.05, max:4.29 to typ.: 5.03, max:5.31
		18	Input power correct from typ.97.4, max:103 to typ.:120.8, max:127.5
		24	Drawing update
		25	Drawing update
0.2	2014/7/10	7	Add TCON and Driver characteristic
		31	Precaution modified.
		27	Reliability test condition correct.

1. General Description

This specification applies to the 55 inch Color TFT-LCD Module P550HVN05.0. This LCD module has a TFT active matrix type liquid crystal panel 1,920x1,080 pixels, and diagonal size of 55.0 inch. This module supports 1,920x1080 mode. Each pixel is divided into Red, Green and Blue sub-pixels or dots which are arranged in vertical stripes. Gray scale or the brightness of the sub-pixel color is determined with a 8/10-bits gray scale signal for each dot.

The P550HVN05.0 has been designed to apply the 8/10-bits 2 channel LVDS interface method. It is intended to support displays where high brightness, and wide viewing angle.

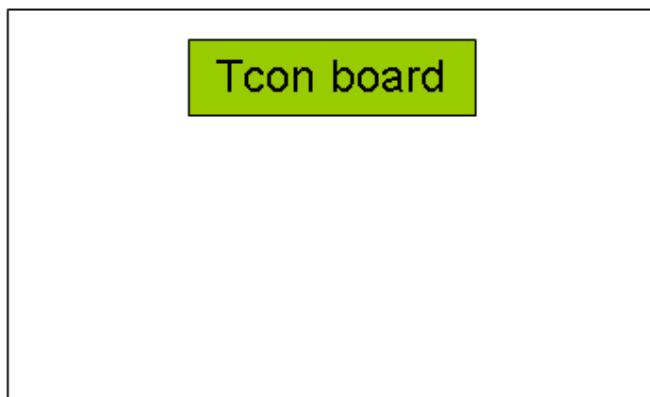
* General Information

Items	Specification	Unit	Note
Active Screen Size	55.0	Inch	
Display Area	1209.6(H) x 680.4(V)	mm	
Outline Dimension	1219.0(H) x 689.8(V) x 37.5(D)	mm	1
Driver Element	a-Si TFT active matrix		
Display Colors	8bits, 16.58M	Colors	2
Number of Pixels	1,920x1080	Pixel	
Pixel Pitch	0.21 (H) x 0.63(W)	mm	
Pixel Arrangement	RGB vertical stripe		
Display Operation Mode	Normally Black		
Display Orientation	Landscape/Portrait Enable		
Surface Treatment	AG		Haze = 11%

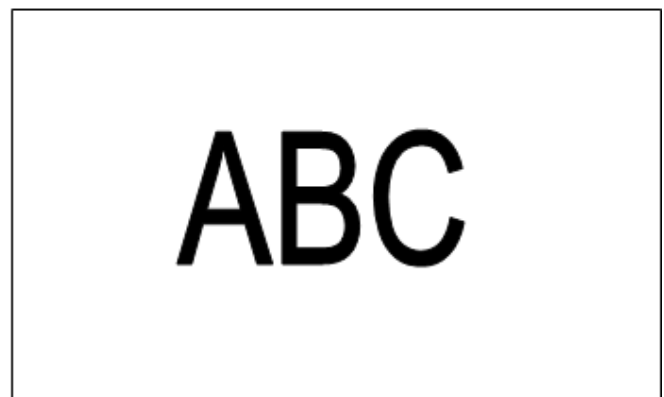
Note:

- (1) Dmax: 55mm (Front bezel to Driver cover); Dmin: 37.5mm (Front bezel to Bezel back)
- (2) 8/10 Bits select function is available.

Rear side



Front side



2. Absolute Maximum Ratings

The followings are maximum values which, if exceeded, may cause faulty operation or damage to the unit

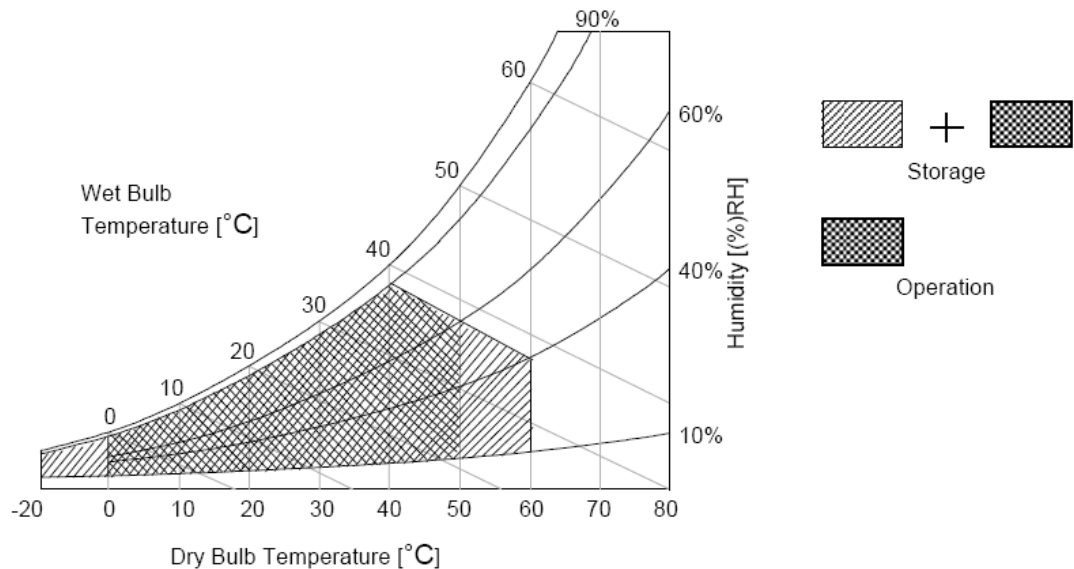
Item	Symbol	Min	Max	Unit	Conditions
Logic/LCD Drive Voltage	Vcc	-0.3	14	[Volt]	Note 1
Input Voltage of Signal	Vin	-0.3	4	[Volt]	Note 1
Operating Temperature	TOP	0	+50	[°C]	Note 2
Operating Humidity	HOP	10	90	[%RH]	Note 2
Storage Temperature	TST	-20	+60	[°C]	Note 2
Storage Humidity	HST	10	90	[%RH]	Note 2
Panel Surface Temperature	PST		65	[°C]	Note 3

Note 1: Duration:50 msec.

Note 2 : Maximum Wet-Bulb should be 39°C and No condensation.

The relative humidity must not exceed 90% non-condensing at temperatures of 40°C or less. At temperatures greater than 40°C, the wet bulb temperature must not exceed 39°C.

Note 3: Surface temperature is measured at 50°C Dry condition



3. Electrical Specification

The P550HVN05.0 requires two power inputs. One is employed to power the LCD electronics and to drive the TFT array and liquid crystal. The second is employed for LED driver.

3.1 Electrical Characteristics

3.1.1 DC Characteristics (Ta = 25 ± 2 °C)

Parameter		Symbol	Value			Unit	Note
			Min.	Typ.	Max		
LCD							
Power Supply Input Voltage		V _{DD}	10.8	12	13.2	V _{DC}	
Power Supply Input Current		I _{DD}	--	0.88	1.05	A	1
Power Consumption		P _C	--	10.56	12.6	Watt	1
Inrush Current		I _{RUSH}	--	--	2	A	2
Permissible Ripple of Power Supply Input Voltage (for input power=12V)		V _{RP}	--	--	V _{DD} * 5%	mV _{pk-pk}	3
LVDS Interface	Input Differential Voltage	V _{ID}	200	400	600	mV _{DC}	4
	Differential Input High Threshold Voltage	V _{TH}	+100	--	+300	mV _{DC}	4
	Differential Input Low Threshold Voltage	V _{TL}	-300	--	-100	mV _{DC}	4
	Input Common Mode Voltage	V _{ICM}	1.1	1.25	1.4	V _{DC}	4
CMOS Interface	Input High Threshold Voltage	V _{IH} (High)	2.7	--	3.3	V _{DC}	7
	Input Low Threshold Voltage	V _{IL} (Low)	0	--	0.6	V _{DC}	
Backlight Power Consumption		P _{BL}		120.8	127.5	W	
Life Time(MTTF)				50000		--	8

3.1.2 AC Characteristics (Ta = 25 ± 2 °C)

Parameter		Symbol	Value			Unit	Note
			Min.	Typ.	Max		
LVDS Interface	Receiver Clock : Spread Spectrum Modulation range	Fclk_ss	Fclk -3%	--	Fclk +3%	MHz	9
	Receiver Clock : Spread Spectrum Modulation frequency	Fss	30	--	200	KHz	9
	Receiver Data Input Margin Fclk = 85 MHz Fclk = 65 MHz	tRMG	-0.4 -0.5	-- --	0.4 0.5	ns	10

3.1.3 Driver Characteristics

Item	Symbol	Min	Max	Unit	condition
Driver Surface Temperature	DST		100	[°C]	Note

Note : Any point on the driver surface must be less than 100°C under any conditions.

3.1.4 TCON Characteristics

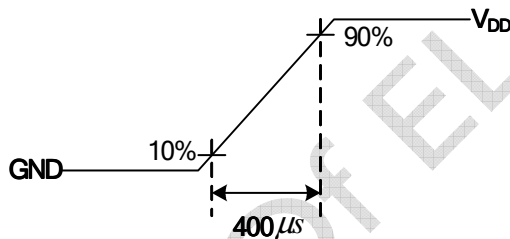
Item	Symbol	Min	Max	Unit	condition
TCON Surface Temperature	TST		85	[°C]	Note

Note: Any point on the TCON surface must be less than 85°C under any conditions.

Note :

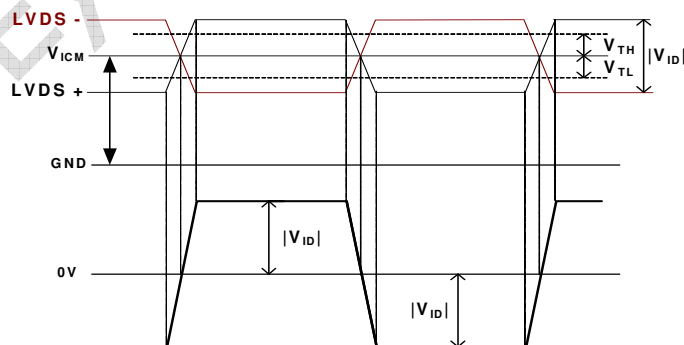
1. Test Condition:
 - (1) $V_{DD} = 12.0V$
 - (2) $F_v =$ Type Timing, 60Hz, 120Hz or Other
 - (3) $F_{CLK} =$ Max freq.
 - (4) Temperature = 25 °C
 - (5) Test Pattern : White Pattern

2. Measurement condition : Rising time = 400us



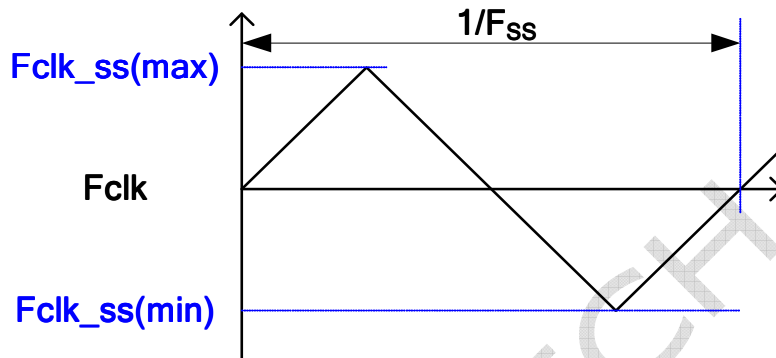
3. Test Condition:
 - (1) The measure point of V_{RP} is in LCM side after connecting the System Board and LCM.
 - (2) Under Max. Input current spec. condition.

4. $V_{ICM} = 1.25V$



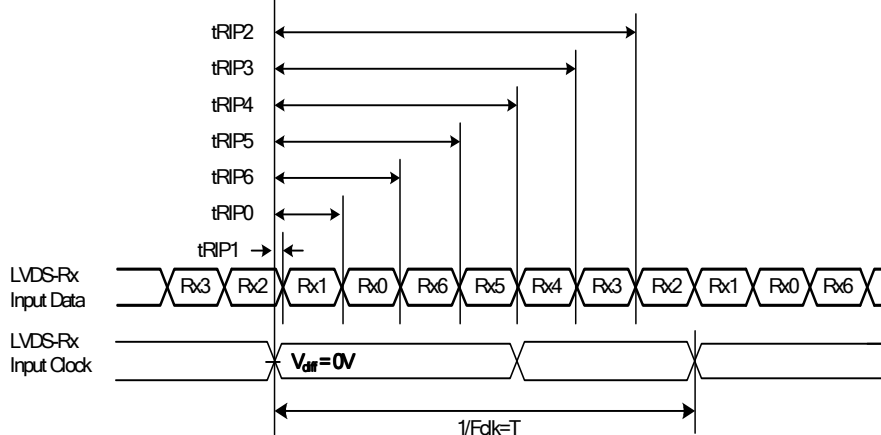
5. Do not attach a conducting tape to lamp connecting wire. If the lamp wire attach to conducting tape, TFT-LCD Module have a low luminance and the inverter has abnormal action because leakage current occurs between lamp wire and conducting tape.

6. The relative humidity must not exceed 80% non-condensing at temperatures of 40°C or less. At temperatures greater than 40°C, the wet bulb temperature must not exceed 39°C. When operate at low temperatures, the brightness of LED will drop and the life time of LED will be reduced.
7. The measure points of V_{IH} and V_{IL} are in LCM side after connecting the System Board and LCM.
8. The lifetime (MTTF) is defined as the time which luminance of the LED is 50% compared to its original value. [Operating condition: Continuous operating at $T_a = 25 \pm 2^\circ\text{C}$]
9. LVDS Receiver Clock SSCG (Spread spectrum clock generator) is defined as below figures



10. Receiver Data Input Margin

Parameter	Symbol	Rating			Unit	Note
		Min	Type	Max		
Input Clock Frequency	Fclk	Fclk (min)	--	Fclk (max)	MHz	$T=1/Fclk$
Input Data Position0	tRIP1	- tRMG	0	tRMG	ns	
Input Data Position1	tRIP0	$T/7 - tRMG $	$T/7$	$T/7 + tRMG $	ns	
Input Data Position2	tRIP6	$2T/7 - tRMG $	$2T/7$	$2T/7 + tRMG $	ns	
Input Data Position3	tRIP5	$3T/7 - tRMG $	$3T/7$	$3T/7 + tRMG $	ns	
Input Data Position4	tRIP4	$4T/7 - tRMG $	$4T/7$	$4T/7 + tRMG $	ns	
Input Data Position5	tRIP3	$5T/7 - tRMG $	$5T/7$	$5T/7 + tRMG $	ns	
Input Data Position6	tRIP2	$6T/7 - tRMG $	$6T/7$	$6T/7 + tRMG $	ns	



3.2 Interface Connections

● LCD connector : JAE FI-RE51S-HF

PIN	Symbol	Description	PIN	Symbol	Description
1	V _{DD}	12V Power Supply	27	CH2_1-	LVDS Even pixel data input pair 1(-)
2	V _{DD}	12V Power Supply	28	CH2_1+	LVDS Even pixel data input pair 1(+)
3	V _{DD}	12V Power Supply	29	CH2_2-	LVDS Even pixel data input pair 2(-)
4	V _{DD}	12V Power Supply	30	CH2_2+	LVDS Even pixel data input pair 2(+)
5	V _{DD}	12V Power Supply	31	GND	GND
6	N.C.	No connection	32	CH2_CLK-	LVDS Even pixel clock input pair(-)
7	GND	GND	33	CH2_CLK+	LVDS Even pixel clock input pair(+)
8	GND	GND	34	GND	GND
9	GND	GND	35	CH2_3-	LVDS Even pixel data input pair 3(-)
10	CH1_0-	LVDS Odd pixel data input pair 0(-)	36	CH2_3+	LVDS Even pixel data input pair 3(+)
11	CH1_0+	LVDS Odd pixel data input pair 0(+)	37	CH2_4-	LVDS Even pixel data input pair 4(-)
12	CH1_1-	LVDS Odd pixel data input pair 1(-)	38	CH2_4+	LVDS Even pixel data input pair 4(+)
13	CH1_1+	LVDS Odd pixel data input pair 1(+)	39	GND	GND
14	CH1_2-	LVDS Odd pixel data input pair 2(-)	40	NC	No connection
15	CH1_2+	LVDS Odd pixel data input pair 2(+)	41	BITSEL.	High(3.3V) : LVDS input 10bits Open/Low (GND) : LVDS input 8bits
16	GND	GND	42	NC	No connection
17	CH1_CLK-	LVDS Odd pixel clock input pair(-)	43	NC	No connection
18	CH1_CLK+	LVDS Odd pixel clock input pair(+)	44	NC	No connection
19	GND	GND	45	LVDS_SEL	High(3.3V) for NS, Open/Low(GND) for JEIDA
20	CH1_3-	LVDS Odd pixel data input pair 3(-)			
21	CH1_3+	LVDS Odd pixel data input pair 3(+)	46	NC	No connected
22	CH1_4-	LVDS Odd pixel data input pair 4(-)	47	NC	No connected
23	CH1_4+	LVDS Odd pixel data input pair 4(+)	48	NC	No connected
24	GND	GND	49	NC	No connected
25	CH2_0-	LVDS Even pixel data input pair 0(-)	50	NC	No connected
26	CH2_0+	LVDS Even pixel data input pair 0(+)	51	NC	No connected

Note 1: All GND (ground) pins should be connected together and should also be connected to the LCD's metal frame.

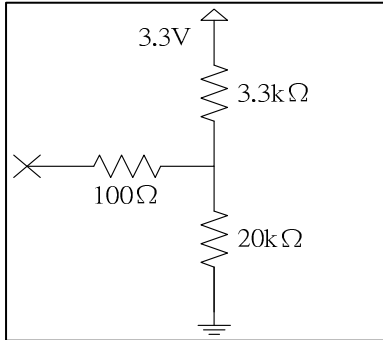
Note 2: All V_{DD} (power input) pins should be connected together.

Note 3: All NC (no connection) pins should be open without voltage input.

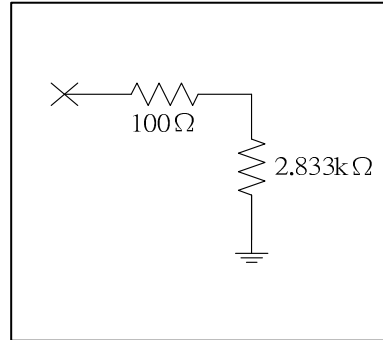
Note 4: If Customers would like to apply 8bit input, please note that not only pin 41 needs to set as open/low, but also pin 22, 23, 37, and 38 all need to set as N.C.

● LVDS connector control pin description

Note * : Open/High(3.3V)

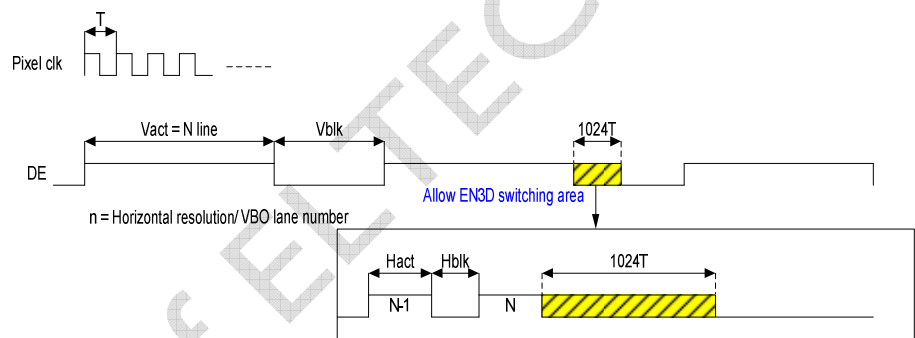
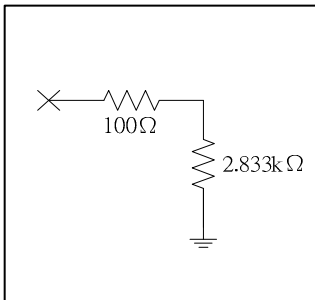


Note ** : Open/Low(GND)

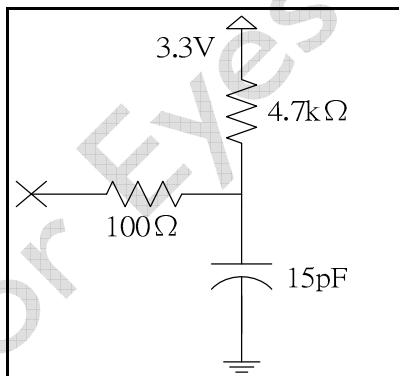


Note * : Open/Low(GND)**

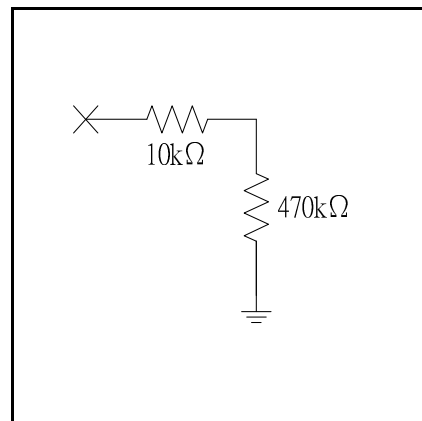
The switch range of 3D_EN control signal is from the last DE falling to 1024T. (T is a pixel clk)



Note ** : SCL/SDA**

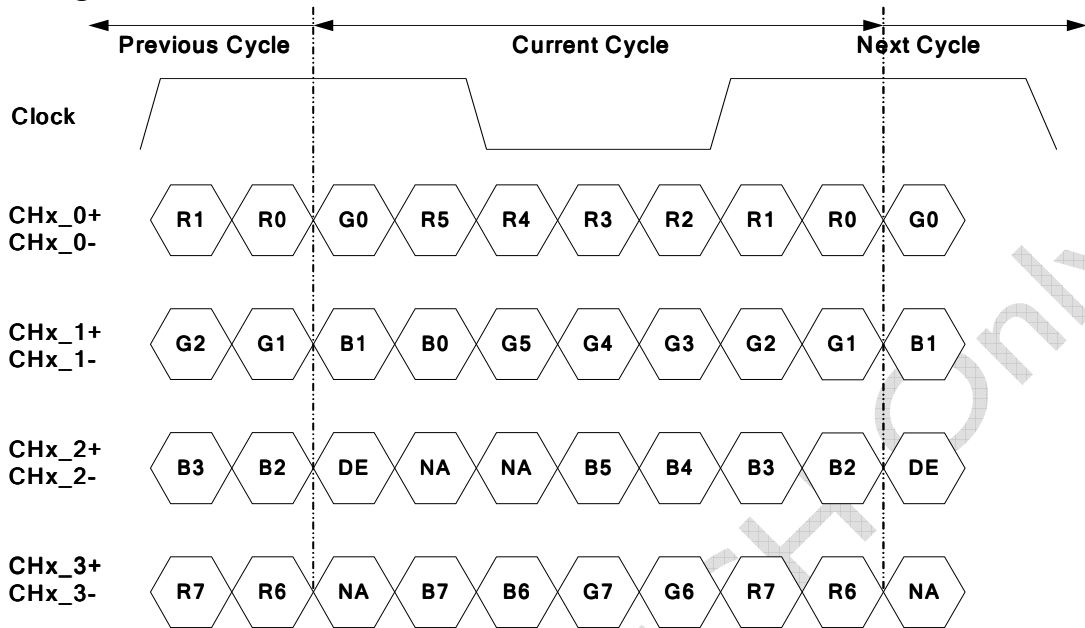


Note *** : WP**



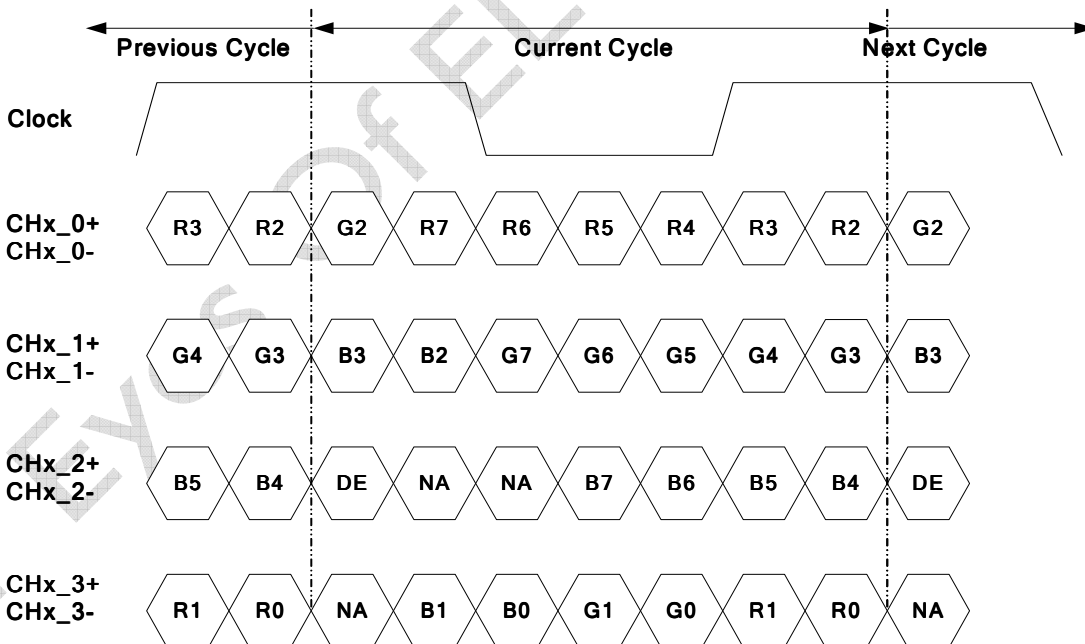
LVDS Option for 8bits

LVDS Option = High → NS



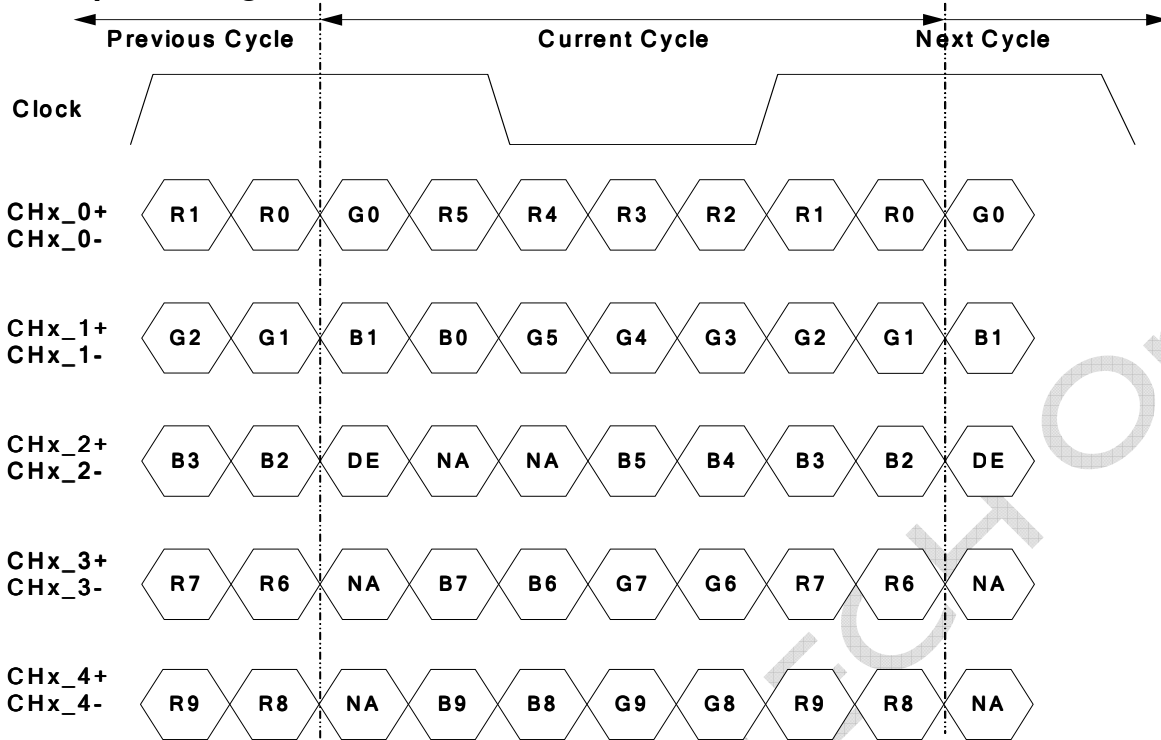
Note: x = 1, 2, 3, 4...

LVDS Option = Low / Open → JEIDA (8 bits Mode)



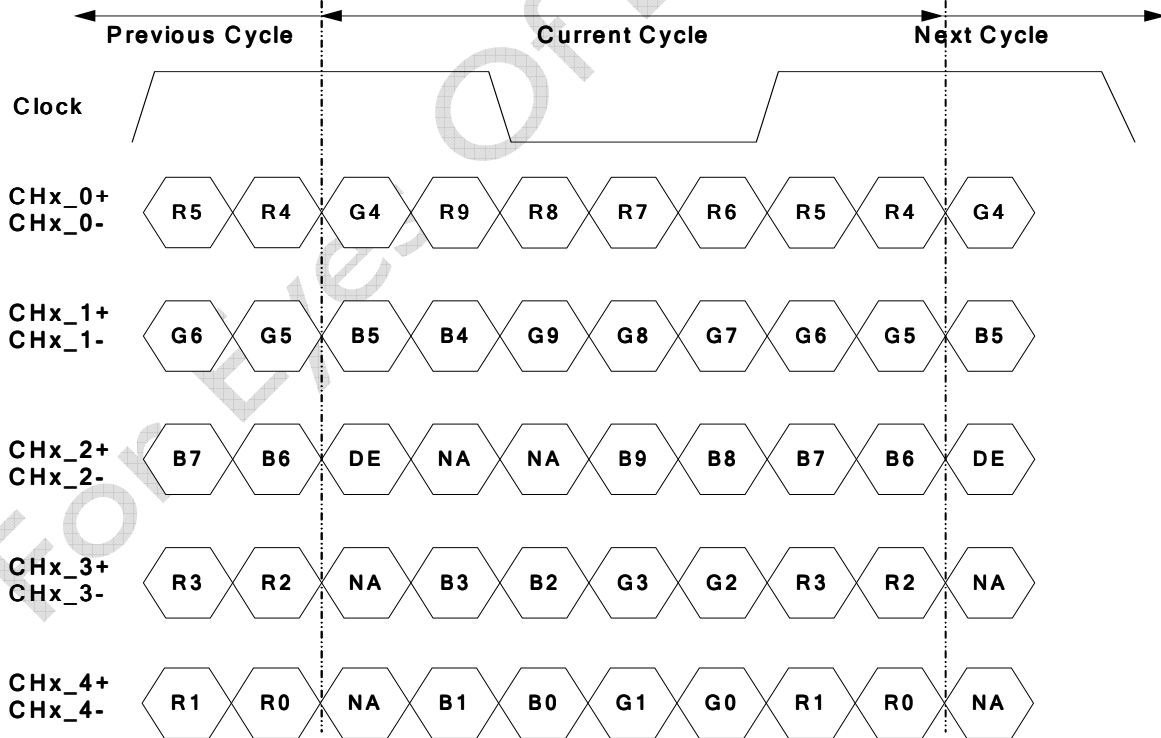
Note: x = 1, 2, 3, 4...

LVDS Option for 10bits
LVDS Option = High→NS



Note: x = 1, 2, 3, 4...

LVDS Option = Low / Open→JEIDA



Note: x = 1, 2, 3, 4...

3.3 Signal Timing Specification

This is the signal timing required at the input of the user connector. All of the interface signal timing should be satisfied with the following specifications for its proper operation.

Timing Table (DE only Mode)

Vertical Frequency Range (60Hz)

Signal	Item	Symbol	Min.	Typ.	Max	Unit
Vertical Section	Period	Tv	1100	1125	1480	Th
	Active	Tdisp (v)	1080			Th
	Blanking	Tblk (v)	20	45	400	Th
Horizontal Section	Period	Th	1060	1100	1328	Tclk
	Active	Tdisp (h)	960			Tclk
	Blanking	Tblk (h)	100	140	368	Tclk
Clock	Frequency	Fclk=1/Tclk	53	74.25	82	MHz
Vertical Frequency	Frequency	Fv	47	60	63	Hz
Horizontal Frequency	Frequency	Fh	60	67.5	73	KHz

Notes:

(1) Display position is specific by the rise of DE signal only.

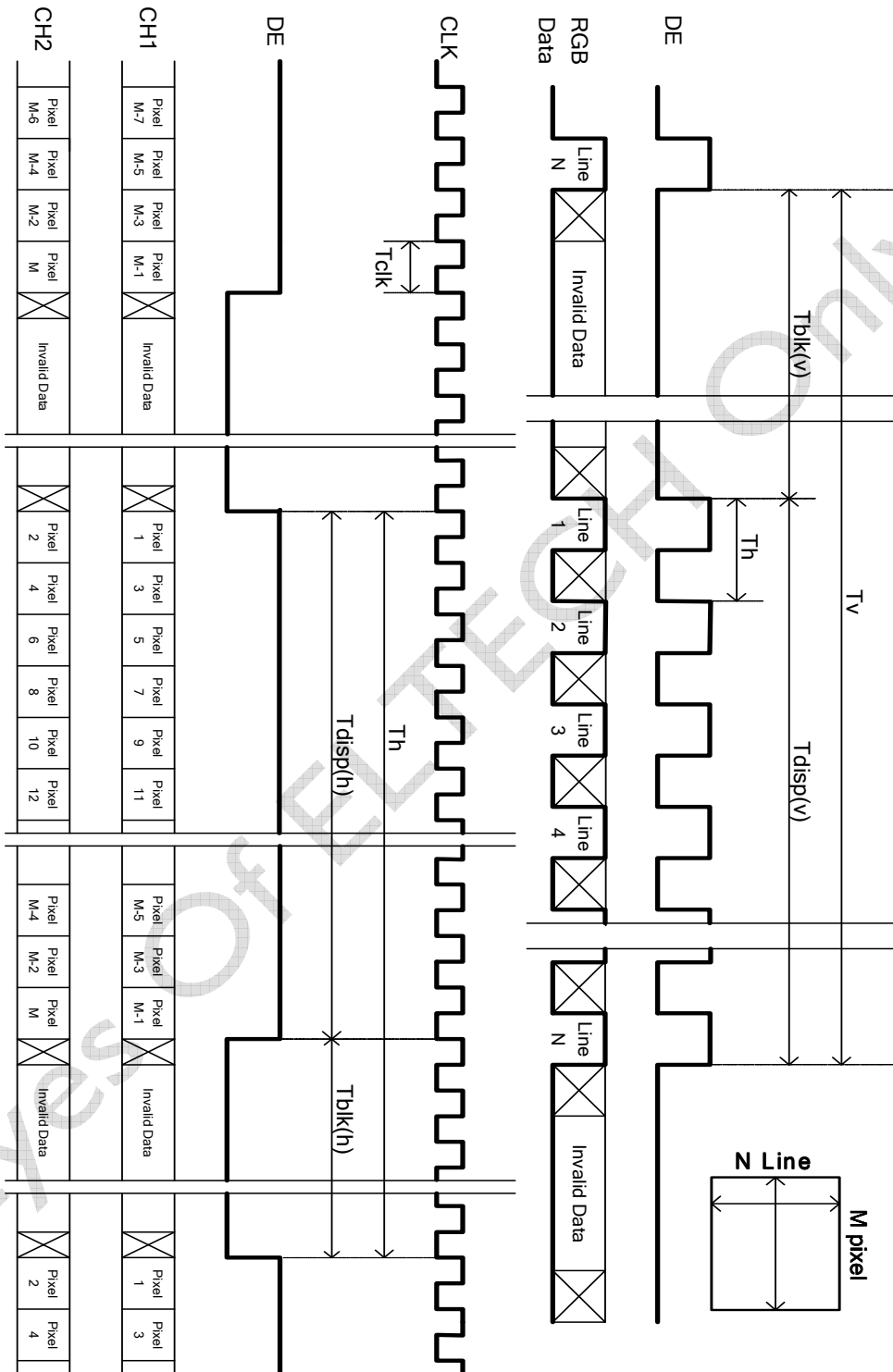
Horizontal display position is specified by the rising edge of 1st DCLK after the rise of 1st DE, is displayed on the left edge of the screen.

(2) Vertical display position is specified by the rise of DE after a "Low" level period equivalent to eight times of horizontal period. The 1st data corresponding to one horizontal line after the rise of 1st DE is displayed at the top line of screen.

(3) If a period of DE "High" is less than 1920 DCLK or less than 1080 lines, the rest of the screen displays black.

(4) The display position does not fit to the screen if a period of DE "High" and the effective data period do not synchronize with each other.

3.4 Signal Timing Waveforms



3.5 Color Input Data Reference

3.5.1 LVDS Option for 8bits

The brightness of each primary color (red, green and blue) is based on the 8 bits gray scale data input for the color; the higher the binary input, the brighter the color. The table below provides a reference for color versus data input.

Color		Input Color Data																							
		RED								GREEN								BLUE							
		MSB				LSB				MSB				LSB				MSB				LSB			
		R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0
Basic Color	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(255)	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green(255)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	Blue(255)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Cyan	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	Magenta	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
R	RED(000)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	RED(001)	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	RED(254)	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	RED(255)	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
G	GREEN(000)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	GREEN(001)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0

	GREEN(254)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0
	GREEN(255)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
B	BLUE(000)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	BLUE(001)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

	BLUE(254)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0
	BLUE(255)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

3.5.2 LVDS Option for 10bits

The brightness of each primary color (red, green and blue) is based on the 10 bits gray scale data input for the color; the higher the binary input, the brighter the color. The table below provides a reference for color versus data input.

Color		Input Color Data																													
		RED										GREEN										BLUE									
		MSB					LSB					MSB					LSB					MSB					LSB				
		R9	R8	R7	R6	R5	R4	R3	R2	R1	R0	G9	G8	G7	G6	G5	G4	G3	G2	G1	G0	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Basic Color	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(1023)	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green(1023)	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0
	Blue(1023)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1
	Cyan	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	Magenta	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
R	RED(000)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	RED(001)	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	

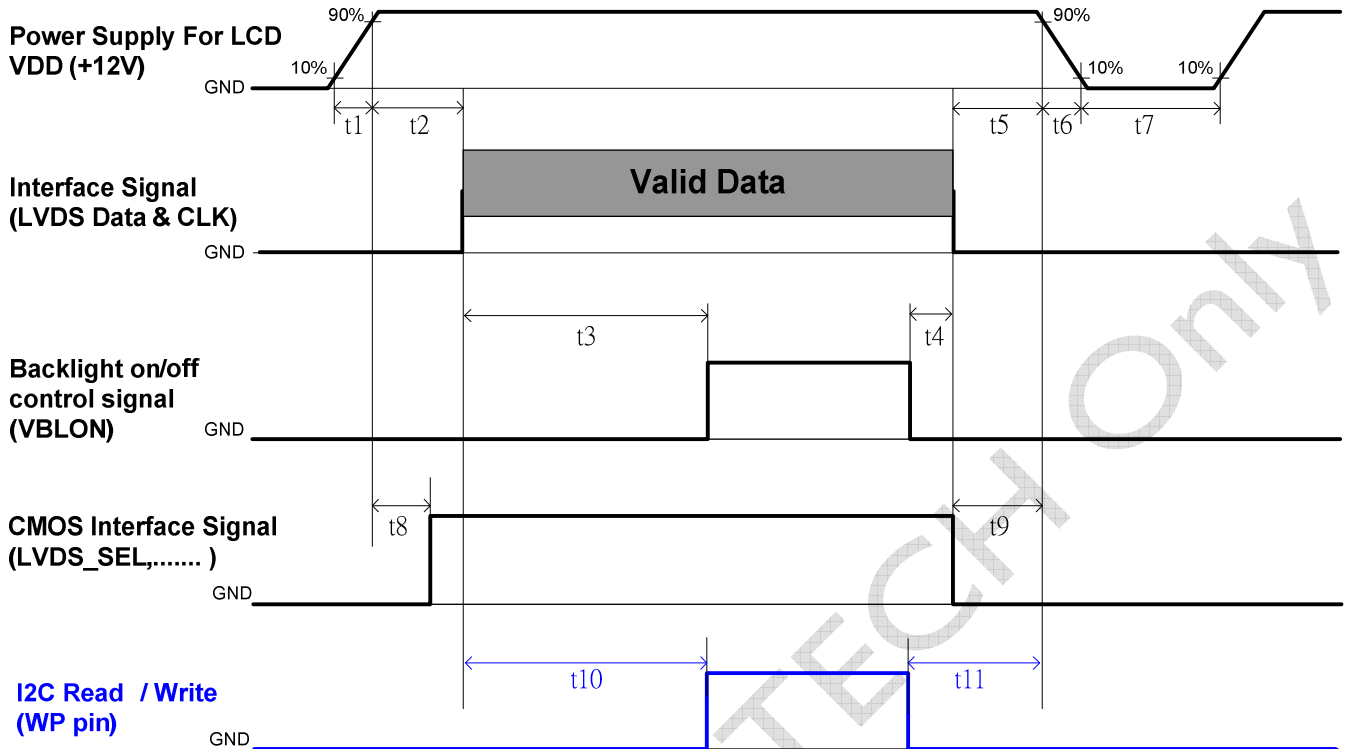
	RED(1022)	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	RED(1023)	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
G	GREEN(000)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	GREEN(001)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	

	GREEN(1022)	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	
	GREEN(1023)	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	
B	BLUE(000)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	BLUE(001)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	

	BLUE(1022)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	0	
	BLUE(1023)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	

3.6 Power Sequence

◆ Power Sequence of LCD

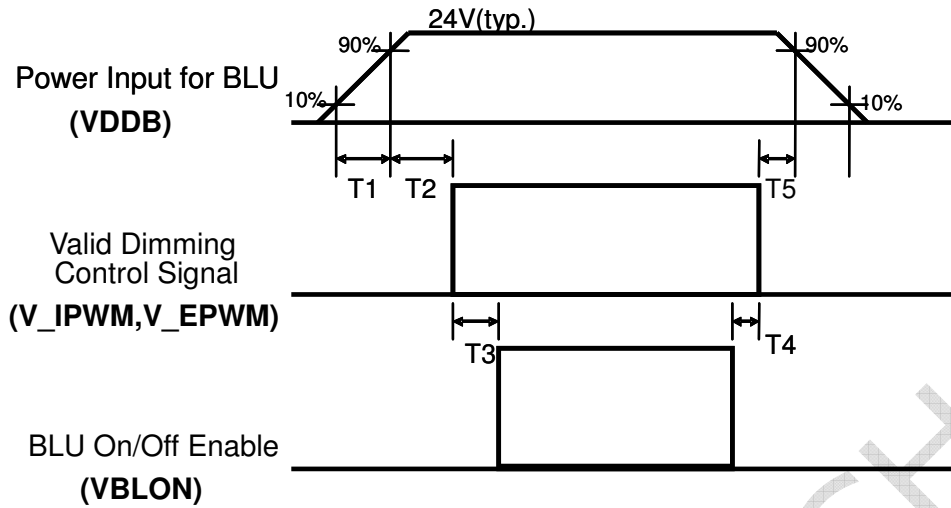


Parameter	Values			Unit
	Min.	Type.	Max.	
t1	0.4	---	30	ms
t2	0.1	---	50	ms
t3	840	---	---	ms
t4	0 ^{*1}	---	---	ms
t5	0	---	---	ms
t6	---	---	--- ^{*2}	ms
t7	500	---	---	ms
t8	10 ^{*3}	---	50	ms
t9	0	---	---	ms
t10	840	---	---	ms
t11	150	---	---	ms

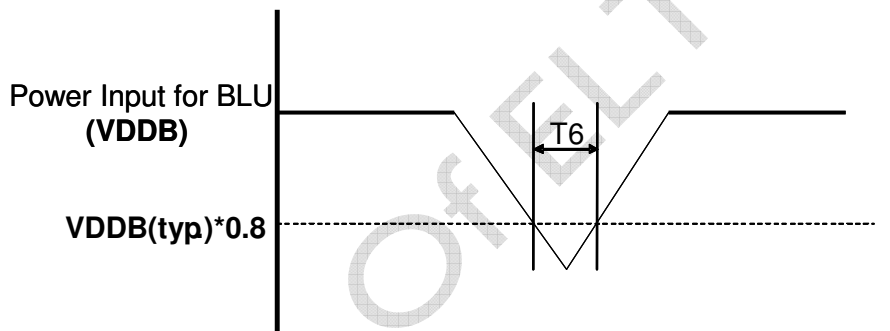
Note:

- (1) t4=0 : concern for residual pattern before BLU turn off.
- (2) t6 : voltage of VDD must decay smoothly after power-off. (customer system decide this value)
- (3) When CMOS Interface signal is N.C. (no connection), opened in Transmitted end, t8 timing spec can be negligible.

◆ Power Sequence of Backlight



Dip condition



Parameter	Value			Units
	Min	Typ	Max	
T1	20	-	-	ms ^{*1}
T2	250	-	-	ms
T3	200	-	-	ms
T4	0	-	-	ms
T5	0	-	-	ms
T6	-	-	1000	ms ^{*2}

Note:1. T1 describes rising time of 0V to 24V and this parameter does not applied at restarting time. Even though T1 is over the specified value, there is no problem if I2t spec of fuse is satisfied.

Note:2. T6 describes VDDB dip condition and VDDB couldn't lower than 10% VDDB.

3.7 Backlight Specification

The backlight unit contains 144 pcs LED.

3.7.1 Electrical specification

	Item	Symbol	Condition	Spec			Unit	Note	
				Min	Typ	Max			
1	Input Voltage	V _{DDB}	-	22.8	24	25.2	VDC	-	
2	Input Current	I _{DDB}	V _{DDB} =24V		5.03	5.31	ADC	1	
3	Input Power	P _{DDB}	V _{DDB} =24V		120.8	127.5	W	1	
4	Inrush Current	I _{RUSH}	V _{DDB} =24V			10	A _{peak}	2	
5	Control signal voltage	V _{Signal}	Hi	V _{DDB} =24V	2	-	5.5	VDC	-
			Low		0	-	0.8		3
6	Control signal current	I _{Signal}	V _{DDB} =24V	-	-	1.5	mA	-	
7	External PWM Duty ratio (input duty ratio)	D_EPWM	V _{DDB} =24V	0	-	100	%	4	
8	External PWM Frequency	F_EPWM	V _{DDB} =24V	90	180	240	Hz	4	
9	DET status signal	DET	Hi	V _{DDB} =24V	Open Collector			VDC	5
			Lo		0	-	0.8	VDC	5
10	Input Impedance	R _{in}	V _{DDB} =24V	300			Kohm	-	

Note 1: Dimming ratio= 100%, (Ta=25±5°C, Turn on for 45minutes)

Note 2: MAX input current while DB turn on, measurement condition V_{DDB} rising time=20ms(V_{DDB}: 10%~90%)

Note 3: When BLU off (V_{DDB} = 24V , V_{BLON} = 0V) , I_{DDB} (max) = 0.1A

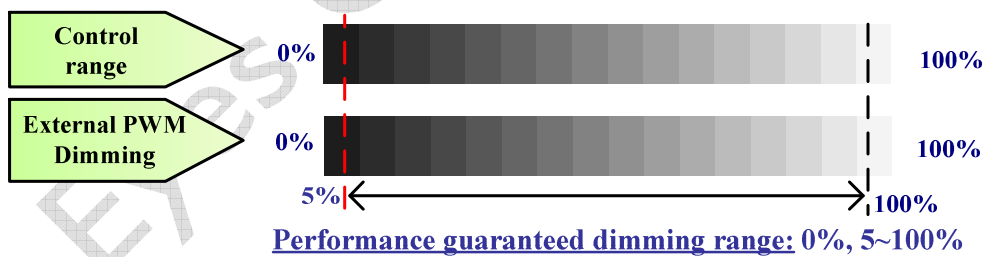
Note 4: Less than 5% dimming control is functional well and no backlight shutdown happened

Note 5: Normal: 0~0.8V ; Abnormal : Open collector

3.7.2 Input Pin Assignment

LED driver board connector: CI0114M1HR0-NH (Cvilux)

Pin	Symbol	Description
1	VDDDB	Operating Voltage Supply, +24V DC regulated
2	VDDDB	Operating Voltage Supply, +24V DC regulated
3	VDDDB	Operating Voltage Supply, +24V DC regulated
4	VDDDB	Operating Voltage Supply, +24V DC regulated
5	VDDDB	Operating Voltage Supply, +24V DC regulated
6	BLGND	Ground and Current Return
7	BLGND	Ground and Current Return
8	BLGND	Ground and Current Return
9	BLGND	Ground and Current Return
10	BLGND	Ground and Current Return
11	DET	BLU status detection: Normal : 0~0.8V ; Abnormal : Open collector (Recommend Pull high R > 10K, VDD = 3.3V)
12	VBLON	BLU On-Off control: BL On : High/Open (2V~5.5V); BL off : Low (0~0.8V/GND)
13	N.C.	N.C.
14	PDIM	External PWM (0%~100% Duty, open for 100%)



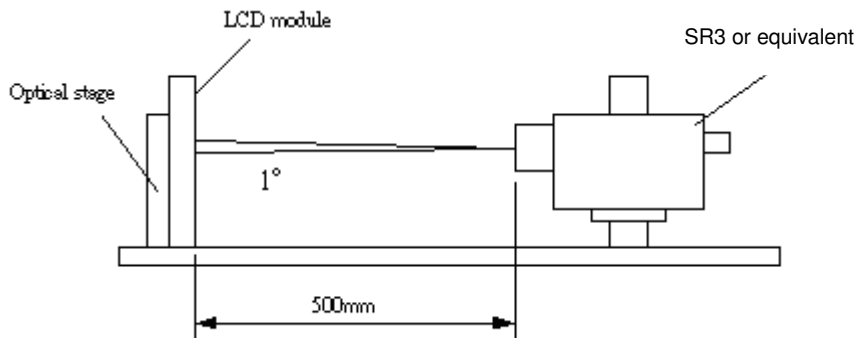
(Note*) IF External PWM function includes 5% dimming ratio. Judge condition as below:

- (1) Backlight module must be lighted ON normally.
- (2) All protection function must work normally.
- (3) Uniformity and flicker could NOT be guaranteed

4. Optical Specification

Optical characteristics are determined after the unit has been 'ON' and stable for approximately 45 minutes in a dark environment at 25°C while panel is placed in the default position. The default position is T-con side as the top side of panel. The value specified is at an approximate distance 50cm from the LCD surface at a viewing angle of φ and θ equal to 0°.

Fig.1 presents additional information concerning the measurement equipment and method.



Parameter	Symbol	Values			Unit	Notes
		Min.	Typ.	Max		
Contrast Ratio	CR	3200	4000	--		1
Surface Luminance (White)	L_{WH}	400	500	--	cd/m ²	2
Luminance Variation	$\delta_{WHITE(9P)}$	--	--	1.33		3
Response Time (G to G)	T_{γ}	--	8	--	ms	4
Color Gamut	NTSC		72		%	
Color Coordinates						
Red	R_x	Typ.-0.03	0.640	Typ.+0.03		
	R_y		0.330			
Green	G_x		0.300			
	G_y		0.605			
Blue	B_x		0.150			
	B_y		0.050			
White	W_x		0.280			
	W_y		0.290			
Viewing Angle						
x axis, right($\varphi=0^\circ$)	θ_r	--	89	--	degree	5
x axis, left($\varphi=180^\circ$)	θ_l	--	89	--	degree	
y axis, up($\varphi=90^\circ$)	θ_u	--	89	--	degree	
y axis, down ($\varphi=270^\circ$)	θ_d	--	89	--	degree	

Note:

1. Contrast Ratio (CR) is defined mathematically as:

$$\text{Contrast Ratio} = \frac{\text{Surface Luminance of } L_{on5}}{\text{Surface Luminance of } L_{off5}}$$

2. Surface luminance is luminance value at point 5 across the LCD surface 50cm from the surface with all pixels displaying white. From more information see FIG 2. When lamp current $I_H = 11\text{mA}$. $L_{WH} = L_{on5}$ where L_{on5} is the luminance with all pixels displaying white at center 5 location.

3. The variation in surface luminance, δ_{WHITE} is defined (center of Screen) as:

$$\delta_{WHITE(9P)} = \frac{\text{Maximum}(L_{on1}, L_{on2}, \dots, L_{on9})}{\text{Minimum}(L_{on1}, L_{on2}, \dots, L_{on9})}$$

4. Response time T_γ is the average time required for display transition by switching the input signal for five luminance ratio (0%, 25%, 50%, 75%, 100% brightness matrix) and is based on $F_v = 60\text{Hz}$ to optimize.

T_γ is determined by 10% to 90% brightness difference of rising or falling period. (As illustrated)

Measured Response Time		Target				
		0%	25%	50%	75%	100%
Start	0%		0% to 25%	0% to 50%	0% to 75%	0% to 100%
	25%	25% to 0%		25% to 50%	25% to 75%	25% to 100%
	50%	50% to 0%	50% to 25%		50% to 75%	50% to 100%
	75%	75% to 0%	75% to 25%	75% to 50%		75% to 100%
	100%	100% to 0%	100% to 25%	100% to 50%	100% to 75%	

5. Viewing angle is the angle at which the contrast ratio is greater than 10. The angles are determined for the horizontal or x axis and the vertical or y axis with respect to the z axis which is normal to the LCD surface. For more information see FIG4.

FIG. 2 Luminance

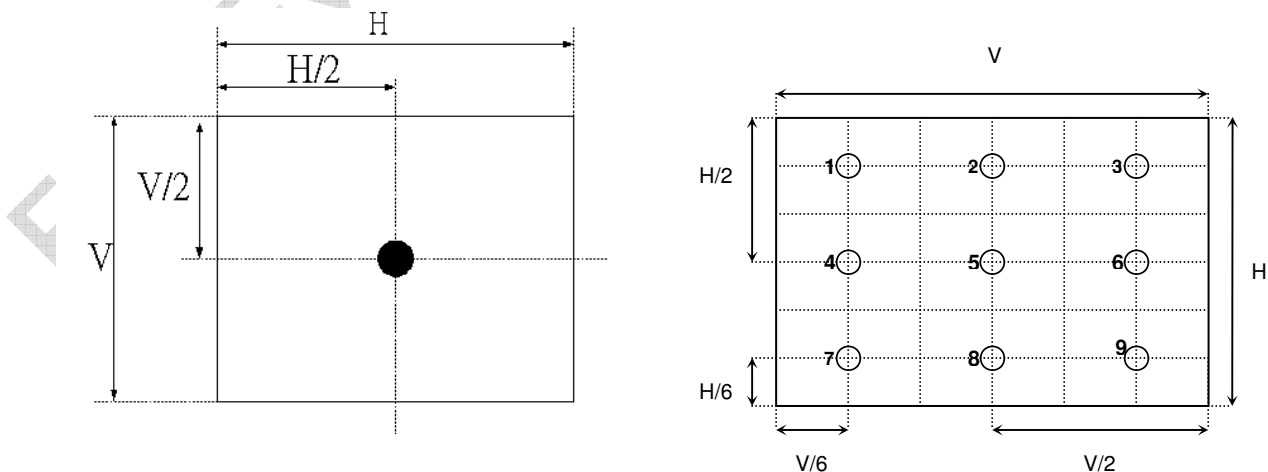


FIG.3 Response Time

The response time is defined as the following figure and shall be measured by switching the input signal for “any level of gray(bright) “ and “any level of gray(dark)”.

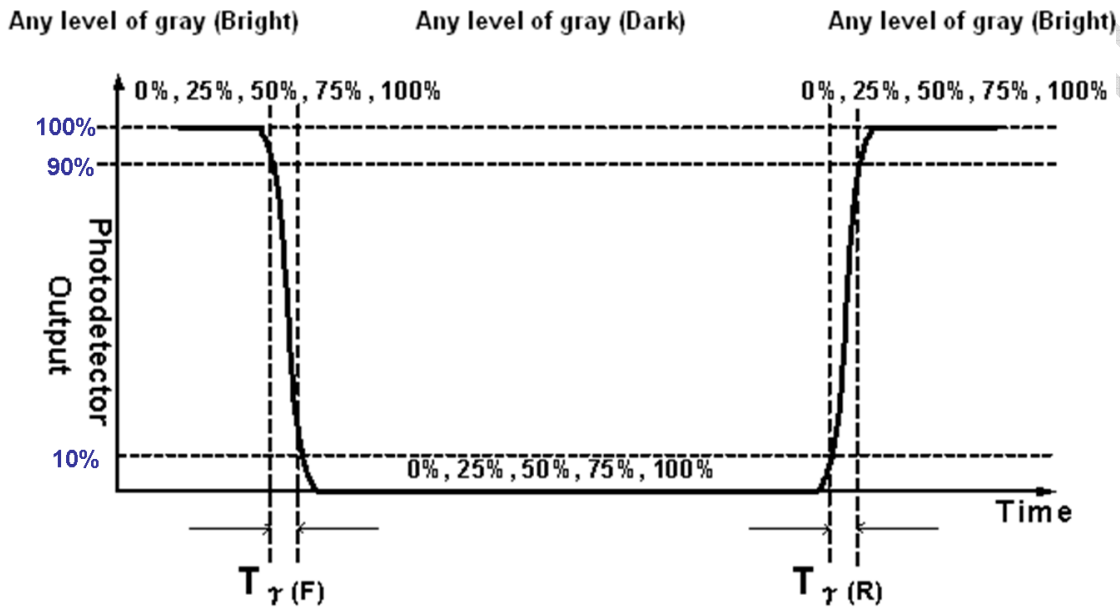
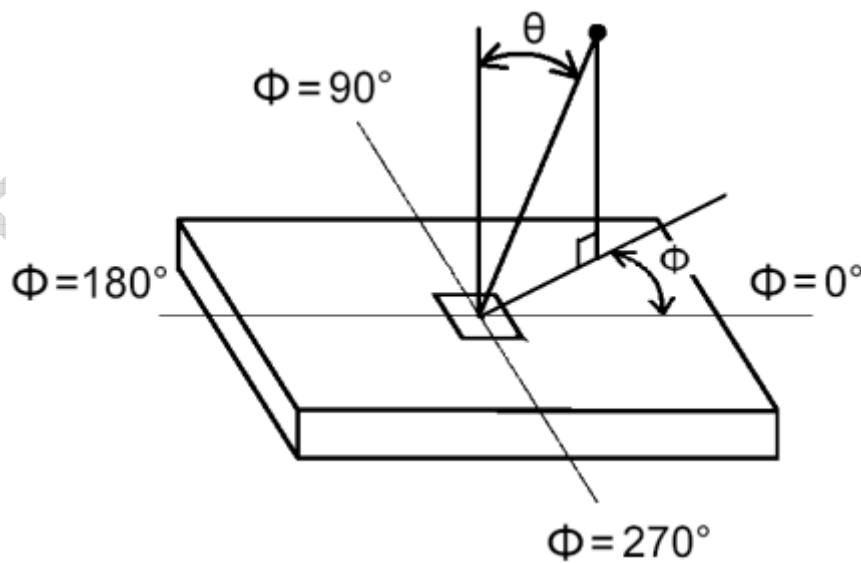


FIG.4 Viewing Angle



5. Mechanical Characteristics

The contents provide general mechanical characteristics for the model P550HVN05.0. In addition the figures in the next page are detailed mechanical drawing of the LCD.

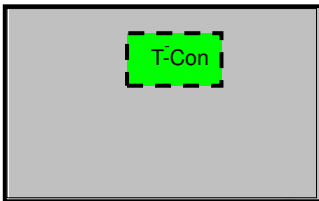
Outline Dimension	Horizontal (typ.)	1219.0 mm
	Vertical (typ.)	689.8mm
	Depth (typ.)	37.5 mm
Bezel Opening Area	Horizontal (typ.)	1209.8 mm
	Vertical (typ.)	680.6 mm
Active Display Area	Horizontal	1209.6 mm
	Vertical	680.4 mm
Weight	18000g	

5.1 Placement suggestions:

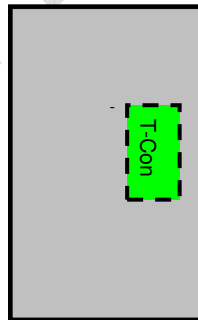
The Suggestion placement is as following:

1. Landscape mode: The default placement is T-Con Side as the top side.
2. Portrait mode: The default placement is T-Con side has to be placed in the right side via viewing from the front.

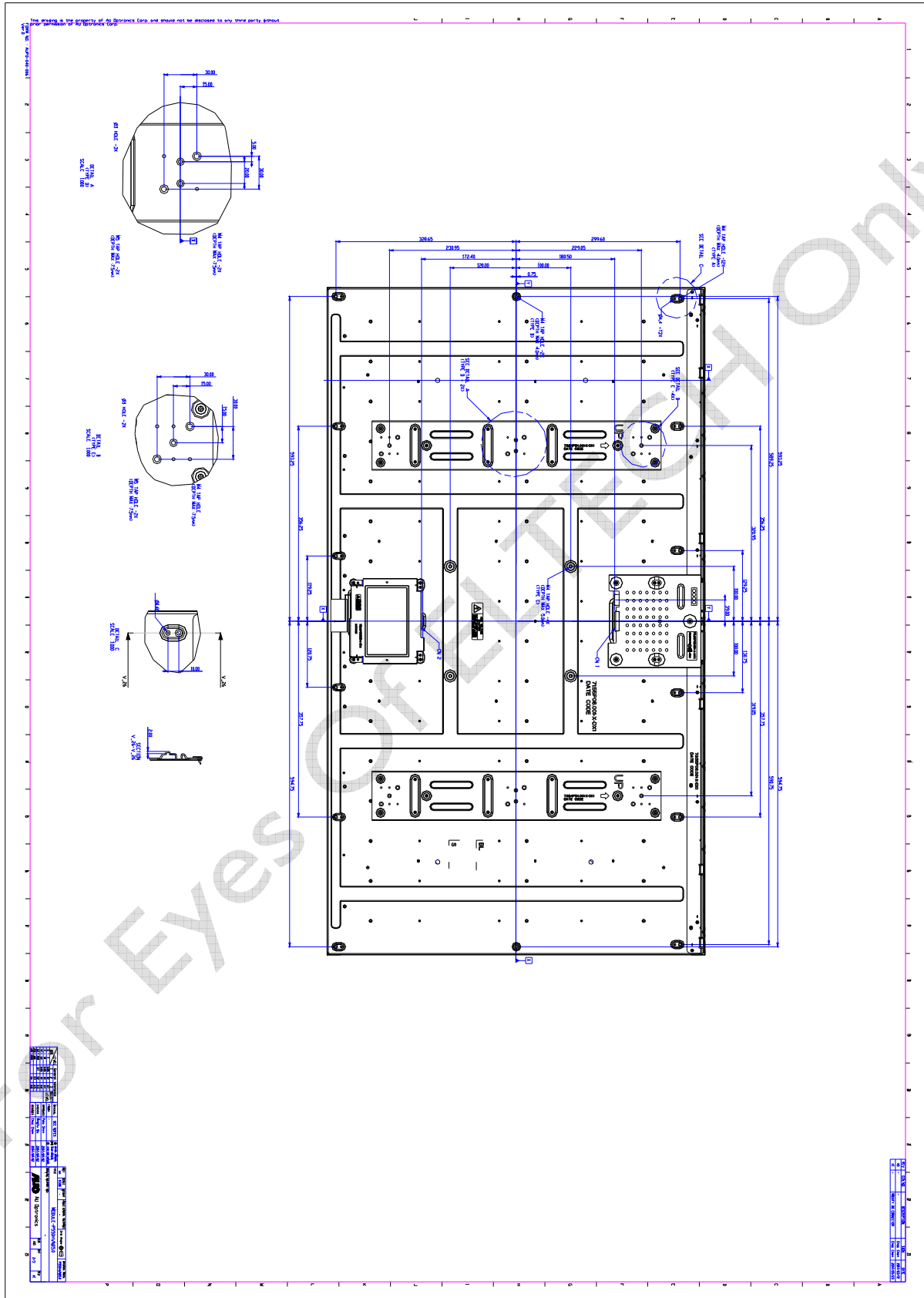
Landscape (Front view)



Portrait (Front view)



Back View



6. Reliability Test Items

	Test Item	Q'ty	Condition
1	High temperature storage test	3	60°C , 500hrs
2	Low temperature storage test	3	-20°C , 500hrs
3	High temperature operation test	3	50°C , 500hrs
4	Low temperature operation test	3	-10°C , 500hrs
5	Vibration test (non-operation)	3	Wave form: random Vibration level: 0.5G RMS Bandwidth: 10-300Hz, Duration: X, Y, Z 30min per axes X,Y,Z : Vertical.
6	Shock test (non-operation)	3	Shock level: 10G Waveform: half sine wave, 11ms Direction: ±X, ±Y, ±Z, One time each direction
7	Vibration test (With carton)	1 (PKG)	Random wave (1.05G RMS, 10-200Hz) 20mins per each X,Y,Z axes
8	Drop test (With carton)	1 (PKG)	Drop Height: 25.4 cm, Surround four flats and bottom flat twice. (ASTMD4169-I)

7. International Standard

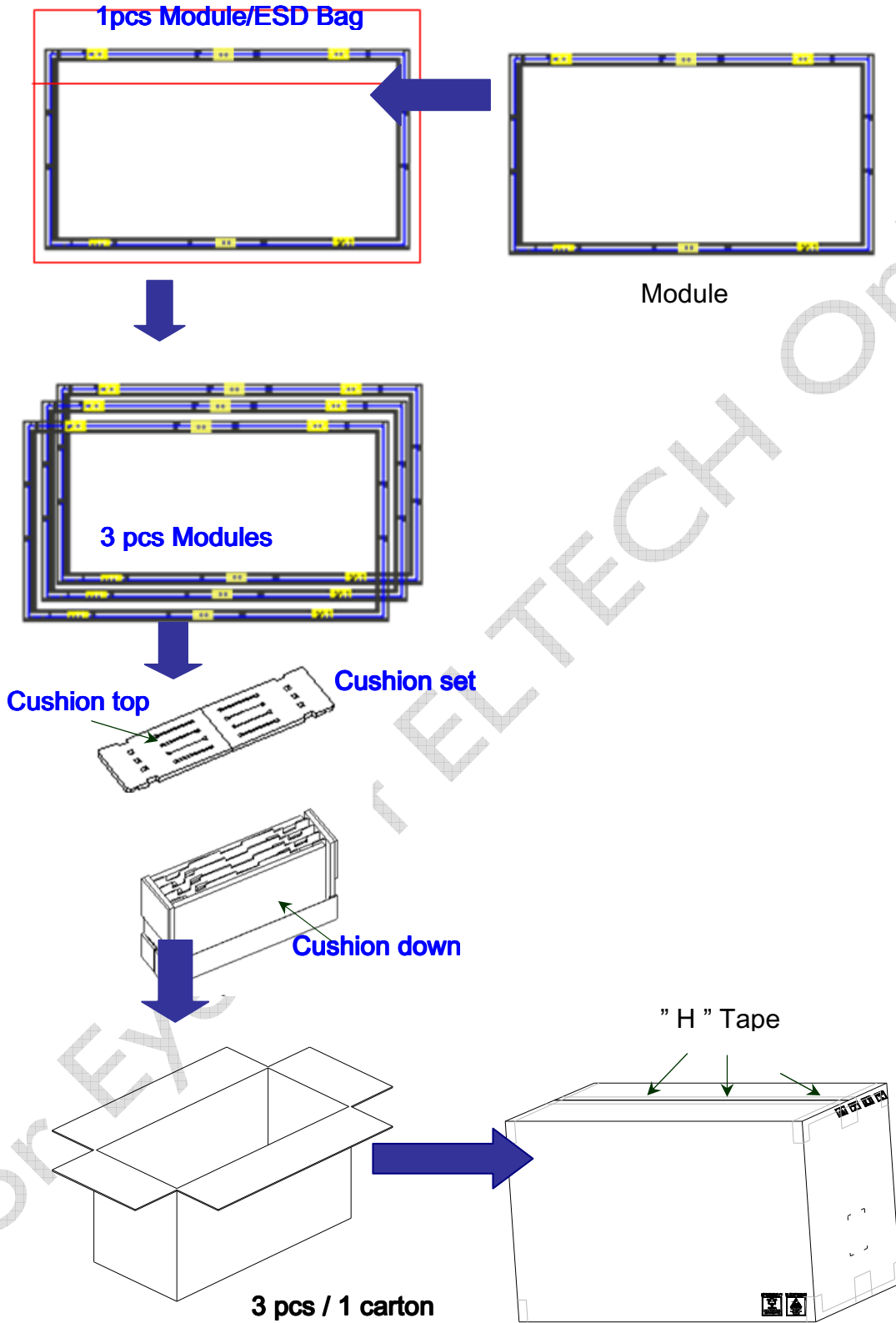
7.1 Safety

- (1) UL 60950-1, UL 60065; Standard for Safety of Information Technology Equipment Including electrical Business Equipment.
- (2) IEC 60950-1 : 2001, IEC 60065:2001 ; Standard for Safety of International Electro technical Commission
- (3) EN 60950 : 2001+A11, EN 60065:2002+A1:2006; European Committee for Electro technical Standardization (CENELEC), EUROPEAN STANDARD for Safety of Information Technology Equipment Including Electrical Business Equipment

7.2 EMC

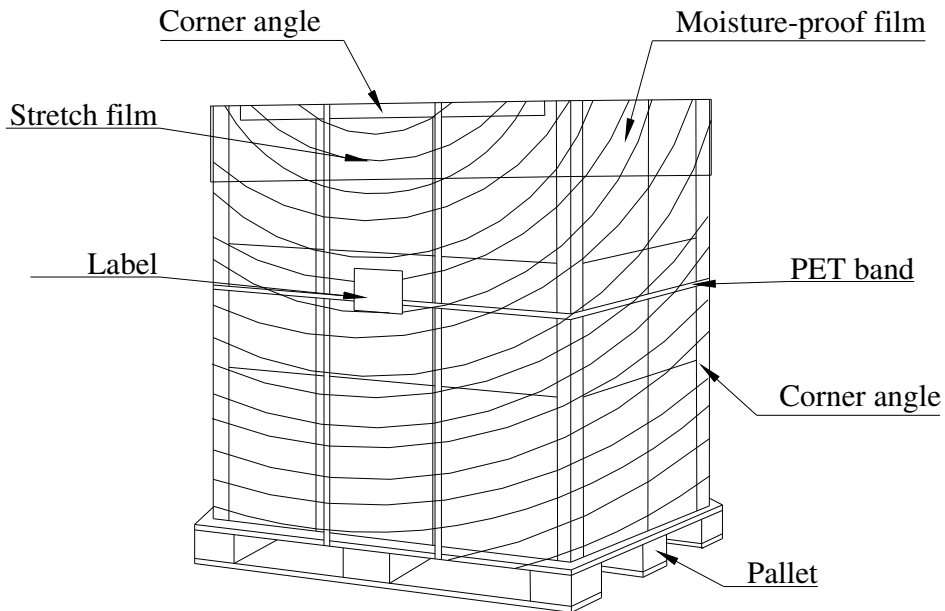
- (1) ANSI C63.4 “Methods of Measurement of Radio-Noise Emissions from Low-Voltage Electrical and Electrical Equipment in the Range of 9kHz to 40GHz. “American National standards Institute(ANSI), 1992
- (2) C.I.S.P.R “Limits and Methods of Measurement of Radio Interface Characteristics of Information Technology Equipment.” International Special committee on Radio Interference.
- (3) EN 55022 “Limits and Methods of Measurement of Radio Interface Characteristics of Information Technology Equipment.” European Committee for Electro technical Standardization. (CENELEC), 1998

8-2 PACKING METHODS:



8-3 Pallet and Shipment Information

	Item	Specification			Packing Remark
		Qty.	Dimension	Weight (kg)	
1	Packing Box	3pcs/box	1355(L)mm*375(W)mm*800(H)mm	63.2	
2	Pallet	1	1390(L)mm*1150(W)mm*138(H)mm	18	
3	Boxes per Pallet	3 boxes/Pallet (By Air) ; 3 boxes /Pallet (By Sea)			
4	Panels per Pallet	9pcs/pallet(By Air) ; 9pcs/Pallet (By Sea)			
5	Pallet after packing	9(by Air)	1390(L)mm*1150(W)mm*938(H)mm (by Air)	207.6 (by Air)	
		18(by Sea)	1390(L)mm*1150(W)mm*1876(H)mm (by Sea)	415.2 (by Sea)	40ft DC



9. Precautions

Please pay attention to the followings when you use this TFT LCD module.

9.1 Mounting Precautions

- (1) You must mount a module using holes arranged in four corners or four sides.
- (2) You should consider the mounting structure so that uneven force (ex. twisted stress) is not applied to module. And the case on which a module is mounted should have sufficient strength so that external force is not transmitted directly to the module.
- (3) Please attach the surface transparent protective plate to the surface in order to protect the polarizer. Transparent protective plate should have sufficient strength in order to resist external force.
- (4) You should adopt radiation structure to satisfy the temperature specification.
- (5) Acetic acid type and chlorine type materials for the cover case are not desirable because the former generates corrosive gas of attacking the polarizer at high temperature and the latter cause circuit broken by electro-chemical reaction.
- (6) Do not touch, push or rub the exposed polarizer with glass, tweezers or anything harder than HB pencil lead. And please do not rub with dust clothes with chemical treatment. Do not touch the surface of polarizer for bare hand or greasy cloth. (Some cosmetics are detrimental to the polarizer.)
- (7) When the surface becomes dusty, please wipe gently with absorbent cotton or other soft materials like chamois soaks with petroleum benzene. Normal-hexane is recommended for cleaning the adhesives used to attach front/ rear polarizer. Do not use acetone, toluene and alcohol because they cause chemical damage to the polarizer.
- (8) Wipe off saliva or water drops as soon as possible. Their long time contact with polarizer causes deformations and color fading.
- (9) Do not open the case because inside circuits do not have sufficient strength.

9.2 Operating Precautions

- (1) The spike noise causes the mis-operation of circuits. It should be lower than following voltage:
 $V = \pm 200\text{mV}$ (Over and under shoot voltage)
- (2) Response time depends on the temperature. (In lower temperature, it becomes longer..)
- (3) Brightness depends on the temperature. (In lower temperature, it may become lower.) And in lower temperature, response time (required time that brightness is stable after turned on) becomes longer.
- (4) Be careful for condensation at sudden temperature change. Condensation makes damage to polarizer or electrical contacted parts. And after fading condensation, smear or spot will occur.
- (5) When fixed patterns are displayed for a long time, remnant image is likely to occur.
- (6) Module has high frequency circuits. Sufficient suppression to the electromagnetic interference shall be done by system manufacturers. Grounding and shielding methods may be important to minimize the interface.

9.3 Operating Condition for Public Information Display

The device listed in the product specification is designed and manufactured for PID (Public Information Display) application. To optimize module's lifetime and function, below operating usages are required.

- (1) Normal operating condition
 1. Operating temperature: 5~40°C
 2. Operating humidity: 10~90%
 3. Display pattern: dynamic pattern (Real display).
Note) Long-term static display would cause image sticking.
- (2) Operation usage to protect against abnormal display due to long-term static display.
 - (1) Suitable operating time: under **20** hours a day.
 - (2) Liquid Crystal refresh time is required. Cycling display between 5 minutes' information (static) display and 10 seconds' moving image.
 - (3) Periodically change background and character (image) color.
 - (4) Avoid combination of background and character with large different luminance.
- (3) Periodically adopt one of the following actions after long time display.
 - A. Running the screen saver (motion picture or black pattern)
 - B. Power off the system for a while
- (4) LCD system is required to place in well-ventilated environment. Adapting active cooling system is highly recommended.
- (5) Product reliability and functions are only guaranteed when the product is used under right operation usages. If product will be used in extreme conditions, such as high temperature/humidity, display stationary patterns, or long operation time etc..., it is strongly recommended to contact AUO for filed application engineering advice. Otherwise, its reliability and function may not be guaranteed. Extreme conditions are commonly found at airports, transit stations, banks, stock market and controlling systems.

9.4 Electrostatic Discharge Control

Since a module is composed of electronic circuits, it is not strong to electrostatic discharge. Make certain that treatment persons are connected to ground through wristband etc. And don't touch interface pin directly.

9.5 Precautions for Strong Light Exposure

Strong light exposure causes degradation of polarizer and color filter.

9.6 Storage

When storing modules as spares for a long time, the following precautions are necessary.

- (1) Store them in a dark place. Do not expose the module to sunlight or fluorescent light. Keep the temperature between 5°C and 35°C at normal humidity.

- (2) The polarizer surface should not come in contact with any other object. It is recommended that they be stored in the container in which they were shipped.
- (3) Storage condition is guaranteed under packing conditions.
- (4) The phase transition of Liquid Crystal in the condition of the low or high storage temperature will be recovered when the LCD module returns to the normal condition.

9.7 Handling Precautions for Protection Film

- (1) The protection film is attached to the bezel with a small masking tape. When the protection film is peeled off, static electricity is generated between the film and polarizer. This should be peeled off slowly and carefully by people who are electrically grounded and with well ion-blown equipment or in such a condition, etc.
- (2) When the module with protection film attached is stored for a long time, sometimes there remains a very small amount of glue still on the bezel after the protection film is peeled off.
- (3) You can remove the glue easily. When the glue remains on the bezel or its vestige is recognized, please wipe them off with absorbent cotton waste or other soft material like chamois soaked with normal-hexane.