PRELIMINARY

NLT Technologies, Ltd.

TFT COLOR LCD MODULE

NL204153AC21-25

54cm (21.3 Type)
QXGA
LVDS interface (4 ports)

PRELIMINARY DATA SHEET

DOD-PP-1871 (2nd edition)

This PRELIMINARY DATA SHEET is updated document from DOD-PP-1803(1).

All information is subject to change without notice. Please confirm the sales representative before starting to design your system.

INTRODUCTION

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Some electronic products would fail or malfunction at a certain rate. In spite of every effort to enhance reliability of products by NLT, the possibility of failures and malfunction might not be avoided entirely. To prevent the risks of damage to death, human bodily injury or other property arising out thereof or in connection therewith, each customer is required to take sufficient measures in its safety designs and plans including, but not limited to, redundant system, fire-containment and anti-failure.

The products are classified into three grades: **"Standard"**, **"Special"**, and **"Specific"**.
Each quality grade is designed for applications described below. Any customer who intends to use a product for application other than that of Standard is required to contact an NLT sales representative in advance.

The **Standard:** Applications as any failure, malfunction or error of the products are free from any damage to death, human bodily injury or other property (Products Safety Issue) and not related the safety of the public (Social Issues), like general electric devices.
Examples: Office equipment, audio and visual equipment, communication equipment, test and measurement equipment, personal electronic equipment, home electronic appliances, car navigation system (with no vehicle control functions), seat entertainment monitor for vehicles and airplanes, fish finder (except marine radar integrated type), PDA, etc.

The **Special:** Applications as any failure, malfunction or error of the products might directly cause any damage to death, human bodily injury or other property (Products Safety Issue) and the safety of the public (Social Issues) and required high level reliability by conventional wisdom.
Examples: Vehicle/train/ship control system, traffic signals system, traffic information control system, air traffic control system, surgery/operation equipment monitor, disaster/crime prevention system, etc.

The **Specific:** Applications as any failure, malfunction or error of the products might severe cause any damage to death, human bodily injury or other property (Products Safety Issue) and the safety of the public (Social Issues) and developed, designed and manufactured in accordance with the standards or quality assurance program designated by the customer who requires extremely high level reliability and quality.
Examples: Aerospace system (except seat entertainment monitor), nuclear control system, life support system, etc.

The quality grade of this product is the **"Standard"** unless otherwise specified in this document.

CONTENTS

1. OUTLINE

1.1 STRUCTURE AND PRINCIPLE

Color LCD module NL204153AC21-25 is composed of the amorphous silicon thin film transistor liquid crystal display (a-Si TFT LCD) panel structure with driver LSIs for driving the TFT (Thin Film Transistor) array and a backlight.

The a-Si TFT LCD panel structure is injected liquid crystal material into a narrow gap between the TFT array glass substrate and a color-filter glass substrate.

Color data signals from a host system (e.g. signal generator, etc.) are modulated into best form for active matrix system by a signal processing board, and sent to the driver LSIs which drive the individual TFT arrays.

The TFT array as an electro-optical switch regulates the amount of transmitted light from the backlight assembly, when it is controlled by data signals. Color images are created by regulating the amount of transmitted light through the TFT array of red, green and blue dots.

1.2 APPLICATION

- Color monitor system

1.3 FEATURES

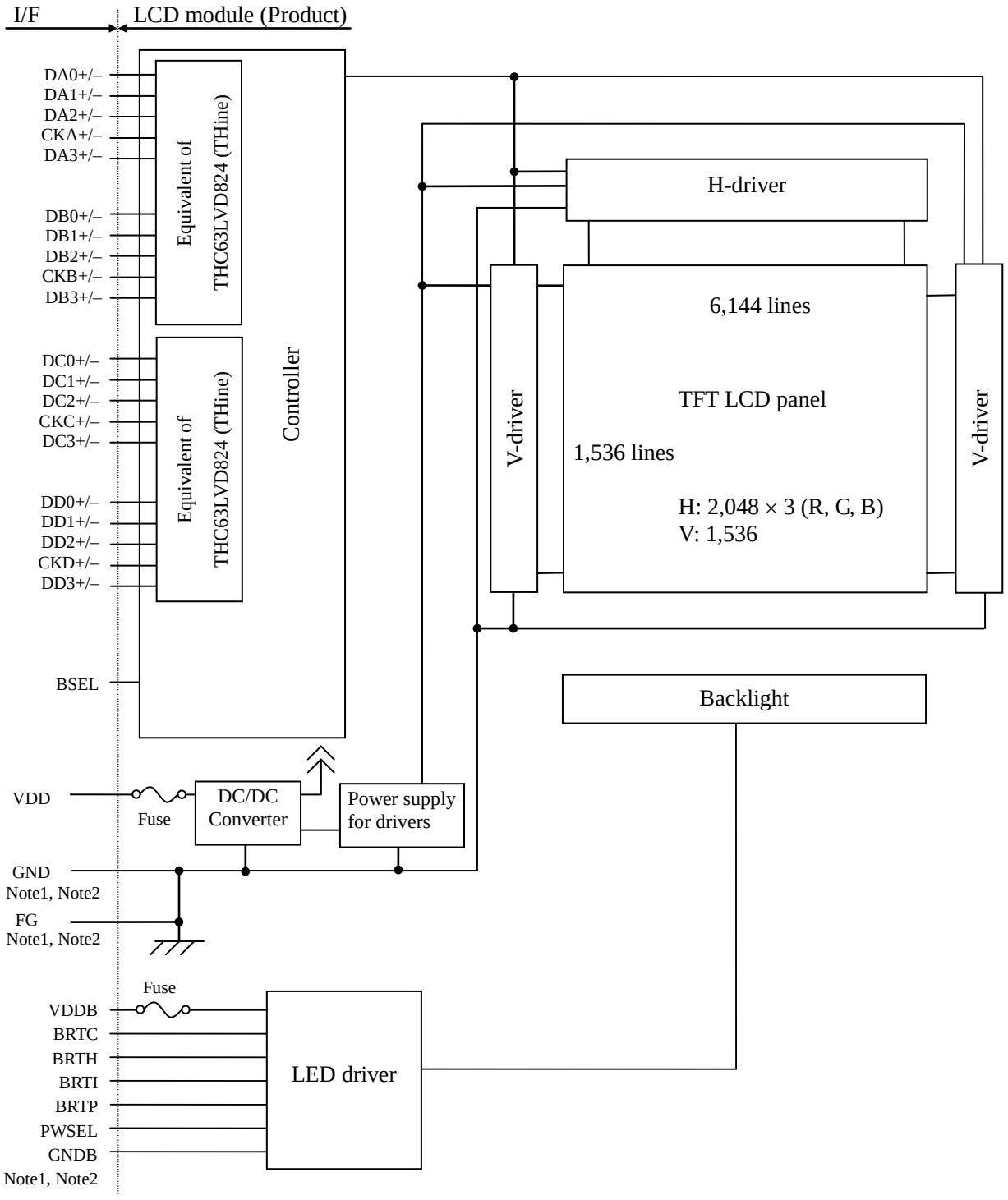
- Ultra-wide viewing angle (Super Fine TFT (SFT))
- Wide color gamut
- High luminance
- High contrast
- Low reflection
- High resolution QXGA (2,048 × 1,536 pixels, 1 pixel consists of 3 sub-pixels)
- 256 gray scale in each R, G, B sub-pixel (8-bit), 16,777,216 colors
- LVDS interface
- Selectable LVDS data input map
- Small foot print
- Long life LED backlight with an LED driver

2. GENERAL SPECIFICATIONS

Display area	433.152 (H) × 324.864 (V) mm	
Diagonal size of display	54cm (21.3 inches)	
Drive system	a-Si TFT active matrix	
Display color	16,777,216 colors	
Pixel	2,048 (H) × 1,536 (V) pixels (1 pixel consists of 3 sub-pixels (RGB).)	
Pixel arrangement	RGB (Red dot, Green dot, Blue dot) vertical stripe	
Sub-pixel pitch	0.0705 (H) × 0.2115 (V) mm	
Pixel pitch	0.2115 (H) × 0.2115 (V) mm	
Module size	457.0 (W) × 350.0 (H) × 21.5 (D) mm (typ.)	
Weight	2,700 g (typ.)	2
Contrast ratio	1,400:1 (typ.)	2
Viewing angle	*At the contrast ratio ≥ 10:1* • Horizontal: Right side 88° (typ.), Left side 88° (typ.) • Vertical: Up side 88° (typ.), Down side 88° (typ.)	
Designed viewing direction	Viewing angle with optimum grayscale (γ≒DICOM): Normal axis (perpendicular) Note1	
Polarizer surface	Antiglare	
Polarizer pencil-hardness	2H (min.) [by JIS K5600]	
Color gamut	*At LCD panel center* 72 % (typ.) [against NTSC color space]	
Response time	*Ton+Toff (10%←→90%)* (40) ms (typ.)	
Luminance	*At the maximum luminance control* 800 cd/m^2 (typ.)	2
Signal system	4 ports LVDS interface. (Characteristics of AC receiver THC63LVD824×2pcs, THine Electronics, Inc. or equivalent) [RGB 8-bit signals, Data enable signal (DE), Dot clock (CLK)]	
Power supply voltage	LCD panel signal processing board: 12.0V LED driver: 12.0V/ 18.0V	2
Backlight	LED backlight type with LED driver board	
Power consumption	*At checkered flag pattern, the maximum luminance control* (58.2)W (typ.)	2

Note1: When the product luminance is 450cd/m^2, the gamma characteristic is designed to γ≒DICOM.

3. BLOCK DIAGRAM



Note1: Relations between GND (Signal ground), FG (Frame ground) and GNDB (LED driver board ground) in the LCD module are as follows.

GND- FG	Connected
GND- GNDB	Not connected
FG- GNDB	Not connected

Note2: GND, FG and GNDB must be connected to customer equipment's ground, and it is recommended that these grounds be connected together in customer equipment.

Note3: Each pair of the LVDS signal has a 100Ω terminating resistance between D+ and D-.

4. DETAILED SPECIFICATIONS

4.1 MECHANICAL SPECIFICATIONS

Parameter	Specification		Unit
Module size	457.0 ±0.5 (W) × 350.0 ± 0.5 (H) × 21.5 (typ., D) 23.0 (max., D)	Note1, Note2	mm
Display area	433.152 (H) × 324.864 (V)	Note2	mm
Weight	2,700 (typ.), 2,980 (max.)		g

Note1: Excluding warpage of the cover for LED driver board.
Note2: See "**8. OUTLINE DRAWINGS**".

4.2 ABSOLUTE MAXIMUM RATINGS

Parameter			Symbol	Rating	Unit	Remarks
Power supply voltage	LCD panel signal processing board		VDD	-0.3 to +14.0	V	-
	LED driver		VDDB	-0.3 to +22.5	V	
Input voltage for signals	LCD panel signal processing board Note1		Vi	-0.3 to +2.8	V	VDD= 12.0V
	LED driver board	BRTI signal	VBI	-0.3 to +1.5	V	VDDB= 12.0V
		BRTP signal	VBP	-0.3 to +5.5	V	
		BRTC signal	VBC	-0.3 to +5.5	V	
		PWSEL signal	VBS	-0.3 to +5.5	V	
Storage temperature Note6			Tst	-20 to +60	°C	-
Operating temperature Note6		Front surface	TopF	0 to +60	°C	Note2
		Rear surface	TopR	0 to +60	°C	Note3
Relative humidity Note4, Note6			RH	≤ 95	%	Ta ≤ 40°C
				≤ 85	%	40°C < Ta ≤ 50°C
				≤ 70	%	50°C < Ta ≤ 55°C
Absolute humidity Note4, Note6			AH	≤ 73 Note5	g/m^3	Ta > 55°C
Operating altitude			-	≤ 5,100	m	0°C ≤ Ta ≤ 55°C
Storage altitude			-	≤ 13,600	m	-20°C ≤ Ta ≤ 60°C

Note1: Display signals are DA0+/-, DA1+/-, DA2+/-, DA3+/-, CKA+/-, DB0+/-, DB1+/-, DB2+/-, DB3+/-, CKB+/-, DC0+/-, DC1+/-, DC2+/-, DC3+/-, CKC+/-, DD0+/-, DD1+/-, DD2+/-, DD3+/-, CKD+/-,BSEL.
Note2: Measured at LCD panel surface (including self-heat)
Note3: Measured at LCD module's rear shield surface (including self-heat)
Note4: No condensation
Note5: Water amount at Ta= 55°C and RH= 70%
Note6: The image quality may cause degradation in case of rapid change humidity and temperature.

4.3 ELECTRICAL CHARACTERISTICS

4.3.1 LCD panel signal processing board

(Ta= 25°C)

Parameter		Symbol	min.	typ.	max.	Unit	Remarks
Power supply voltage		VDD	10.8	12.0	13.2	V	-
Power supply current		IDD	-	(650) Note1	(980) Note2	mA	at VDD= 12.0V
Permissible ripple voltage		VRP	-	-	100	mVp-p	for VDD
Differential input threshold voltage	High	VTH	-	-	+100	mV	at VCM= 1.2V Note3, Note4
	Low	VTL	-100	-	-	mV	
Input voltage swing		VI	0	-	2.4	V	Note4
Terminating resistance		RT	-	100	-	Ω	-
Control signal input threshold voltage	High	VIH	Keep this pin open.			-	Note5
	Low	VIL	0	-	0.5	V	
Control signal input current	Low	IIL	-10	-	10	μA	

Note1: Checkered flag pattern (by EIAJ ED-2522)
Note2: Pattern for maximum current
Note3: Common mode voltage for LVDS driver
Note4: DA0+/-, DA1+/-, DA2+/-, DA3+/-, CKA+/-, DB0+/-, DB1+/-, DB2+/-, DB3+/-, CKB+/-, DC0+/-, DC1+/-, DC2+/-, DC3+/-, CKC+/-, DD0+/-, DD1+/-, DD2+/-, DD3+/-, CKD+/-
Note5: BSEL

4.3.2 LED driver

(Ta= 25°C)

Parameter			Symbol	min.	typ.	max.	Unit	Remarks	
Power supply voltage			VDDB	11.4	12.0	12.6	V	-	2
				17.1	18.0	18.9			2
Power supply current			IDDB	-	(4,200)	(5,800)	mA	VDDB= 12.0V, At the maximum luminance control	
				-	(2,800)	(3,900)		VDDB= 18.0V, At the maximum luminance control	
Input voltage for signals	BRTI signal		VBI	0.1	-	1.0	V	-	
	BRTP signal	High	VBPH	2.0	-	5.25	V		
		Low	VBPL	0	-	0.8	V		
	BRTC signal	High	VBCH	2.0	-	5.25	V		
		Low	VBCL	0	-	0.8	V		
	PWSEL signal	High	VBSH	2.0	-	5.25	V		
		Low	VBSL	0	-	0.68	V		
Input current for signals	BRTI signal		IBI	(-200)	-	(-100)	µA		
	BRTP signal	High	IBPH	-	-	(1,000)	µA		
		Low	IBPL	(-600)	-	-	µA		
	BRTC signal	High	IBCH	-	-	(1,000)	µA		
		Low	IBCL	(-300)	-	-	µA		
	PWSEL signal	High	IPSH	-	-	(1,000)	µA		
		Low	IPSL	(-600)	-	-	µA		

4.3.3 Power supply voltage ripple

This product works, even if the ripple voltage levels are beyond the permissible values as following the table, but there might be noise on the display image.

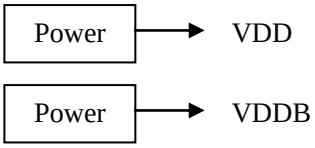
Power supply voltage		Ripple voltage Note1 (Measure at input terminal of power supply)	Unit
VDD	12.0V	≤ 100	mVp-p
VDDB	12.0V	≤ 200	mVp-p
	18.0V	≤ 200	

2

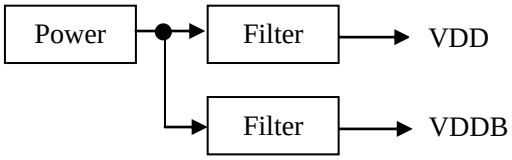
Note1: The permissible ripple voltage includes spike noise.

Example of the power supply connection

a) Separate the power supply



b) Put in the filter



4.3.4 Fuse

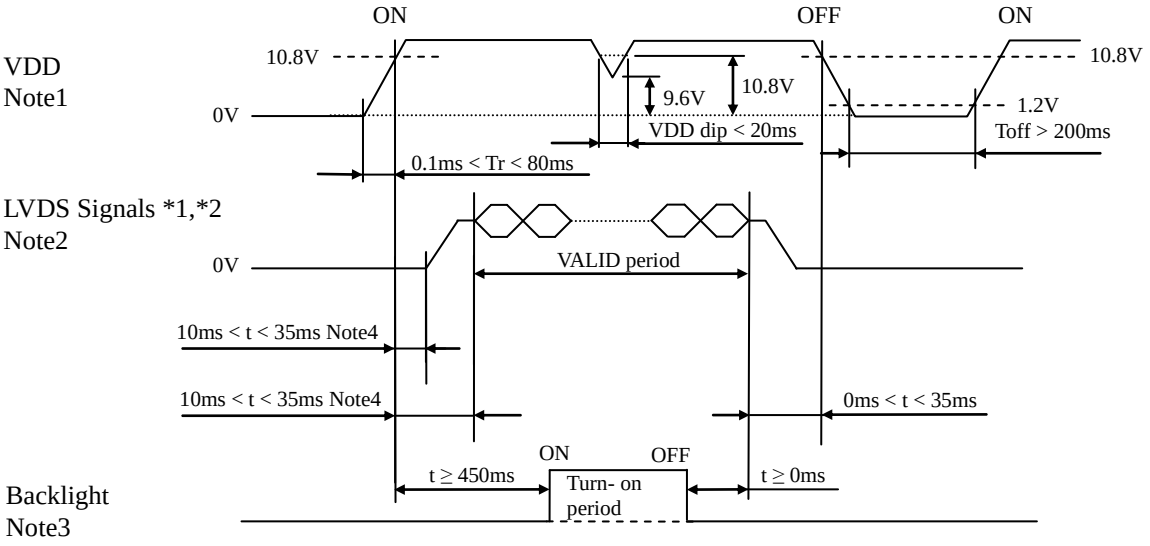
Parameter	Fuse		Rating	Fusing current	Remarks
	Type	Supplier			
VDD	FCC16202AB	KAMAYA ELECTRIC Co., Ltd.	2.0A 32V	4.0A, 5 seconds maximum	Note1
VDDB	CCF1N10	KOA Corporation	10A 60V	20 A, 1 seconds maximum	

2

Note1: The power supply capacity should be more than the fusing current. If it is less than the fusing current, the fuse may not blow in a short time, and then nasty smell, smoke and so on may occur.

4.4 POWER SUPPLY VOLTAGE SEQUENCE

4.4.1 LCD panel signal processing board



*1: DA0+/-, DA1+/-, DA2+/-, DA3+/-, CKA+/-, DB0+/-, DB1+/-, DB2+/-, DB3+/-, CKB+/-, DC0+/-, DC1+/-, DC2+/-, DC3+/-, CKC+/-, DD0+/-, DD1+/-, DD2+/-, DD3+/-, CKD+/-

*2: LVDS signals should be measured at the terminal of 100 Ω resistance.

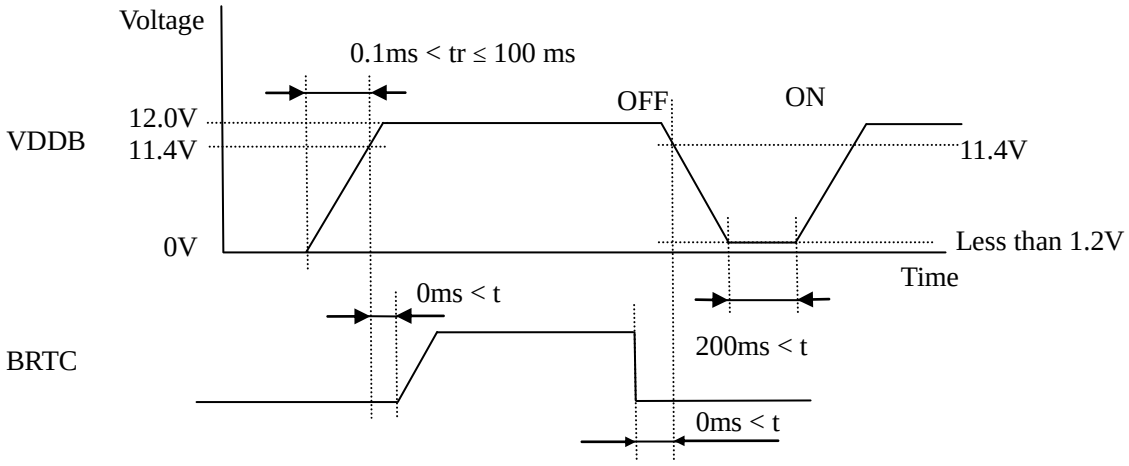
Note1: If there is a voltage variation (voltage drop) at the rising edge of VDD below 10.8V, there is a possibility that a product does not work due to a protection circuit.

Note2: LVDS signals must be set to Low or High-impedance, except the VALID period (See above sequence diagram), in order to avoid the circuitry damage.
If some of signals are cut while this product is working, even if the signal input to it once again, it might not work normally. If a customer stops the display and function signals, VDD also must be shut down.

Note3: The backlight should be turned on within the turn-on period, in order to avoid unstable data display.

Note4: After turning VDD on, terminal voltages on LVDS input terminals (*1) will rise. This is caused by initial operation of the product.

4.4.2 LED driver



Note1: If tr is more than 100ms, the backlight will be turned off by a protection circuit for LED driver board.
Note2: When VDDB is 0V or BRTC is Low, PWSEL must be set to Low or Open.

4.5 CONNECTIONS AND FUNCTIONS FOR INTERFACE PINS

4.5.1 LCD panel signal processing board

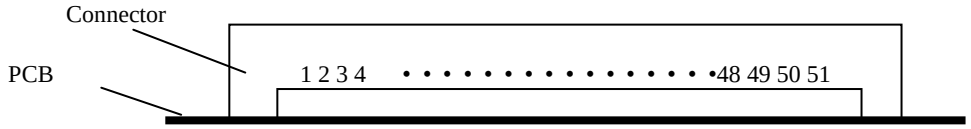
CN1 socket (LCD module side): FI-RE51S-HF (Japan Aviation Electronics Industry Limited (JAE))
Adaptable plug: FI-RE51HL (Japan Aviation Electronics Industry Limited (JAE))

Pin No.	Symbol	Signal	Remarks
1	GND	Ground	Note1
2	GND	Ground	
3	GND	Ground	
4	DA0-	Pixel data A0	LVDS differential data input Note2
5	DA0+		
6	GND	Ground	Note1
7	DA1-	Pixel data A1	LVDS differential data input Note2
8	DA1+		
9	GND	Ground	Note1
10	DA2-	Pixel data A2	LVDS differential data input Note2
11	DA2+		
12	GND	Ground	Note1
13	CKA-	Pixel clock A	LVDS differential data input Note2
14	CKA+		
15	GND	Ground	Note1
16	DA3-	Pixel data A3	LVDS differential data input Note2
17	DA3+		
18	GND	Ground	Note1
19	GND	-	Keep this pin Open.
20	GND		
21	GND	Ground	Note1
22	DB0-	Pixel data B0	LVDS differential data input Note2
23	DB0+		
24	GND	Ground	Note1
25	DB1-	Pixel data B1	LVDS differential data input Note2
26	DB1+		
27	GND	Ground	Note1
28	DB2-	Pixel data B2	LVDS differential data input Note2
29	DB2+		
30	GND	Ground	Note1
31	CKB-	Pixel clock B	LVDS differential data input Note2
32	CKB+		
33	GND	Ground	Note1
34	DB3-	Pixel data B3	LVDS differential data input Note2
35	DB3+		
36	GND	Ground	Note1
37	GND	-	Keep this pin Open.
38	GND		
39	GND	Ground	Note1

Continued

Pin No.	Symbol	Signal	Remarks
40	GND	Ground	Note1
41	RSEV	-	Keep this pin Open.
42	RSEV	-	Keep this pin Open.
43	RSEV	-	Keep this pin Open.
44	RSEV	-	Keep this pin Open.
45	GND	Ground	Note1
46	GND	Ground	Note1
47	GND	Ground	Note1
48	RSEV	-	Keep this pin Open.
49	RSEV	-	Keep this pin Open.
50	RSEV	-	Keep this pin Open.
51	GND	Ground	Note1

CN1: Insert surface side



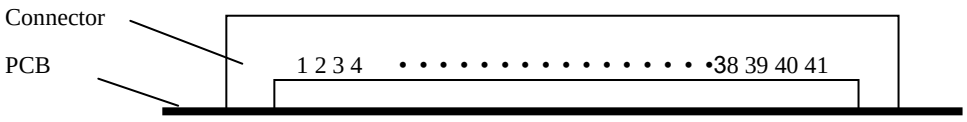
Note1: All GND terminals should be used without any non-connected lines.

Note2: Twist pair wires with 100Ω (Characteristic impedance) should be used between LCD panel signal processing board and LVDS transmitter.

CN2 socket (LCD module side): FI-RE41S-HF (Japan Aviation Electronics Industry Limited (JAE))
Adaptable plug: FI-RE41HL (Japan Aviation Electronics Industry Limited (JAE))

Pin No.	Symbol	Signal	Remarks
1	GND	Ground	Note1
2	GND	Ground	
3	GND	Ground	
4	DC0-	Pixel data C0	LVDS differential data input Note2
5	DC0+		
6	GND	Ground	Note1
7	DC1-	Pixel data C1	LVDS differential data input Note2
8	DC1+		
9	GND	Ground	Note1
10	DC2-	Pixel data C2	LVDS differential data input Note2
11	DC2+		
12	GND	Ground	Note1
13	CKC-	Pixel clock C	LVDS differential data input Note2
14	CKC+		
15	GND	Ground	Note1
16	DC3-	Pixel data C3	LVDS differential data input Note2
17	DC3+		
18	GND	Ground	Note1
19	GND	-	Keep this pin Open.
20	GND		
21	GND	Ground	Note1
22	DD0-	Pixel data D0	LVDS differential data input Note2
23	DD0+		
24	GND	Ground	Note1
25	DD1-	Pixel data D1	LVDS differential data input Note2
26	DD1+		
27	GND	Ground	Note1
28	DD2-	Pixel data D2	LVDS differential data input Note2
29	DD2+		
30	GND	Ground	Note1
31	CKD-	Pixel clock D	LVDS differential data input Note2
32	CKD+		
33	GND	Ground	Note1
34	DD3-	Pixel data D3	LVDS differential data input Note2
35	DD3+		
36	GND	Ground	Note1
37	GND	-	Keep this pin Open.
38	GND		
39	GND	Ground	Note1
40	GND	Ground	Note1
41	GND	Ground	Note1

CN2: Insert surface side

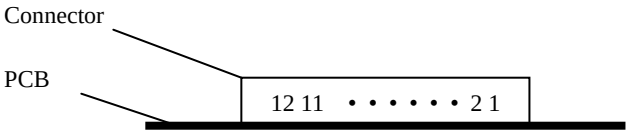


Note1: All GND terminals should be used without any non-connected lines.
Note2: Twist pair wires with 100Ω (Characteristic impedance) should be used between LCD panel signal processing board and LVDS transmitter.

CN3 socket (LCD module side): IL-Z-12PL-SMTYE (Japan Aviation Electronics Industry Limited (JAE))
Adaptable plug: IL-Z-12S-S125C (Japan Aviation Electronics Industry Limited (JAE))

Pin No.	Symbol	Function	Description
1	VDD	Power supply	Note1
2	VDD		
3	VDD		
4	VDD		
5	VDD		
6	VDD		
7	GND	Signal ground	Note1
8	GND		
9	GND		
10	GND		
11	GND		
12	GND		

CN3: Insert surface side



Note1: All VDD and GND terminals should be used without any non-connected lines.

4.5.2 LED driver

CN201 socket (LCD module side): DF3Z-10P-2H (2∗) (HIROSE ELECTRIC Co,. Ltd.)
Adaptable plug: DF3-10S-2C (HIROSE ELECTRIC Co,. Ltd.)

Pin No.	Symbol	Function	Description
1	GNDB	LED driver ground	Note1
2	GNDB		
3	GNDB		
4	GNDB		
5	GNDB		
6	VDDB	Power supply	Note1
7	VDDB		
8	VDDB		
9	VDDB		
10	VDDB		

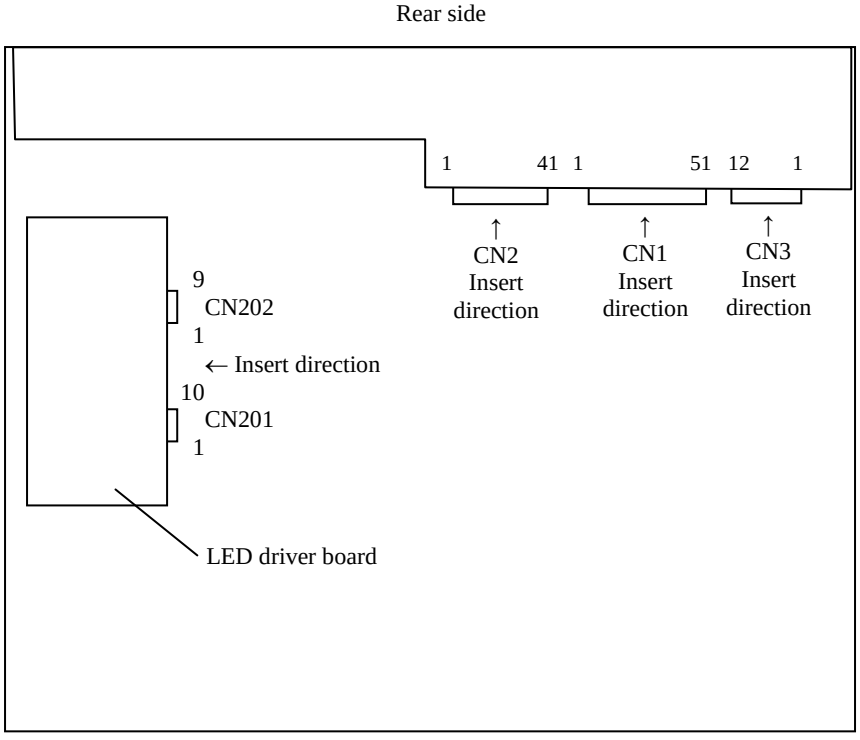
Note1: All VDDB and GNDB terminals should be used without any non-connected lines.

CN202 socket (LCD module side): 53261-0971 (MOLEX Inc.)
Adaptable plug: 51021-0900 (MOLEX Inc.)

Pin No.	Symbol	Function	Description
1	PWSEL	Selection of luminance control signal method	Note2, Note3
2	GNDB	LED driver ground	Note1
3	BRTP	BRTP signal	Note2
4	BRTI	Luminance control terminal	
5	BRTH		
6	BRTC	Backlight ON/OFF control signal	High or Open: Backlight ON Low: Backlight OFF
7	N. C.	-	Keep this pin Open.
8	GNDB	LED driver ground	Note1
9	GNDB		

Note1: All GNDB terminals should be used without any non-connected lines.
Note2: See "**4.6 LUMINANCE CONTROL** ".
Note3: When VDDB is 0V or BRTC is Low, PWSEL must be set to Low or Open.

4.5.3 Positions of socket

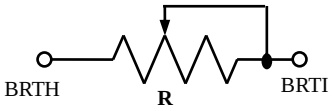


4.6 LUMINANCE CONTROL

4.6.1 Luminance control methods

<table>
<tr><th>Method</th><th>Adjustment and luminance ratio</th><th>PWSEL terminal</th><th>BRTP terminal</th></tr>
<tr><td>Variable resistor control

Note1</td><td>• Adjustment

The variable resistor (R) for luminance control should be 10kΩ ±5%, 1/10W. Minimum point of the resistance is the minimum luminance and maximum point of the resistance is the maximum luminance.
The resistor (R) must be connected between BRTH-BRTI terminals.
 

• Luminance ratio Note3
<table><tr><th>Resistance</th><th>Luminance ratio</th></tr><tr><td>0Ω</td><td>(25)% (typ.)</td></tr><tr><td>10 kΩ</td><td>100% (Max. Luminance)</td></tr></table></td><td rowspan="2">High or Open</td><td rowspan="2">Open</td></tr>
<tr><td>Voltage control

Note1</td><td>• Adjustment

Voltage control method works, when BRTH terminal is 0V and VBI voltage is input between BRTI-BRTH terminals. This control method can carry out continuation adjustment of luminance.
Luminance is the maximum when BRTI terminal is Open.

• Luminance ratio Note3
<table><tr><th>BRTI Voltage (VBI)</th><th>Luminance ratio</th></tr><tr><td>0V</td><td>(25)% (typ.)</td></tr><tr><td>1.0V</td><td>100% (Max. Luminance)</td></tr></table></td></tr>
<tr><td>Pulse width modulation

Note1
Note2
Note4</td><td>• Adjustment

Pulse width modulation (PWM) method works, when PWSEL terminal is Low and PWM signal (BRTP signal) is input into BRTP terminal. The luminance is controlled by duty ratio of BRTP signal.

• Luminance ratio Note3
<table><tr><th>Duty ratio</th><th>Luminance ratio</th></tr><tr><td>0.21 Note5</td><td>(25)% (typ.)</td></tr><tr><td>1.0</td><td>100% (Max. Luminance)</td></tr></table></td><td>Low</td><td>BRTP signal</td></tr>
</table>

2

Note1: In case of the variable resistor control method and the voltage control method, noises may appear on the display image depending on the input signals timing for LCD panel signal processing board.
Use PWM method, if interference noises appear on the display image!

Note2: The LED driver board will stop working, if the Low period of BRTP signal is more than 50ms while BRTC signal is High or Open. Then the backlight will not turn on anymore, even if BRTP signal is input again. This is not out of order. The LED driver board will start to work when power is supplied again.

Note3: These data are the target values.

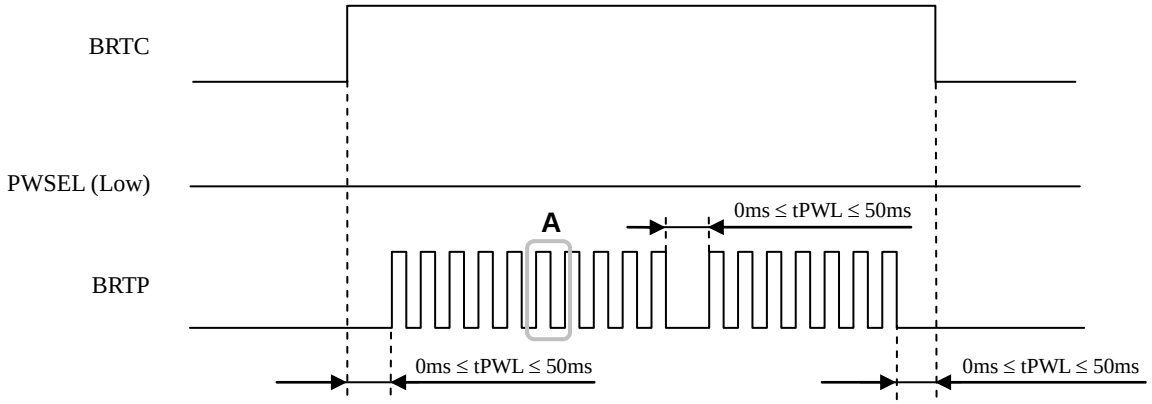
Note4: See "**4.6.2 Detail of BRTP timing**".

Note5: In the pulse width modulation mode, LED driver is designed so that it can work under the condition of duty ratio is about 0.1. 2
Although the LED elementary substance turns on at the duty ratio is about 0.1, the driving condition is not covered under warranty.
Therefore, in case that the customer drives the backlight at the duty ratio is less than 0.21, sufficient evaluation is required to the customer.

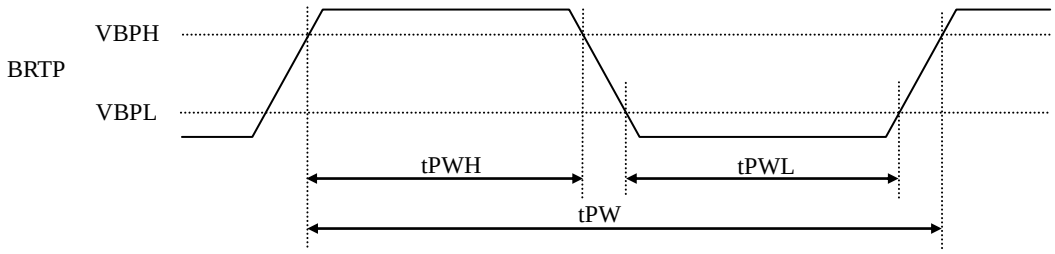
4.6.2 Detail of BRTP timing

(1) Timing diagrams

- Outline chart



- Detail of **A** part



(2) Each parameter

Parameter	Symbol	min.	typ.	max.	Unit	Remarks
PWM frequency	f_{PWM}	185	-	1,000	Hz	Note1,2,3
PWM duty ratio	DR_{PWM}	1	-	100	%	Note4,5
PWM pulse width	tPWH	TBD	-	-	μs	Note1,4,5

Note1: Definition of parameters is as follows.

$$f_{PWM} = \frac{1}{tPW}, \quad DR_{PWM} = \frac{tPWH}{tPW}$$

Note2: A recommended f_{PWM} value is as follows.

$$f_{PWM} = \frac{2n-1}{4} \times fv$$

(n= integer, fv= frame frequency of LCD module)

Note3: Depending on the frequency used, so noise may appear on the screen, please conduct a thorough evaluation.

Note4: While the BRTC signal is high, do not set the tPWH (PWM pulse width) is less than TBD μs. It may cause abnormal working of the backlight. In this case, turn the backlight off and then on again by BRTC signal.

Note5: Regardless of the PWM frequency, both PWM duty ratio and PWM pulse width must be always more than the minimum values.

4.7 METHOD OF CONNECTION FOR LVDS TRANSMITTER

LVDS data input map is selectable by BSEL terminal.

	Bit mapping			Transmitter Pin Assignment					CN1	
	BSEL Note1			Single type LVDS Tx	Dual type LVDS TX		Output Connector		Pin No.	Signal name
	[H] Mode A		[L] Mode C		THine THC63LVD823	NS DS90C387				
Pixel data A	RA2		RA0	TA0	R12	R10				
	RA3		RA1	TA1	R13	R11		Note2		
	RA4		RA2	TA2	R14	R12	ATA-	→	40	DA0-
	RA5		RA3	TA3	R15	R13	ATA+	→	39	DA0+
	RA6		RA4	TA4	R16	R14				
	RA7		RA5	TA5	R17	R15				
	GA2		GA0	TA6	G12	G10				
	GA3		GA1	TB0	G13	G11				
	GA4		GA2	TB1	G14	G12				
	GA5		GA3	TB2	G15	G13	ATB-	→	37	DA1-
	GA6		GA4	TB3	G16	G14	ATB+	→	36	DA1+
	GA7		GA5	TB4	G17	G15				
	BA2		BA0	TB5	B12	B10				
	BA3		BA1	TB6	B13	B11				
	BA4		BA2	TC0	B14	B12				
	BA5		BA3	TC1	B15	B13				
	BA6		BA4	TC2	B16	B14	ATC-	→	34	DA2-
	BA7		BA5	TC3	B17	B15	ATC+	→	33	DA2+
	Hsync		Hsync	TC4	HSYNC	HSYNC				
	Vsync		Vsync	TC5	VSYNC	VSYNC				
	DE		DE	TC6	DE	DE				
	RA0		RA6	TD0	R10	R16				
	RA1		RA7	TD1	R11	R17				
	GA0		GA6	TD2	G10	G16	ATD-	→	28	DA3-
	GA1		GA7	TD3	G11	G17	ATD+	→	27	DA3+
	BA0		BA6	TD4	B10	B16				
	BA1		BA7	TD5	B11	B17				
	N.C.		N.C.	TD6	-	-				
	CLK		CLK	CLK	CLK	CLK	ATCLK-	→	31	CKA-
							ATCLK+	→	30	CKA+
Pixel data B	RB2		RB0	TA0	R22	R20				
	RB3		RB1	TA1	R23	R21				
	RB4		RB2	TA2	R24	R22	BTA-	→	25	DB0-
	RB5		RB3	TA3	R25	R23	BTA+	→	24	DB0+
	RB6		RB4	TA4	R26	R24				
	RB7		RB5	TA5	R27	R25				
	GB2		GB0	TA6	G22	G20				
	GB3		GB1	TB0	G23	G21				
	GB4		GB2	TB1	G24	G22				
	GB5		GB3	TB2	G25	G23	BTB-	→	22	DB1-
	GB6		GB4	TB3	G26	G24	BTB+	→	21	DB1+
	GB7		GB5	TB4	G27	G25				
	BB2		BB0	TB5	B22	B20				
	BB3		BB1	TB6	B23	B21				
	BB4		BB2	TC0	B24	B22				
	BB5		BB3	TC1	B25	B23				
	BB6		BB4	TC2	B26	B24	BTC-	→	19	DB2-
	BB7		BB5	TC3	B27	B25	BTC+	→	18	DB2+
	Hsync		Hsync	TC4	HSYNC	HSYNC				
	Vsync		Vsync	TC5	VSYNC	VSYNC				
	DE		DE	TC6	DE	DE				
	RB0		RB6	TD0	R20	R26				
	RB1		RB7	TD1	R21	R27				
	GB0		GB6	TD2	G20	G26	BTD-	→	13	DB3-
	GB1		GB7	TD3	G21	G27	BTD+	→	12	DB3+
	BB0		BB6	TD4	B20	B26				
	BB1		BB7	TD5	B21	B27				
	N.C.		N.C.	TD6	-	-				
	CLK		CLK	CLK	CLK	CLK	BTCLK-	→	16	CKB-
							BTCLK+	→	15	CKB+

	BSEL Note1			Single type LVDS Tx	Dual type LVDS TX		Output Connector		CN2	
	[H] Mode A		[L] Mode C		THine THC63LVD823	NS DS90C387			Pin No.	Signal name
Pixel data C	RC2		RC0	TA0	R12	R10				
	RC3		RC1	TA1	R13	R11		Note2		
	RC4		RC2	TA2	R14	R12	CTA-	→	30	DC0-
	RC5		RC3	TA3	R15	R13	CTA+	→	29	DC0+
	RC6		RC4	TA4	R16	R14				
	RC7		RC5	TA5	R17	R15				
	GC2		GC0	TA6	G12	G10				
	GC3		GC1	TB0	G13	G11				
	GC4		GC2	TB1	G14	G12				
	GC5		GC3	TB2	G15	G13	CTB-	→	27	DC1-
	GC6		GC4	TB3	G16	G14	CTB+	→	26	DC1+
	GC7		GC5	TB4	G17	G15				
	BC2		BC0	TB5	B12	B10				
	BC3		BC1	TB6	B13	B11				
	BC4		BC2	TC0	B14	B12				
	BC5		BC3	TC1	B15	B13				
	BC6		BC4	TC2	B16	B14	CTC-	→	24	DC2-
	BC7		BC5	TC3	B17	B15	CTC+	→	23	DC2+
	Hsync		Hsync	TC4	HSYNC	HSYNC				
	Vsync		Vsync	TC5	VSYNC	VSYNC				
	DE		DE	TC6	DE	DE				
	RC0		RC6	TD0	R10	R16				
	RC1		RC7	TD1	R11	R17				
	GC0		GC6	TD2	G10	G16	CTD-	→	18	DC3-
	GC1		GC7	TD3	G11	G17	CTD+	→	17	DC3+
	BC0		BC6	TD4	B10	B16				
	BC1		BC7	TD5	B11	B17				
	N.C.		N.C.	TD6	-	-				
	CLK		CLK	CLK	CLK	CLK	CTCLK-	→	21	CKC-
							CTCLK+	→	20	CKC+
Pixel data D	RD2		RD0	TA0	R22	R20				
	RD3		RD1	TA1	R23	R21				
	RD4		RD2	TA2	R24	R22	DTA-	→	15	DD0-
	RD5		RD3	TA3	R25	R23	DTA+	→	14	DD0+
	RD6		RD4	TA4	R26	R24				
	RD7		RD5	TA5	R27	R25				
	GD2		GD0	TA6	G22	G20				
	GD3		GD1	TB0	G23	G21				
	GD4		GD2	TB1	G24	G22				
	GD5		GD3	TB2	G25	G23	DTB-	→	12	DD1-
	GD6		GD4	TB3	G26	G24	DTB+	→	11	DD1+
	GD7		GD5	TB4	G27	G25				
	BD2		BD0	TB5	B22	B20				
	BD3		BD1	TB6	B23	B21				
	BD4		BD2	TC0	B24	B22				
	BD5		BD3	TC1	B25	B23				
	BD6		BD4	TC2	B26	B24	DTC-	→	9	DD2-
	BD7		BD5	TC3	B27	B25	DTC+	→	8	DD2+
	Hsync		Hsync	TC4	HSYNC	HSYNC				
	Vsync		Vsync	TC5	VSYNC	VSYNC				
	DE		DE	TC6	DE	DE				
	RD0		RD6	TD0	R20	R26				
	RD1		RD7	TD1	R21	R27				
	GD0		GD6	TD2	G20	G26	DTD-	→	3	DD3-
	GD1		GD7	TD3	G21	G27	DTD+	→	2	DD3+
	BD0		BD6	TD4	B20	B26				
	BD1		BD7	TD5	B21	B27				
	N.C.		N.C.	TD6	-	-				
	CLK		CLK	CLK	CLK	CLK	DTCLK-	→	6	CKD-
							DTCLK+	→	5	CKD+

Note1: High must be Open.

Note2: Do not change the setting of BSEL during VDD ON period.

Note3: Twist pair wires with 100Ω (Characteristic impedance) should be used between LCD panel signal processing board and LVDS transmitter.

4.8 DISPLAY COLORS AND INPUT DATA SIGNALS

This product can display in equivalent to 16,777,216 colors in 256 gray scale in each R, G, B sub-pixel. Also the relation between display colors and input data signals is as the following table.

Display colors		Data signal (0: Low level, 1: High level)																											
		RA7	RA6	RA5	RA4	RA3	RA2	RA1	RA0	GA7	GA6	GA5	GA4	GA3	GA2	GA1	GA0	BA7	BA6	BA5	BA4	BA3	BA2	BA1	BA0
		RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0	GB7	GB6	GB5	GB4	GB3	GB2	GB1	GB0	BB7	BB6	BB5	BB4	BB3	BB2	BB1	BB0
		RC7	RC6	RC5	RC4	RC3	RC2	RC1	RC0	GC7	GC6	GC5	GC4	GC3	GC2	GC1	GC0	BC7	BC6	BC5	BC4	BC3	BC2	BC1	BC0
		RD7	RD6	RD5	RD4	RD3	RD2	RD1	RD0	GD7	GD6	GD5	GD4	GD3	GD2	GD1	GD0	BD7	BD6	BD5	BD4	BD3	BD2	BD1	BD0
Basic colors	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Red	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Magenta	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Green	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	Cyan	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Red gray scale	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	dark	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	↑					:								:								:			
	↓					:								:								:			
	bright	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Green gray scale	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
	dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
	↑					:								:								:			
	↓					:								:								:			
	bright	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0
		0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0
	Green	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
Blue gray scale	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
	↑					:								:								:			
	↓					:								:								:			
	bright	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

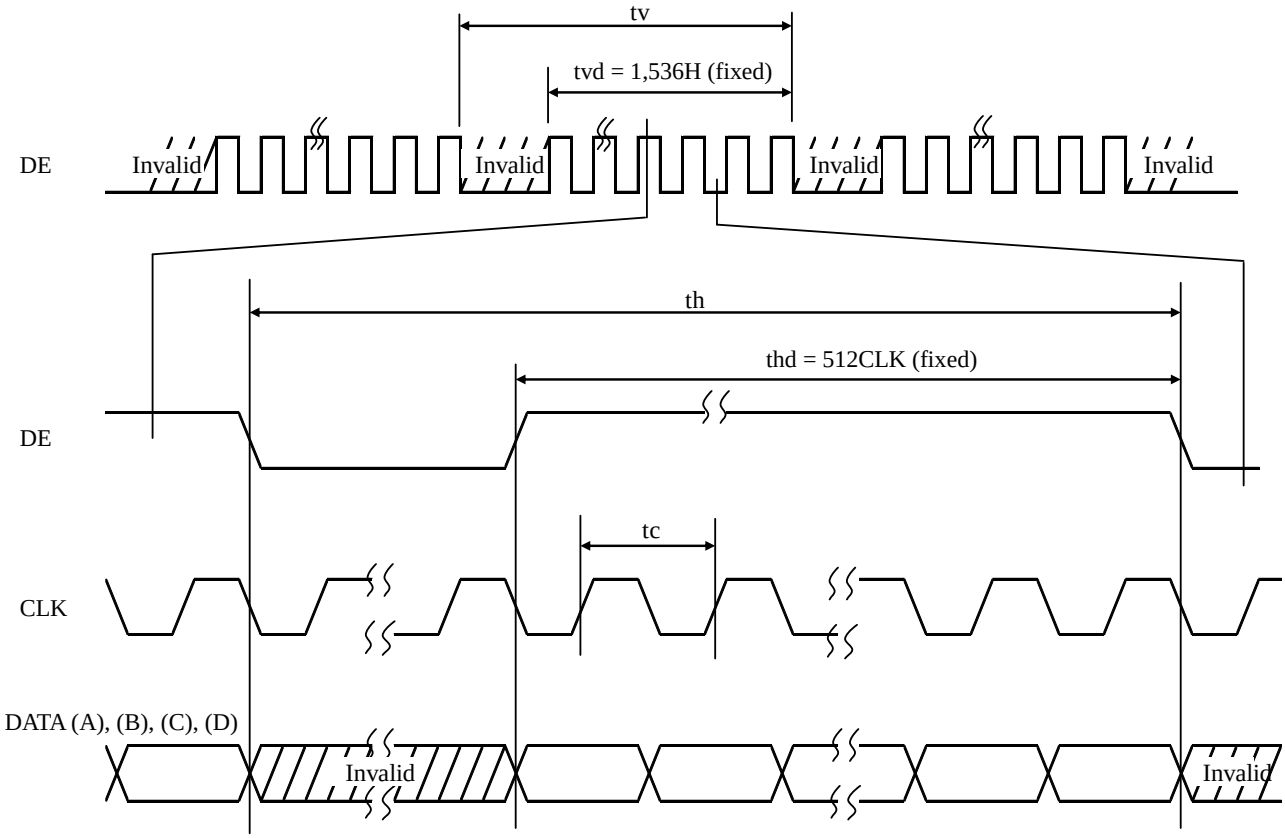
4.9 INPUT SIGNAL TIMINGS

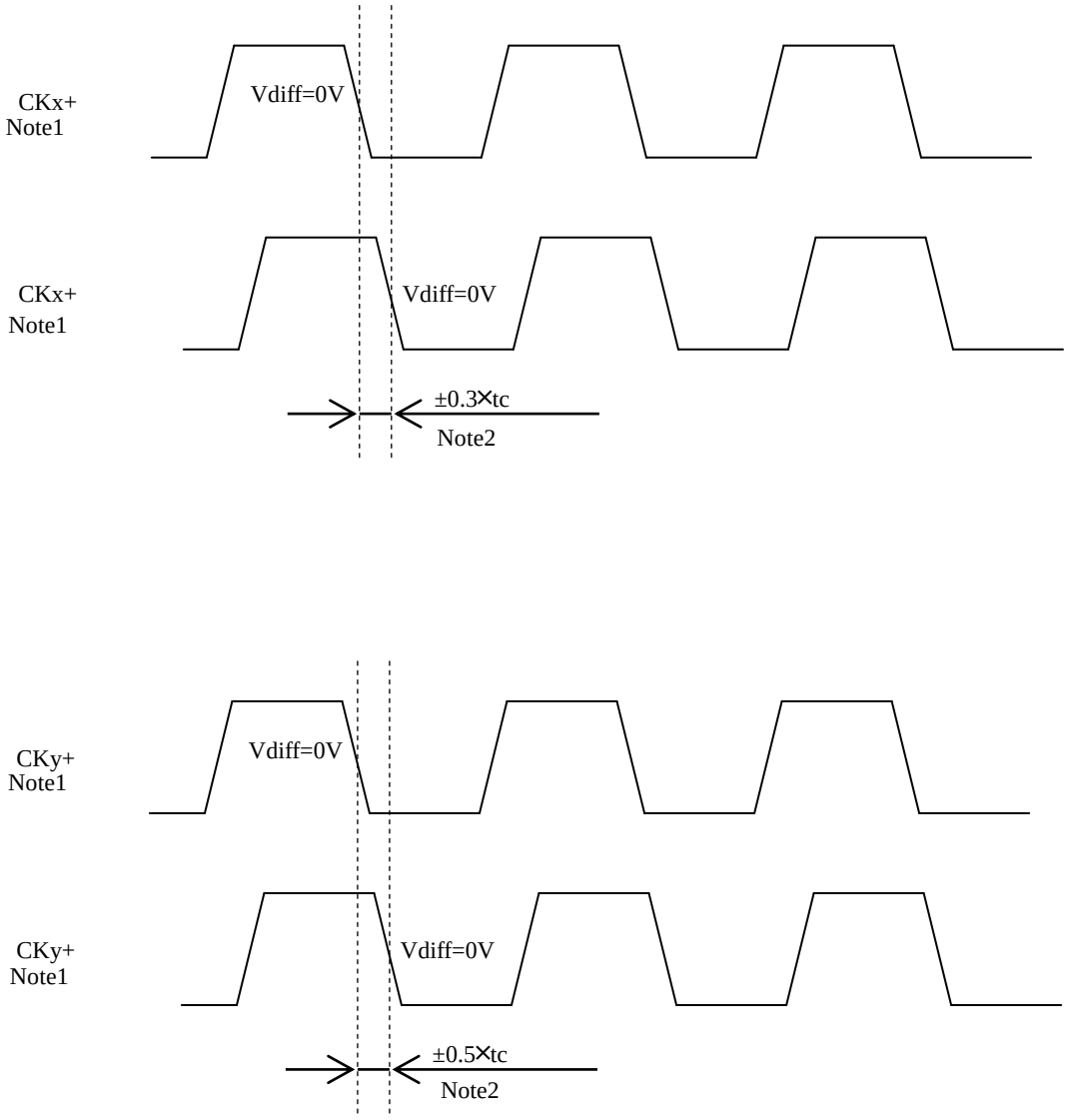
4.9.1 Timing characteristics

Parameter			Symbol	min.	typ.	max.	Unit	Remarks
CLK	Frequency		1/ tc	60.0	65.0	66.0	MHz	15.38 ns (typ.)
	Duty		-	See the data sheet of LVDS transmitter.			-	-
	Rise time, Fall time		-				ns	-
DE	Horizontal	Cycle	th	10.34	10.34	10.77	µs	96.72 kHz (typ.) Note1
				640	672	700	CLK	
		Display period	thd	512			CLK	-
	Vertical	Cycle	tv	15.47	16.667	17.9	ms	60.0 Hz (yp.)
				1,547	1,612	1,628	H	
		Display period	tvd	1,536			H	-
	CLK-DE	Setup time	-	See the data sheet of LVDS transmitter.			ns	-
		Hold time	-				ns	-
	Rise time, Fall time		-				ns	-
DATA (A) to (D)	CLK-DATA	Setup time	-	See the data sheet of LVDS transmitter.			ns	-
		Hold time	-				ns	-
	Rise time, Fall time		-				ns	-

Note1: The sum of jitter and skew of horizontal period should be within ±1 CLK.

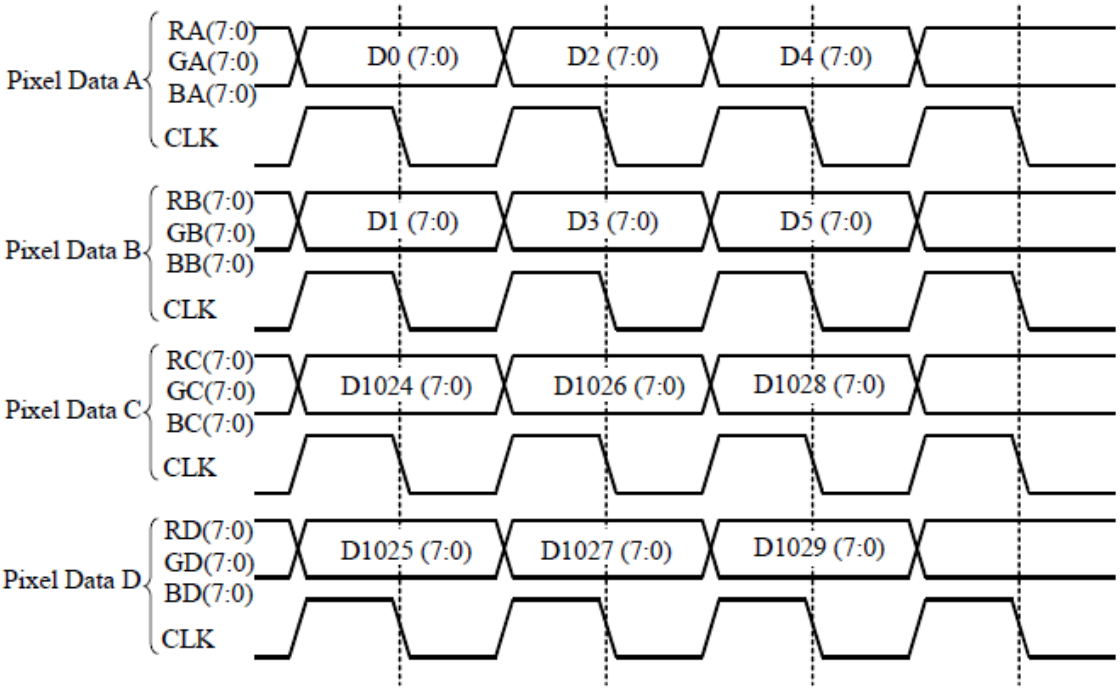
4.9.2 Input signal timing chart





Note1: Combination: y= A, C and y= A, D and y= B, C and y= B, D
Note2: CKA+ - CKC+ ≤+ 0.5 tc, CKA+ - CKD+ ≤+ 0.5 tc
CKB+ - CKC+ ≤+ 0.5 tc, CKB+ - CKD+ ≤+ 0.5 tc

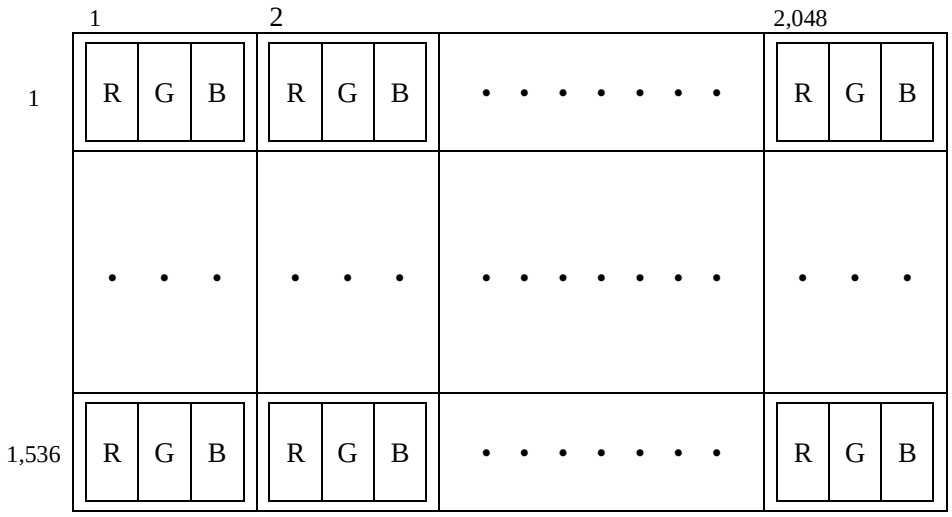
4.10 LVDS DATA TARANSMISSION METHOD



4.11 DISPLAY POSITIONS

1, 1	2, 1	• • •	1023, 1	1024, 1	1025, 1	1026, 1	• • •	2047, 1	2048, 1
1, 2	2, 2	• • •	1023, 2	1024, 2	1025, 2	1026, 2	• • •	2047, 2	2048, 2
•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•
1, 1535	2, 1535	• • •	1023, 1535	1024, 1535	1025, 1535	1026, 1535	• • •	2047, 1535	2048, 1535
1, 1536	2, 1536	• • •	1023, 1536	1024, 1536	1025, 1536	1026, 1536	• • •	2047, 1536	2048, 1536

4.12 PIXEL ARRANGNMENT



4.13 OPTICS

4.13.1 Optical characteristics

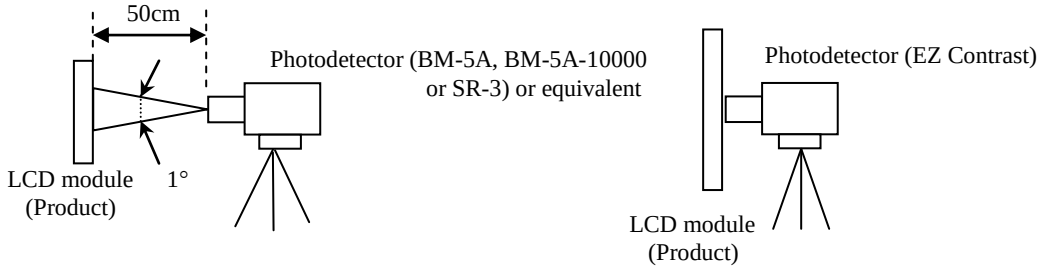
(Note1, Note2)

Parameter		Condition	Symbol	min.	typ.	max.	Unit	Measuring instrument	Remarks	
Luminance		White at center θR= 0°, θL= 0°, θU= 0°, θD= 0°	L	600	800	-	cd/m^2	BM-5A or SR-3	Note3	2
Contrast ratio		White/Black at center θR= 0°, θL= 0°, θU= 0°, θD= 0°	CR	(1,000)	1,400	-	-	BM-5A or SR-3	Note3 Note5	2
Luminance uniformity		White θR = 0°, θL = 0°, θU = 0°, θD = 0°	LU	80	-	-	%	BM-5A or SR-3	Note4 Note6	
Chromaticity	White	**x** coordinate	Wx	0.269	0.299	0.329		SR-3	Note3 Note7	
		y coordinate	Wy	0.285	0.315	0.345	-			
	Red	**x** coordinate	Rx	-	0.65	-	-			
		y coordinate	Ry	-	0.33	-	-			
	Green	**x** coordinate	Gx	-	0.29	-	-			
		y coordinate	Gy	-	0.60	-	-			
	Blue	**x** coordinate	Bx	-	0.15	-	-			
		y coordinate	By	-	0.07	-	-			
Color gamut		θR = 0°, θL = 0°, θU = 0°, θD = 0° at center, against NTSC color space	C	65	72	-	%	SR-3	Note3	
Response time		Black to White	Ton	-	(20)	(30)	ms	BM-5A -10000	Note8 Note9	2
		White to Black	Toff	-	(20)	(30)	ms			2
Viewing angle	Right	θU= 0°, θD= 0°, CR≥ 10	θR	70	88	-	°	BM-5A or EZ Contrast	Note3 Note10	
	Left	θU= 0°, θD= 0°, CR≥ 10	θL	70	88	-	°			
	Up	θR= 0°, θL= 0°, CR≥ 10	θU	70	88	-	°			
	Down	θR= 0°, θL= 0°, CR≥ 10	θD	70	88	-	°			

Note1: These are initial characteristics.

Note2: Measurement conditions are as follows.
Ta= 25°C, VDD= 12.0V, VDDB= 12.0V, PWM: Duty 100%, Display mode: QXGA,
Horizontal cycle= 1/96.72 kHz, Vertical cycle= 1/60.0 Hz

Optical characteristics are measured at luminance saturation 20minutes after the product works in the dark room. Also measurement methods are as follows.



Note3: Product surface temperature TopF= 32°C, TopR= 43°C (at the maximum luminance control)

Note4: Product surface temperature TopF= 30°C, TopR= 38°C (at the product luminance (450cd/m^2)) 2
LU is measured under the condition of temperature differences in the display area are less than 10°C

Note5: See "**4.13.2 Definition of contrast ratio**".
Note6: See "**4.13.3 Definition of luminance uniformity**".
Note7: These coordinates are found on CIE 1931 chromaticity diagram.
Note8: See "**4.13.4 Definition of response times**".
Note9 Product surface temperature TopF= (35)°C 2
Note10: See "**4.13.5 Definition of viewing angles**".

4.13.2 Definition of contrast ratio

The contrast ratio is calculated by using the following formula.

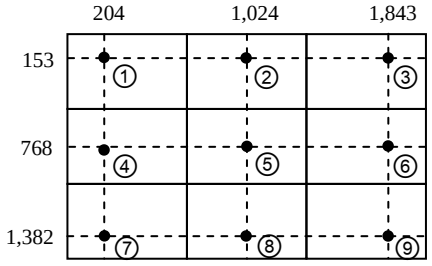
$$\text{Contrast ratio (CR)} = \frac{\text{Luminance of white screen}}{\text{Luminance of black screen}}$$

4.13.3 Definition of luminance uniformity

The luminance uniformity is calculated by using following formula.

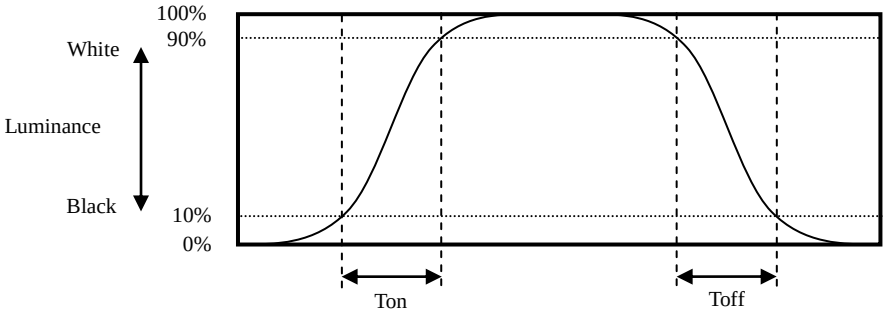
$$\text{Luminance uniformity (LU)} = \frac{\text{Minimum luminance from ① to ⑨}}{\text{Maximum luminance from ① to ⑨}}$$

The luminance is measured at near the 9 points shown below.

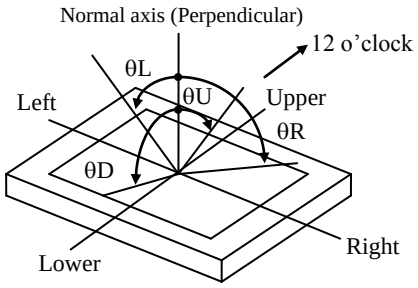


4.13.4 Definition of response times

Response time is measured at the time when the luminance changes from "black" to "white", or "white" to "black" on the same screen point, by photo-detector. Ton is the time when the luminance changes from 10% up to 90%. Also Toff is the time when the luminance changes from 90% down to 10% (See the following diagram.).



4.13.5 Definition of viewing angles



5. ESTIMATED LUMINANCE LIFETIME

The luminance lifetime is the time from initial luminance to half-luminance.

This lifetime is the estimated value, and is not guarantee value.

Condition		Estimated luminance lifetime (Life time expectancy) Note1, Note2, Note3	Unit
LED elementary substance	25°C (Ambient temperature of the product) Continuous operation, PWM: Duty 100%	70,000	h
	60°C (Temperature of LCD panel surface or LCD module's rear shield surface.) Continuous operation, PWM: Duty 100%	60,000	

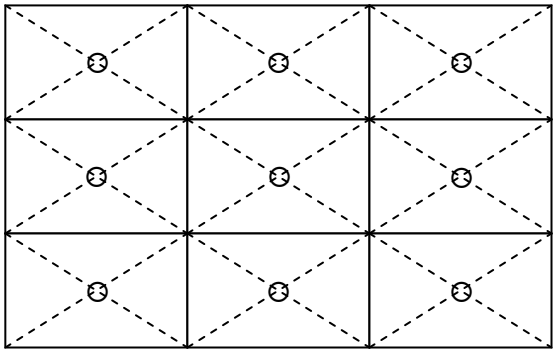
2

Note1: Life time expectancy is mean time to half-luminance.
Note2: Estimated luminance lifetime is not the value for LCD module but the value for LED elementary substance.
Note3: By ambient temperature, the lifetime changes particularly. Especially, in case the product works under high temperature environment, the lifetime becomes short.

6. RELIABILITY TESTS

Test item		Condition	Judgment Note1
High temperature and humidity (Operation)		① 60 ± 2°C, RH= 60%, 240hours ② Display data is white. Note2	No display malfunctions
Heat cycle (Operation)		① 0 ± 3°C 1hour 60 ± 3°C 1hour ② 50cycles, 4hours/cycle ③ Display data is white. Note2	
Thermal shock (Non operation)		① -20 ± 3°C 30minutes 60 ± 3°C 30minutes ② 100cycles, 1hour/cycle ③ Temperature transition time is within 5 minutes.	
Vibration (Non operation)		① 5 to 100Hz, 11.76m/s^2 ② 1 minute/cycle ③ X, Y, Z directions ④ 10 times each directions	No display malfunctions No physical damages
Mechanical shock (Non operation)		① 294m/s^2, 11ms ② X, Y, Z directions ③ 3 times each directions	
ESD (Operation)		① 150pF, 150Ω, ±10kV ② 9 places on a panel surface Note3 ③ 10 times each places at 1 sec interval	No display malfunctions
Low pressure	Non-operation	① 15kPa (Equivalent to altitude 13,600m) ② -20°C±3°C 24 hours ③ +60°C±3°C 24 hours	No display malfunctions
	Operation	① 53.3kPa (Equivalent to altitude 5,100m) ② 0°C±3°C 24 hours ③ +60°C±3°C 24 hours Note2	

Note1: Display and appearance are checked under environmental conditions equivalent to the inspection conditions of defect criteria.
Note2: Luminance: 450cd/m^2 at luminance control.
Note3: See the following figure for discharge points



7. PRECAUTIONS

7.1 MEANING OF CAUTION SIGNS

The following caution signs have very important meaning. **Be sure to read "7.2 CAUTIONS" and "7.3 ATTENTIONS"!**

This sign has the meaning that a customer will be injured or the product will sustain damage if the customer practices wrong operations.

This sign has the meaning that a customer will be injured if the customer practices wrong operations.

7.2 CAUTIONS

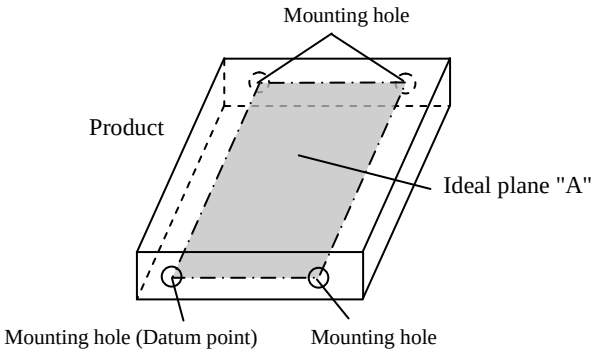
- **Do not shock and press the LCD panel and the backlight! There is a danger of breaking, because they are made of glass. (Shock: Equal to or no greater than 294m/s^2 and equal to or no greater than 11ms, Pressure: Equal to or no greater than 19.6N (ϕ16mm jig))**

7.3 ATTENTIONS

7.3.1 Handling of the product

① Take hold of both ends without touching the circuit board when the product (LCD module) is picked up from inner packing box to avoid broken down or misadjustment, because of stress to mounting parts on the circuit board.
② Do not hook or pull cables such as lamp cable, and so on, in order to avoid any damage.
③ When the product is put on the table temporarily, display surface must be placed downward.
④ When handling the product, take the measures of electrostatic discharge with such as earth band, ionic shower and so on, because the product may be damaged by electrostatic.
⑤ The torque for product mounting screws must never exceed 0.735N·m. Higher torque might result in distortion of the bezel. And the length of product mounting screws must be ≤ 5.0mm.

⑥ The product must be installed using mounting holes without undue stress such as bends or twist (See outline drawings). And do not add undue stress to any portion (such as bezel flat area). Bends or twist described above and undue stress to any portion may cause display mura.
Recommended installing method: Ideal plane "A" is defined by one mounting hole (datum point) and other mounting holes. The ideal plane "A" should be the same plane within ±0.3 mm.



⑦ Do not press or rub on the sensitive product surface. When cleaning the product surface, wipe it with a soft dry cloth.
⑧ Do not push or pull the interface connectors while the product is working.
⑨ When handling the product, use of an original protection sheet on the product surface (polarizer) is recommended for protection of product surface. Adhesive type protection sheet may change color or characteristics of the polarizer.
⑩ Usually liquid crystals don't leak through the breakage of glasses because of the surface tension of thin layer and the construction of LCD panel. But, if you contact with liquid crystal by any chance, please wash it away with soap and water.

7.3.2 Environment

① Do not operate or store in high temperature, high humidity, dewdrop atmosphere or corrosive gases. Keep the product in packing box with antistatic pouch in room temperature to avoid dusts and sunlight, when storing the product.
② In order to prevent dew condensation occurred by temperature difference, the product packing box must be opened after enough time being left under the environment of an unpacking room. Evaluate the storage time sufficiently because dew condensation is affected by the environmental temperature and humidity. (Recommended leaving time: 6 hours or more with the original packing state after a customer receives the package)
③ Do not operate in high magnetic field. If not, circuit boards may be broken.
④ This product is not designed as radiation hardened.

7.3.3 Characteristics

The following items are neither defects nor failures.

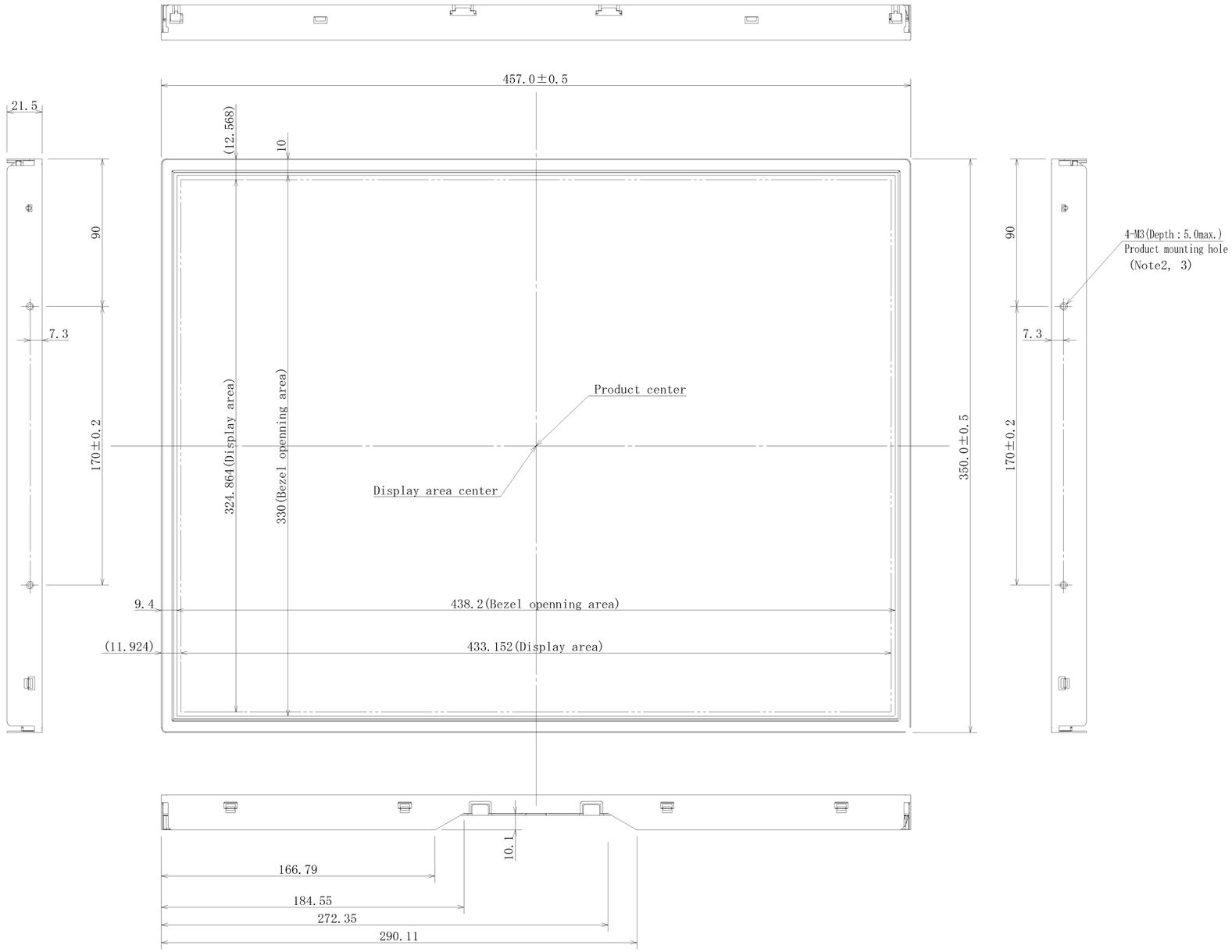
① Response time, luminance and color may be changed by ambient temperature.
② Display mura, flickering, vertical streams or tiny spots may be observed depending on display patterns.
③ Do not display the fixed pattern for a long time because it may cause image sticking. Use a screen saver, if the fixed pattern is displayed on the screen.
④ The display color may be changed depending on viewing angle because of the use of condenser sheet in the backlight.
⑤ Optical characteristics may be changed depending on input signal timings.

7.3.4 Others

① All GND, GNDB, VDD and VDDB terminals should be used without any non-connected lines.
② Do not disassemble a product or adjust variable resistors.
③ Pack the product with the original shipping package, in order to avoid any damages during transportation, when returning the product to NLT for repairing and so on.
④ The LCD module by itself or integrated into end product should be packed and transported with display in the vertical position. Otherwise the display characteristics may be degraded.

8. OUTLINE DRAWINGS

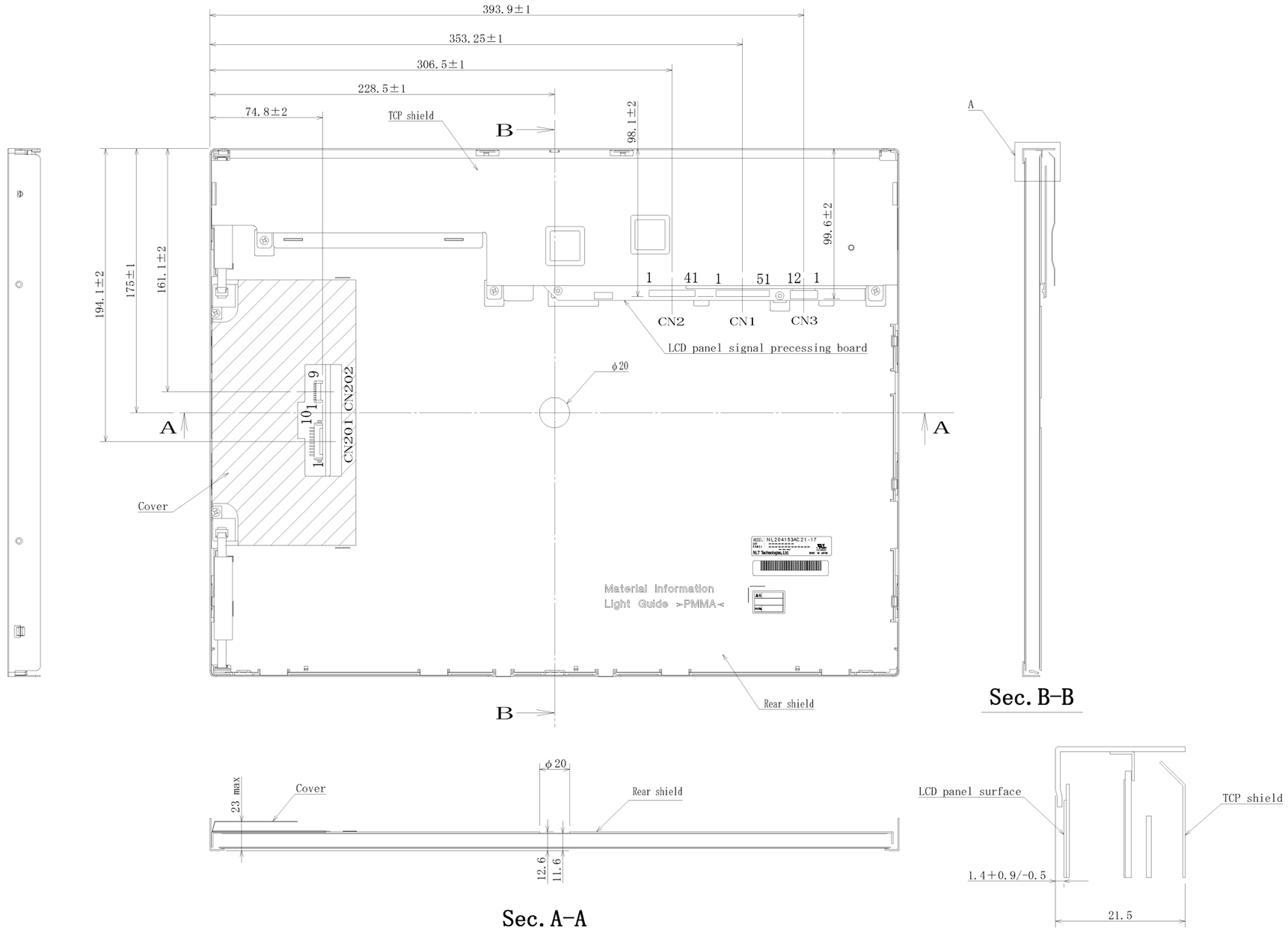
8.1 FRONT VIEW



Note1: Not shown tolerances of the dimensions are ±0.5mm.
Note2: The torque for product mounting screws must never exceed 0.735N·m.
Note3: The length of product mounting screws from surface of plate must be ≤ 5.0mm.
Note4: The values in parentheses are for reference.

Unit: mm

8.2 REAR VIEW



Note1: Not shown tolerances of the dimensions are ±0.5mm.
Note2: The torque for product mounting screws must never exceed 0.735N·m.
Note3: The length of product mounting screws from surface of plate must be ≤ 5.0mm.
Note4: The values in parentheses are for reference.

Unit: mm

REVISION HISTORY

The inside of latest specifications is revised to the clerical error and the major improvement of previous edition. Only a changed part such as functions, characteristic value and so on that may affect a design of customers, are described especially below.

Edition	Document number	Prepared date	Revision contents and signature
1st edition	DOD-PP-1803	Dec. 20, 2013	**Revision contents** New issue **Writer** *Approved by* R. KAWASHIMA　*Checked by* ＿＿＿＿＿＿　*Prepared by* E. YOSHIMURA
2nd edition	DOD-PP-1871	Mar. 13, 2014	**Revision contents** P5 GENERAL SPECIFICATIONS • Weight: (2,700) g (typ.) → 2,700 g (typ.) • Contrast ratio: (1,400:1) (typ.) → 1,400:1 (typ.) • Luminance: (800) cd/m^2 (typ.) → 800 cd/m^2 (typ.) • Power supply voltage- LED driver: 18.0V (addition) • Power consumption: (58.0)W (typ.) → (58.2)W (typ.) P7 DETAILED SPECIFICATIONS • Mechanical Specifications • Weight: (2,700), TBD (typ., max.) g → 2,700, 2,980 (typ., max.) g • Absolute Maximum Ratings • Operating temperature- Front surface, Rear surface: 0 to +55°C → 0 to +60°C P8 Electrical Characteristics • LCD panel signal processing board • Power supply current: 500, 900 (typ., max.) mA → (650), (980) (typ., max.) mA P9 LED driver • Power supply voltage: (10.8), (13.2) (min., max.) V → 11.4, 12.6 (min., max.) V : (16.2), (19.8) (min., max.) V → 17.1, 18.9 (min., max.) V P10 Power supply voltage ripple • VDDB- 18.0V: ≤ (200) mVp-p → ≤ 200 mVp-p Fuse • TF16AT5.00T (elimination) P18, 19 LUMINANCE CONTROL • Luminance control methods • Note5 (addition) P28, 29 OPTICS • Optical characteristics • Luminance: 660, (800) (min., typ.) cd/m^2 → 600, 800 (min., typ.) cd/m^2 • Contrast ratio: (1,400) (typ.) → 1,400 (typ.) • Response time- Ton, Toff: TBD (max.) ms → (30) (max.) ms • Note4: 450cd/m^2 → (450cd/m^2) • Note9: TopF= 35°C →T opF= (35)°C P30 ESTIMATED LUMINANCE LIFETIME • LED elementary substance : 55°C (Temperature of the product front or rear panel) → 60°C (Temperature of LCD panel surface or LCD module's rear shield surface.) P31 RELIABILITY TESTS • High temperature and humidity- ①: 55 ± 2°C → 60 ± 2°C • Heat cycle- ①: 55 ± 3°C → 60 ± 3°C **Signature of writer** *Approved by* R. KAWASHIMA　*Checked by* ＿＿＿＿＿＿　*Prepared by* A. KUMANO