

PRELIMINARY

NLT Technologies, Ltd.

TFT COLOR LCD MODULE

NL128102AC29-17

48cm (19.0 Type)

SXGA

LVDS interface (2port)

PRELIMINARY DATA SHEET 

DOD-PP-1517 (2nd edition)

This PRELIMINARY DATA SHEET is updated document from DOD-PP-1453(1)

All information is subject to change without notice. Please confirm the sales representative before starting to design your system.

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INTRODUCTION

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The **Standard**: Applications as any failure, malfunction or error of the products are free from any damage to death, human bodily injury or other property (Products Safety Issue) and not related the safety of the public (Social Issues), like general electric devices.

Examples: Office equipment, audio and visual equipment, communication equipment, test and measurement equipment, personal electronic equipment, home electronic appliances, car navigation system (with no vehicle control functions), seat entertainment monitor for vehicles and airplanes, fish finder (except marine radar integrated type), PDA, etc.

The **Special**: Applications as any failure, malfunction or error of the products might directly cause any damage to death, human bodily injury or other property (Products Safety Issue) and the safety of the public (Social Issues) and required high level reliability by conventional wisdom.

Examples: Vehicle/train/ship control system, traffic signals system, traffic information control system, air traffic control system, surgery/operation equipment monitor, disaster/crime prevention system, etc.

The **Specific**: Applications as any failure, malfunction or error of the products might severe cause any damage to death, human bodily injury or other property (Products Safety Issue) and the safety of the public (Social Issues) and developed, designed and manufactured in accordance with the standards or quality assurance program designated by the customer who requires extremely high level reliability and quality.

Examples: Aerospace system (except seat entertainment monitor), nuclear control system, life support system, etc.

The quality grade of this product is the "**Standard**" unless otherwise specified in this document.

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1. OUTLINE

1.1 STRUCTURE AND PRINCIPLE

Color LCD module NL128102AC29-17 is composed of the amorphous silicon thin film transistor liquid crystal display (a-Si TFT LCD) panel structure with driver LSIs for driving the TFT (Thin Film Transistor) array and a backlight.

The a-Si TFT LCD panel structure is injected liquid crystal material into a narrow gap between the TFT array glass substrate and a color-filter glass substrate.

Color (Red, Green, Blue) data signals from a host system (e.g. signal generator, etc.) are modulated into best form for active matrix system by a signal processing board, and sent to the driver LSIs which drive the individual TFT arrays.

The TFT array as an electro-optical switch regulates the amount of transmitted light from the backlight assembly, when it is controlled by data signals. Color images are created by regulating the amount of transmitted light through the TFT array of red, green and blue dots.

1.2 APPLICATION

- Color monitor system

1.3 FEATURES

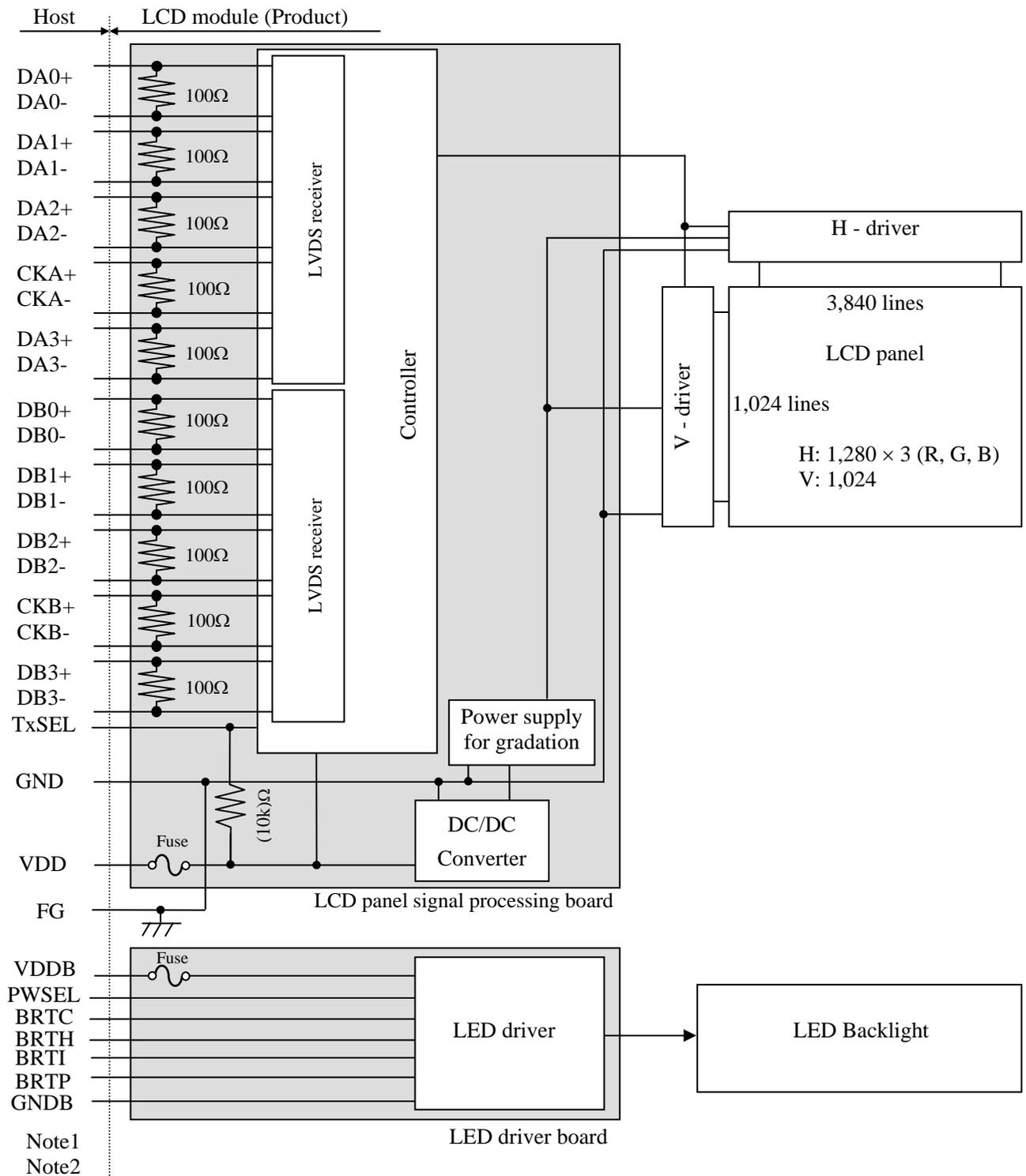
- Ultra-wide viewing angle (Super Fine TFT (SFT))
- Wide color gamut
- High luminance
- High contrast
- LVDS interface
- Selectable LVDS data input map
- LED backlight type
- LED driver Built-in

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2. GENERAL SPECIFICATIONS

Display area	376.32 (H) × 301.056 (V) mm	
Diagonal size of display	48cm (19.0 inches)	
Drive system	a-Si TFT active matrix	
Display color	16,777,216 colors	
Pixel	1,280 (H) × 1,024 (V) pixels	
Pixel arrangement	RGB (Red dot, Green dot, Blue dot) vertical stripe	
Dot pitch	0.098 (H) × 0.294 (V) mm	
Pixel pitch	0.294 (H) × 0.294 (V) mm	
Module size	396.0 (W) (typ.) × 324.0 (H) (typ.) × 22.0 (D) (max.) mm	2
Weight	TBD g (typ.)	
Contrast ratio	(1000):1 (typ.)	
Viewing angle	At the contrast ratio $\geq 10:1$ <ul style="list-style-type: none"> • Horizontal: Right side 88° (typ.), Left side 88° (typ.) • Vertical: Up side 88° (typ.), Down side 88° (typ.) 	
Designed viewing direction	<ul style="list-style-type: none"> • Viewing angle with optimum grayscale ($\gamma \approx 2.2$): Normal axis (perpendicular) 	
Polarizer surface	Antiglare	
Polarizer pencil-hardness	2H (min.) [by JIS K5600]	2
Color gamut	At LCD panel center 72% (typ.) [against NTSC color space]	
Response time	Ton+Toff (10%←→90%) 25ms (typ.)	
Luminance	At the maximum luminance control (800) cd/m ² (typ.)	2
Signal system	LVDS 2port (Receiver: THC63LVDF84B, Thine Electronics Inc. or equivalent) [8bit digital signals for data of RGB colors, Dot clock (CLK), Data enable (DE)]	
Power supply voltage	LCD panel signal processing board: 5.0V LED Driver board: 12.0V	
Backlight	LED backlight type (with LED driver Board)	
Power consumption	At BL Duty Ratio=100%, Checkered flag pattern (45.0)W (typ.) include LED driver board	2

3. BLOCK DIAGRAM



Note1: Relations between GND (Signal ground), GNDB (LED driver ground) and FG (Frame ground) in the LCD module are as follow.

GND - FG	Connected
GND - GNDB	NOT connected
FG - GNDB	NOT connected

Note2: GND, GNDB and FG must be connected to customer equipment's ground, and it is recommended that these grounds be connected together in customer equipment.

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4. DETAILED SPECIFICATIONS

4.1 MECHANICAL SPECIFICATIONS

Parameter	Specification	Unit
Module size	396.0 ± 0.5 (W) × 324.0 ± 0.5 (H) × TBD (D) (typ.)	Note1 Note2 mm
Display area	376.32 (H) × 301.056 (V)	Note1 mm
Weight	TBD (typ.)	g

Note1: Excluding a bulge of the cover for the signal processing board and the LED driver board.

Note2: See "9. OUTLINE DRAWINGS".

4.2 ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Unit	Remarks	
Power supply voltage	LCD panel signal processing board	VDD	-0.3 to +6.5	V	Ta = 25°C
	LED driver	VDDDB	-0.3 to +25.0		
Input voltage for signals	Display signals Note1	VD	-0.3 to +2.4	V	
	Function signals Note2	VF	-0.3 to +3.3		
	Function signal for LED driver	BRTC	-0.3 to +6.3		
		BRTI	-0.3 to +6.0		
		B RTP	-0.3 to +5.5		
PWSEL		-0.3 to +6.5			
Storage temperature	Tst	-30 to +80	°C	-	
Operating temperature	Front surface	TopF	-20 to +70	°C	
	Rear surface	TopR	-20 to +70	°C	Note4
Relative humidity Note5	RH	≤ 95	%	Ta ≤ 40°C	
		≤ 85	%	40°C < Ta ≤ 50°C	
		≤ 55	%	50°C < Ta ≤ 60°C	
		≤ 36	%	60°C < Ta ≤ 70°C	
Absolute humidity Note5	AH	≤ 70 Note6	g/m ³	Ta > 70°C	
Operating altitude	-	≤ 5,100	m	-20°C ≤ Ta ≤ 70°C	
Storage altitude	-	≤ 13,600	m	-30°C ≤ Ta ≤ 80°C	

Note1: Display signals are DA0+/-, DA1+/-, DA2+/-, DA3+/-, CKA+/-, DB0+/-, DB1+/-, DB2+/-, DB3+/-, CKB+/-

Note2: Function signal is TxSEL.

Note3: Measured at LCD panel surface (including self-heat)

Note4: Measured at LCD module's rear shield surface (including self-heat)

Note5: No condensation

Note6: Water amount at Ta= 70°C and RH= 36%

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4.3 ELECTRICAL CHARACTERISTICS

4.3.1 LCD panel signal processing board

(Ta= 25°C)

Parameter	Symbol	min.	typ.	max.	Unit	Remarks	
Power supply voltage	VDD	4.5	5.0	5.5	V	-	
Power supply current	IDD	-	(700) Note1	(900) Note2	mA	at VDD = 5.0V	
Permissible ripple voltage	VRP	-	-	100	mVp-p	for VDD	
Differential input threshold voltage	High	VTH	-	-	+100	mV	at VCM = 1.2V Note3
	Low	VTL	-100	-	-	mV	
Terminating resistance	RT	-	100	-	Ω	-	
Input voltage for TxSEL signal	High	VFH	Keep this pin open.			-	TxSEL Note4
	Low	VFL	-	-	(0.3)	V	
Input current for TxSEL signal	IFL	TBD	-	TBD	μA		

Note1: Checkered flag pattern [by EIAJ ED-2522]

Note2: Pattern for maximum current

Note3: Common mode voltage for LVDS receiver

Note4: TxSEL is pulled-up in the product. (Pull-up resistance: (10k)Ω)

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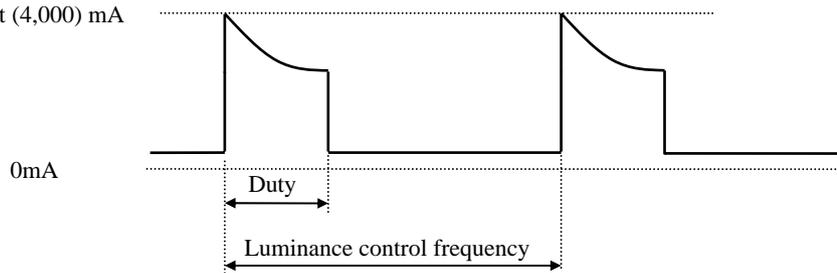
4.3.2 LED driver board

(Ta= 25°C)

Parameter		Symbol	min.	typ.	max.	Unit	Remarks
Power supply voltage		VDDB	10.8	12.0	13.2	V	-
Power supply current		IDDB	-	(3,300)	(3,700)	mA	VDDDB= 12.0V, At the maximum luminance control
Input voltage for signals	BRTI signal		VBI	0	-	1.0	V
	BRTP signal	High	VBPH	(2.0)	-	(5.0)	V
		Low	VBPL	0	-	(0.8)	V
	BRTC signal	High	VBCH	(1.8)	-	(5.0)	V
		Low	VBCL	0	-	(0.6)	V
	PWSEL signal	High	VBSH	(2.1)	-	(3.3)	V
Low		VBSL	0	-	(0.9)	V	
Input current for signals	BRTI signal		IBI	TBD	-	TBD	μA
	BRTP signal	High	IBPH	-	-	TBD	μA
		Low	IBPL	TBD	-	-	μA
	BRTC signal	High	IBCH	-	-	TBD	μA
		Low	IBCL	TBD	-	-	μA
	PWSEL signal	High	IPSH	-	-	TBD	μA
Low		IPSL	TBD	-	-	μA	

4.3.3 LED driver board current wave

Rush peak current (4,000) mA



Duty: At the maximum luminance control 100% to at the minimum luminance control 1%.

Luminance control frequency: 255 Hz (typ.)

Note1: Luminance control frequency indicate the input pulse frequency, when select the external pulse control. See "4.6.2 Detail of BRTP timing".

Note2: The power supply lines (VDDB and GNDB) have large ripple voltage during luminance control. There is the possibility that the ripple voltage produces acoustic noise and signal wave noise in audio circuit and so on. Put a capacitor (5,000 to 6,000μF) between the power supply lines (VDDB and GNDB) to reduce the noise, if the noise occurred in the circuit.

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4.3.4 Power supply voltage ripple

This product works, even if the ripple voltage levels are beyond the permissible values as following the table, but there might be noise on the display image.

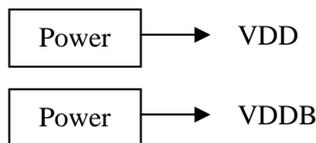
Power supply voltage		Ripple voltage (Measure at input terminal of power supply)	Note1	Unit
VDD	5.0V	≤ 100		mVp-p
VDDDB	12.0V	≤ 200		mVp-p

Note1: The permissible ripple voltage includes spike noise.

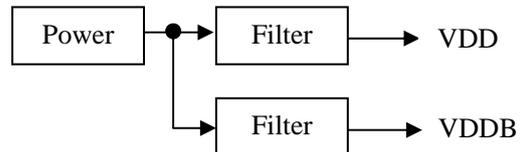
Note2: The load variation influence does not include.

Example of the power supply connection

a) Separate the power supply



b) Put in the filter



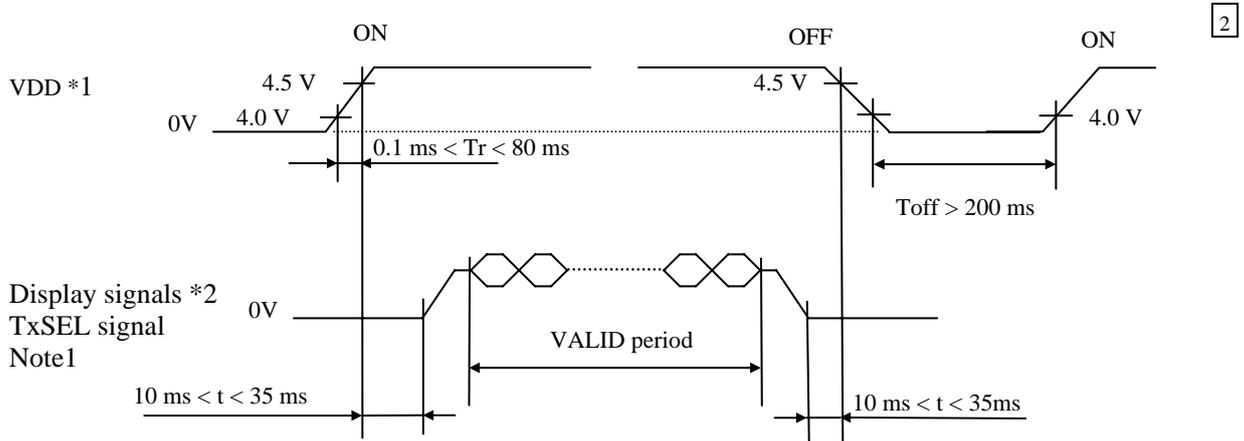
4.3.5 Fuse

Parameter	Fuse		Rating	Fusing current	Remarks
	Type	Supplier			
VDD	FCC32252AD	KAMAYA ELECTRIC Co.,Ltd.	2.5A	6.25A, 5 seconds maximum	Note1
			32V		
VDDDB	CRUCQ12LHK6A125V	CONQUER ELECTRONICS Co.,Ltd.	6.0A	18.0A, 3 seconds maximum	
			63V		
	CRUCQ12LVK4.0A125V		4.0A	10.0A, 5 seconds maximum	
			63V		
	CRUCQ12LVK2.5A125V		2.5A	6.25A, 5 seconds maximum	
			63V		

Note1: The power supply capacity should be more than the fusing current. If it is less than the fusing current, the fuse may not blow in a short time, and then nasty smell, smoke and so on may occur.

4.4 POWER SUPPLY VOLTAGE SEQUENCE

4.4.1 LCD panel signal processing board



*1 In terms of voltage variation (voltage drop) while VDD rising edge is below 4.5 V, a protection circuit may work, and then this product may not work. 2

*2 These signals should be measured at the terminal of 100 Ω resistances.

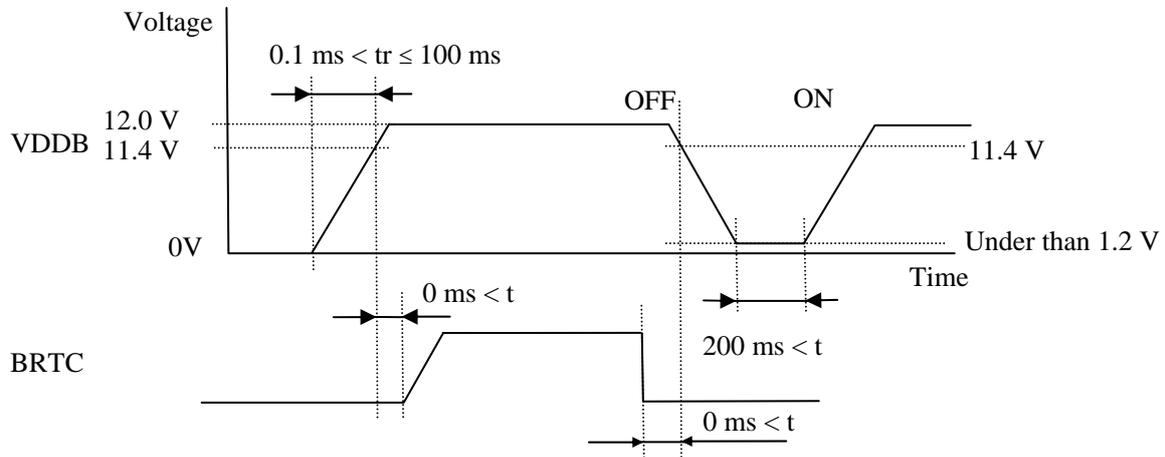
Note1: Display signals (DA0+/-, DA1+/-, DA2+/-, DA3+/-, CKA+/-, DB0+/-, DB1+/-, DB2+/-, DB3+/-, CKB+/-) and TxSEL signal must be "0" voltage, exclude the VALID period (See above sequence diagram). If these signals are higher than 0.3V, the internal circuit is damaged.

If some of display and function signals of this product are cut while this product is working, even if the signal input to it once again, it might not work normally. VDD should be cut when the display and function signals are stopped.

Note2: VDD should be 4.5 V or more while VDD ON period. 2

Note3: The backlight should be turned on within the valid period of display and function signals, in order to avoid unstable data display.

4.4.2 LED driver board



2

Note1: The backlight should be turned on within the valid period of LVDS signals, in order to avoid unstable data display.

Note2: If t_r is more than 100 ms, the backlight will be turned off by a protection circuit for LED driver board.

2

Note3: When VDDB is 0V or BRTC is Low, PWSEL must be set to Low or Open

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4.5 CONNECTIONS AND FUNCTIONS FOR INTERFACE PINS

4.5.1 LCD panel signal processing board

CN1 socket (LCD module side): FI-X30SSL-HF (Japan Aviation Electronics Industry Limited (JAE))
 Adaptable plug: FI-X30C series/ FI-X30H series/ FI-X30M series
 (Japan Aviation Electronics Industry Limited (JAE))

Pin No.	Symbol	Signal	Remarks
1	DA0-	Odd pixel data 0	Note1
2	DA0+		
3	DA1-	Odd pixel data 1	Note1
4	DA1+		
5	DA2-	Odd pixel data 2	Note1
6	DA2+		
7	GND	Ground	Note2
8	CKA-	Odd pixel clock	Note1
9	CKA+		
10	DA3-	Odd pixel data 3	Note1
11	DA3+		
12	DB0-	Even pixel data 0	Note1
13	DB0+		
14	GND	Ground	Note2
15	DB1-	Even pixel data 1	Note1
16	DB1+		
17	GND	Ground	Note2
18	DB2-	Even pixel data 2	Note1
19	DB2+		
20	CKB-	Even pixel clock	Note1
21	CKB+		
22	DB3-	Even pixel data 3	Note1
23	DB3+		
24	GND	Ground	Note2
25	TxSEL	Selection of LVDS data input map	Open: Mode A Low: Mode B Note3, Note4
26	RSVD	-	Keep this pin Open.
27	N.C.	-	Keep this pin Open.
28	VDD	Power supply	Note2
29			
30			

Note1: Twist pair wires with 100Ω (Characteristic impedance) should be used between LCD panel signal processing board and LVDS transmitter.

Note2: All GND and VDD terminals should be used without any non-connected lines.

Note3: TxSEL is pulled-up in the product. (Pull-up resistance: (10k)Ω)

Note4: See "**4.7 SELECTION OF LVDS DATA INPUT MAP**".

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4.5.2 LED driver board

CN201 socket (LCD module side): DF3Z-10P-2H (2*) (HIROSE ELECTRIC Co.,Ltd.)

Adaptable plug: DF3-10S-2C (HIROSE ELECTRIC Co.,Ltd.)

Pin No.	Symbol	Function	Description
1	GNDB	LED driver board ground	Note1
2	GNDB		
3	GNDB		
4	GNDB		
5	GNDB		
6	VDDB	Power supply	Note1
7	VDDB		
8	VDDB		
9	VDDB		
10	VDDB		

Note1: All VDDB and GNDB terminals should be used without any non-connected lines.

CN202 socket (LCD module side): IL-Z-9PL-SMTYE (Japan Aviation Electronics Industry Limited (JAE))

Adaptable plug: IL-Z-9S-S125C3 (Japan Aviation Electronics Industry Limited (JAE))

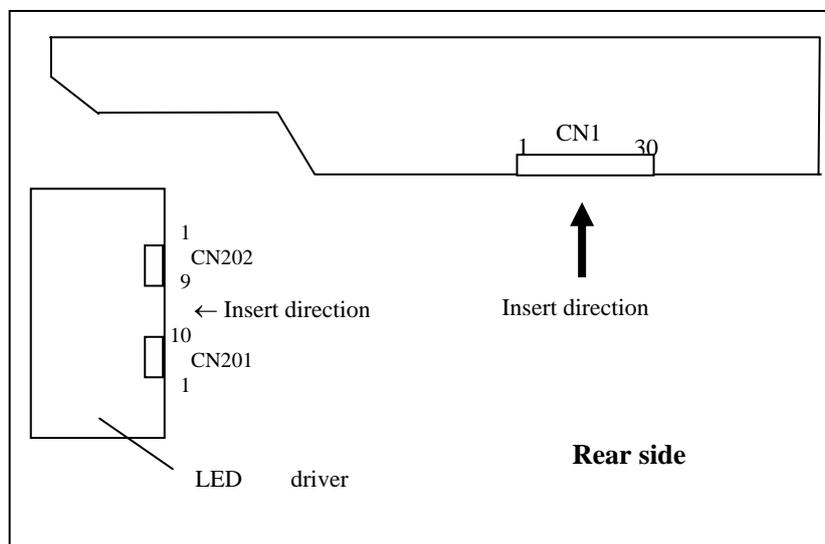
Pin No.	Symbol	Function	Description
1	GNDB	LED driver board ground	Note1
2	GNDB		
3	N.C.	-	Keep this pin Open.
4	BRTC	Backlight ON/OFF control signal	High or Open: Backlight ON Low: Backlight OFF
5	BRTH	Luminance control terminal	Note2
6	BRTI		
7	BRTP	BRTP signal	
8	GNDB	LED driver board ground	Note1
9	PWSEL	Selection of luminance control signal method	Note2, Note3

Note1: All GNDB terminals should be used without any non-connected lines.

Note2: See "4.6 LUMINANCE CONTROL".

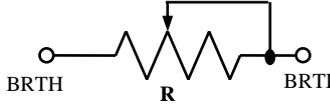
Note3: When VDDB is 0V or BRTC is Low, PWSEL must be set to Low or Open.

4.5.3 Positions of plug and socket



4.6 LUMINANCE CONTROL

4.6.1 Luminance control methods

Method	Adjustment and luminance ratio	PWSEL terminal	BRTP terminal						
<p>Variable resistor control</p> <p>Note1</p>	<ul style="list-style-type: none"> Adjustment <p>The variable resistor (R) for luminance control should be 10kΩ ±5%, 1/10W. Minimum point of the resistance is the minimum luminance and maximum point of the resistance is the maximum luminance.</p> <p>The resistor (R) must be connected between BRTH-BRTI terminals.</p> <div style="text-align: center;">  </div> <ul style="list-style-type: none"> Luminance ratio Note3 <table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>Resistance</th> <th>Luminance ratio</th> </tr> </thead> <tbody> <tr> <td>0 kΩ</td> <td>0% (Min. Luminance)</td> </tr> <tr> <td>10 kΩ</td> <td>100% (Max. Luminance)</td> </tr> </tbody> </table>	Resistance	Luminance ratio	0 kΩ	0% (Min. Luminance)	10 kΩ	100% (Max. Luminance)	High or Open	Open
Resistance	Luminance ratio								
0 kΩ	0% (Min. Luminance)								
10 kΩ	100% (Max. Luminance)								
<p>Voltage control</p> <p>Note1</p>	<ul style="list-style-type: none"> Adjustment <p>Voltage control method works, when BRTH terminal is 0V and VBI voltage is input between BRTI-BRTH terminals. This control method can carry out continuation adjustment of luminance.</p> <p>Luminance is the maximum when BRTI terminal is Open</p> <ul style="list-style-type: none"> Luminance ratio Note3 <table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>BRTI Voltage (VBI)</th> <th>Luminance ratio</th> </tr> </thead> <tbody> <tr> <td>0 V</td> <td>0% (Min. Luminance)</td> </tr> <tr> <td>1.0 V</td> <td>100% (Max. Luminance)</td> </tr> </tbody> </table>	BRTI Voltage (VBI)	Luminance ratio	0 V	0% (Min. Luminance)	1.0 V	100% (Max. Luminance)		
BRTI Voltage (VBI)	Luminance ratio								
0 V	0% (Min. Luminance)								
1.0 V	100% (Max. Luminance)								
<p>Pulse width modulation</p> <p>Note1 Note2 Note4</p>	<ul style="list-style-type: none"> Adjustment <p>Pulse width modulation (PWM) method works, when PWSEL terminal is Low and PWM signal (BRTP signal) is input into BRTP terminal. The luminance is controlled by duty ratio of BRTP signal.</p> <ul style="list-style-type: none"> Luminance ratio Note3 <table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>Duty ratio</th> <th>Luminance ratio</th> </tr> </thead> <tbody> <tr> <td>0.01</td> <td>1% (Min. Luminance) (At frequency: 325 Hz)</td> </tr> <tr> <td>1.0</td> <td>100% (Max. Luminance)</td> </tr> </tbody> </table>	Duty ratio	Luminance ratio	0.01	1% (Min. Luminance) (At frequency: 325 Hz)	1.0	100% (Max. Luminance)	Low	BRTP signal
Duty ratio	Luminance ratio								
0.01	1% (Min. Luminance) (At frequency: 325 Hz)								
1.0	100% (Max. Luminance)								

Note1: In case of the variable resistor control method and the voltage control method, noises may appear on the display image depending on the input signals timing for LCD panel signal processing board.

Use PWM method, if interference noises appear on the display image!

Note2: The LED driver board will stop working, if the Low period of BRTP signal is more than 50ms while BRTC signal is High or Open. Then the backlight will not turn on anymore, even if BRTP signal is input again. This is not out of order. The LED driver board will start to work when power is supplied again.

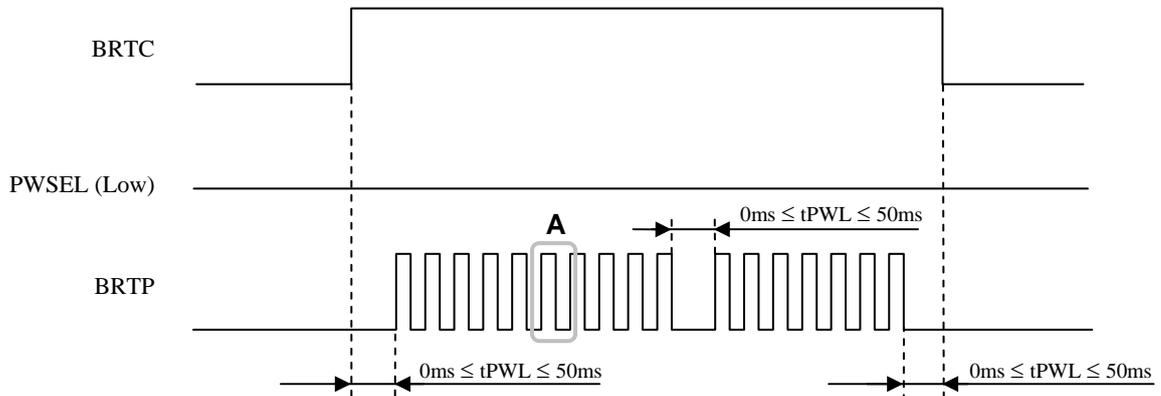
Note3: These data are the target values.

Note4: See "4.6.2 Detail of BRTP timing".

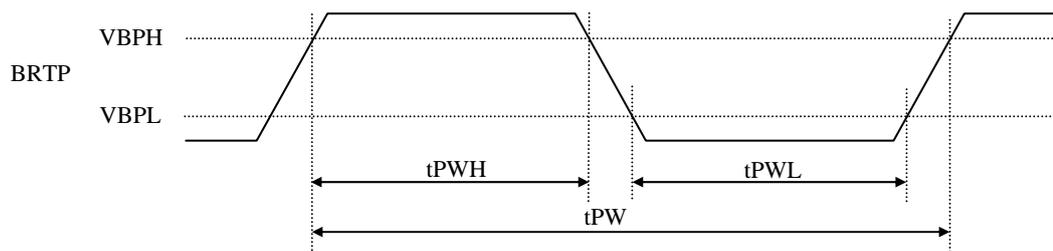
4.6.2 Detail of BRTP timing

(1) Timing diagrams

• Outline chart



• Outline chart



(2) Each parameter

Parameter	Symbol	min.	typ.	max.	Unit	Remarks
PWM frequency	f_{PWM}	(185)	-	(1,000)	Hz	Note1,2,3
PWM duty ratio	DR_{PWM}	1	-	100	%	Note4,5
PWM pulse width	tPWH	(30)	-	-	μs	Note1,4,5

Note1: Definition of parameters is as follows.

$$f_{PWM} = \frac{1}{tPW} \quad , \quad DL = \frac{tPWH}{tPW}$$

Note2: A recommended f_{PWM} value is as follows.

$$f_{PWM} = \frac{2n-1}{4} \times fv$$

(n= integer, fv= frame frequency of LCD module)

Note3: Depending on the frequency used, so noise may appear on the screen, please conduct a thorough evaluation.

Note4: While the BRTC signal is high, do not set the tPWH (PWM pulse width) is less than (30) μs . It may cause abnormal working of the backlight. In this case, turn the backlight off and then on again by BRTC signal.

Note5: Regardless of the PWM frequency, both PWM duty ratio and PWM pulse width must be always more than the minimum values.

PRELIMINARY

4.7 SELECTION OF LVDS DATA INPUT MAP

4.7.1 Mode A

Input data		Note1		Transmitter				Note2		CN1		
				Pin	THC63LVDM83D or equivalent	Pin	THC63LVD823 or equivalent			Pin	Symbol	
Odd pixel data and control signal	RA0	→	51	TA0	1st	53	R12					
	RA1	→	52	TA1		54	R13	TA1-	→	1	DA0-	
	RA2	→	54	TA2		57	R14	TA1+	→	2	DA0+	
	RA3	→	55	TA3		58	R15					
	RA4	→	56	TA4		59	R16	TB1-	→	3	DA1-	
	RA5	→	3	TA5		60	R17	TB1+	→	4	DA1+	
	GA0	→	4	TA6		63	G12					
	GA1	→	6	TB0		64	G13	TC1-	→	5	DA2-	
	GA2	→	7	TB1		65	G14	TC1+	→	6	DA2+	
	GA3	→	11	TB2		66	G15					
	GA4	→	12	TB3		67	G16	TCLK1-	→	8	CKA-	
	GA5	→	14	TB4		68	G17	TCLK1+	→	9	CKA+	
	BA0	→	15	TB5		73	B12					
	BA1	→	19	TB6		74	B13	TD1-	→	10	DA3-	
	BA2	→	20	TC0		75	B14	TD1+	→	11	DA3+	
	BA3	→	22	TC1		76	B15					
	BA4	→	23	TC2		77	B16					
	BA5	→	24	TC3		78	B17					
	Note3	RSVD	→	27		TC4	7	RSVD				
	Note3	RSVD	→	28		TC5	8	RSVD				
		DE	→	30		TC6	9	DE				
		RA6	→	50		TD0	51	R10				
		RA7	→	2		TD1	52	R11				
		GA6	→	8		TD2	61	G10				
		GA7	→	10		TD3	62	G11				
		BA6	→	16		TD4	69	B10				
		BA7	→	18		TD5	70	B11				
	Note3	RSVD	→	25		TD6	-					
		CLK	→	31		CLKIN	10	CLK				
	Even pixel data	RB0	→	51		TA0	2nd	81	R22			
		RB1	→	52		TA1		82	R23	TA2-	→	12
RB2		→	54	TA2	83	R24		TA2+	→	13	DB0+	
RB3		→	55	TA3	84	R25						
RB4		→	56	TA4	85	R26		TB2-	→	15	DB1-	
RB5		→	3	TA5	86	R27		TB2+	→	16	DB1+	
GB0		→	4	TA6	91	G22						
GB1		→	6	TB0	92	G23		TC2-	→	18	DB2-	
GB2		→	7	TB1	93	G24		TC2+	→	19	DB2+	
GB3		→	11	TB2	94	G25						
GB4		→	12	TB3	95	G26		TCLK2-	→	20	CKB-	
GB5		→	14	TB4	96	G27		TCLK2+	→	21	CKB+	
BB0		→	15	TB5	99	B22						
BB1		→	19	TB6	100	B23		TD2-	→	22	DB3-	
BB2		→	20	TC0	1	B24		TD2+	→	23	DB3+	
BB3		→	22	TC1	2	B25						
BB4		→	23	TC2	5	B26						
BB5		→	24	TC3	6	B27						
Note3		RSVD	→	27	TC4	-						
Note3		RSVD	→	28	TC5	-						
Note3		RSVD	→	30	TC6	-						
		RB6	→	50	TD0	79		R20				
		RB7	→	2	TD1	80		R21				
		GB6	→	8	TD2	89		G20				
		GB7	→	10	TD3	90		G21				
		BB6	→	16	TD4	97		B20				
		BB7	→	18	TD5	98		B21				
Note3		RSVD	→	25	TD6	-						
		CLK	→	31	CLKIN	-						

PRELIMINARY

4.7.2 Mode B

Input data		Note1		Transmitter				Note2		CN1		
				Pin	THC63LVDM83D or equivalent	Pin	THC63LVD823 or equivalent			Pin	Symbol	
Odd pixel data and control signal	RA2	→	51	TA0	1st	53	R12					
	RA3	→	52	TA1		54	R13	TA1-	→	1	DA0-	
	RA4	→	54	TA2		57	R14	TA1+	→	2	DA0+	
	RA5	→	55	TA3		58	R15					
	RA6	→	56	TA4		59	R16	TB1-	→	3	DA1-	
	RA7	→	3	TA5		60	R17	TB1+	→	4	DA1+	
	GA2	→	4	TA6		63	G12					
	GA3	→	6	TB0		64	G13	TC1-	→	5	DA2-	
	GA4	→	7	TB1		65	G14	TC1+	→	6	DA2+	
	GA5	→	11	TB2		66	G15					
	GA6	→	12	TB3		67	G16	TCLK1-	→	8	CKA-	
	GA7	→	14	TB4		68	G17	TCLK1+	→	9	CKA+	
	BA2	→	15	TB5		73	B12					
	BA3	→	19	TB6		74	B13	TD1-	→	10	DA3-	
	BA4	→	20	TC0		75	B14	TD1+	→	11	DA3+	
	BA5	→	22	TC1		76	B15					
	BA6	→	23	TC2		77	B16					
	BA7	→	24	TC3		78	B17					
	Note3	RSVD	→	27		TC4	7	RSVD				
	Note3	RSVD	→	28		TC5	8	RSVD				
		DE	→	30		TC6	9	DE				
		RA0	→	50		TD0	51	R10				
		RA1	→	2		TD1	52	R11				
		GA0	→	8		TD2	61	G10				
		GA1	→	10		TD3	62	G11				
		BA0	→	16		TD4	69	B10				
		BA1	→	18		TD5	70	B11				
	Note3	RSVD	→	25		TD6	-					
		CLK	→	31		CLKIN	10	CLK				
	Even pixel data	RB2	→	51		TA0	2nd	81	R22			
		RB3	→	52		TA1		82	R23	TA2-	→	12
RB4		→	54	TA2	83	R24		TA2+	→	13	DB0+	
RB5		→	55	TA3	84	R25						
RB6		→	56	TA4	85	R26		TB2-	→	15	DB1-	
RB7		→	3	TA5	86	R27		TB2+	→	16	DB1+	
GB2		→	4	TA6	91	G22						
GB3		→	6	TB0	92	G23		TC2-	→	18	DB2-	
GB4		→	7	TB1	93	G24		TC2+	→	19	DB2+	
GB5		→	11	TB2	94	G25						
GB6		→	12	TB3	95	G26		TCLK2-	→	20	CKB-	
GB7		→	14	TB4	96	G27		TCLK2+	→	21	CKB+	
BB2		→	15	TB5	99	B22						
BB3		→	19	TB6	100	B23		TD2-	→	22	DB3-	
BB4		→	20	TC0	1	B24		TD2+	→	23	DB3+	
BB5		→	22	TC1	2	B25						
BB6		→	23	TC2	5	B26						
BB7		→	24	TC3	6	B27						
Note3		RSVD	→	27	TC4	-						
Note3		RSVD	→	28	TC5	-						
Note3		RSVD	→	30	TC6	-						
		RB0	→	50	TD0	79		R20				
		RB1	→	2	TD1	80		R21				
		GB0	→	8	TD2	89		G20				
		GB1	→	10	TD3	90		G21				
		BB0	→	16	TD4	97		B20				
		BB1	→	18	TD5	98		B21				
Note3		RSVD	→	25	TD6	-						
		CLK	→	31	CLKIN	-						

PRELIMINARY

Note1: LSB (Least Significant Bit) – RA0, GA0, BA0, RB0, GB0, BB0

MSB (Most Significant Bit) – RA7, GA7, BA7, RB7, GB7, BB7

Note2: Twist pair wires with 100Ω (Characteristic impedance) should be used between LCD panel signal processing board and LVDS transmitter.

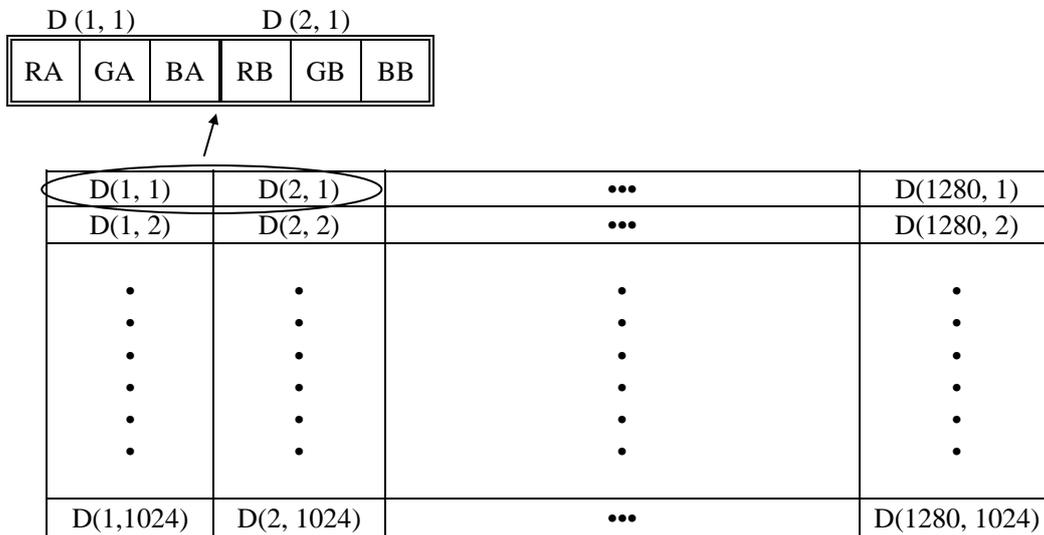
Note3: Input signal RSVD is not used inside the product, but do not keep pin open to avoid noise problem.

4.8 DISPLAY COLORS AND INPUT DATA SIGNALS

This product can display in equivalent to 16,777,216 colors in 256 gray scales. Also the relation between display colors and input data signals is as the following table.

Display colors		Data signal (0: Low level, 1: High level)																							
		RA7	RA6	RA5	RA4	RA3	RA2	RA1	RA0	GA7	GA6	GA5	GA4	GA3	GA2	GA1	GA0	BA7	BA6	BA5	BA4	BA3	BA2	BA1	BA0
		RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0	GB7	GB6	GB5	GB4	GB3	GB2	GB1	GB0	BB7	BB6	BB5	BB4	BB3	BB2	BB1	BB0
Basic Colors	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Red	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Magenta	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Green	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	Cyan	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Red gray scale	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	dark	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	↑					:																			
	↓					:																			
	bright	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Red	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
Red	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
Green gray scale	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
	dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
	↑					:																			
	↓					:																			
	bright	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0
Green	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	
Green	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	
Blue gray scale	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
	↑					:																			
	↓					:																			
	bright	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1
Blue	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	
Blue	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	

4.9 DISPLAY POSITION



4.10 INPUT SIGNAL TIMINGS

4.10.1 Timing characteristics

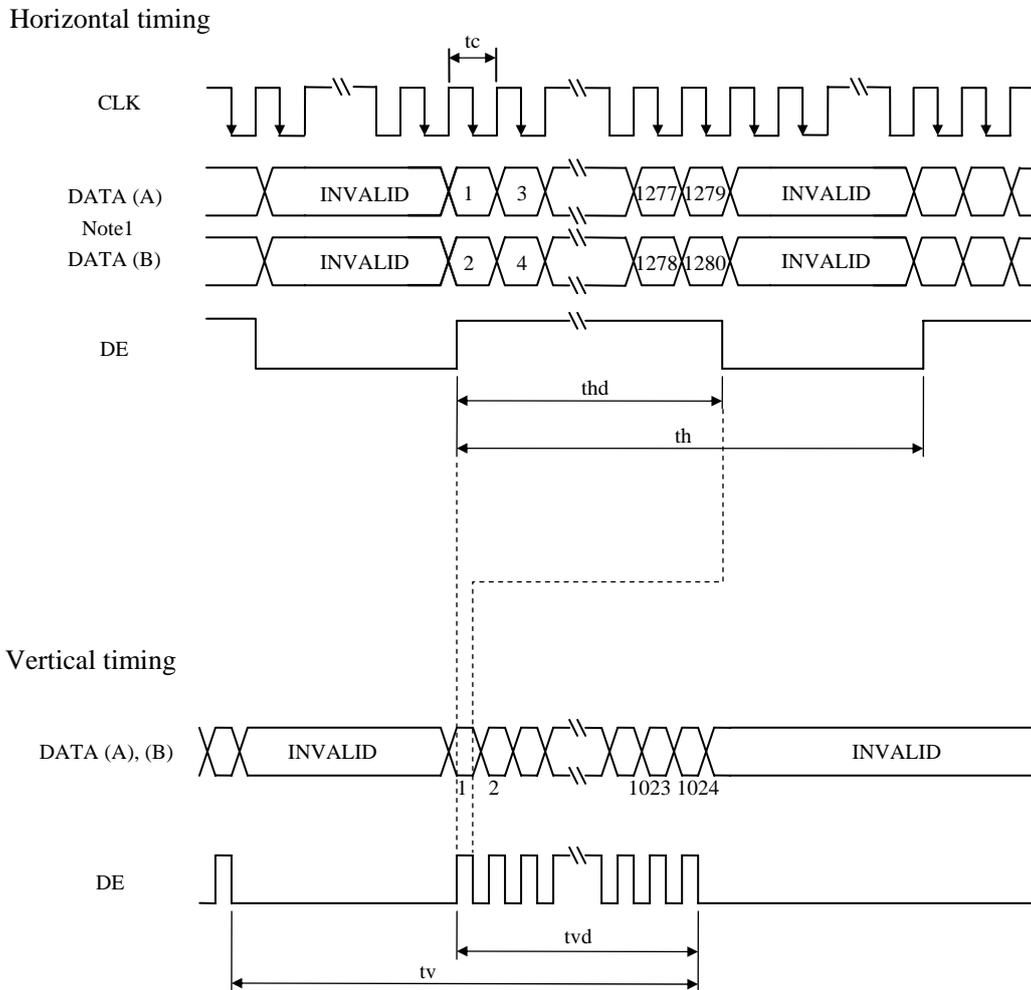
Parameter		Symbol	min.	typ.	max.	Unit	Remarks	
CLK	Frequency	1/tc	49	54	59	MHz	18.52 ns (typ.)	
	Duty	-	-			-	Note2	
	Rise time, Fall time	-	-			ns		
DATA	CLK-DATA	Setup time	-	-			ns	Note2
		Hold time	-	-			ns	
	Rise time, Fall time	-	-			ns		
DE	Horizontal	Cycl	th	12.3	15.63	20.59	μs	64.0 kHz (typ.) Note1, Note2
		Display period	thd	660	844	1,024	CLK	
	Vertical (One frame)	Cycle	tv	13.1	16.6	17.5	ms	60.0 Hz (typ.) Note1
		Display period	tvd	1,030	1,066	1,422	H	
	CLK-DE	Setup time	-	-			ns	Note2
		Hold time	-	-			ns	
Rise time, Fall time		-	-			ns		

Note1: Definition of parameters is as follows.

tc = 1CLK, th = 1H

Note2: See the data sheet of LVDS transmitter.

4.10.2 Input signal timing chart



Note1: DATA (A) = RA0-RA7, GA0-GA7, BA0-BA7
 DATA (B) = RB0-RB7, GB0-GB7, BB0-BB7

PRELIMINARY

4.11 OPTICS

4.11.1 Optical characteristics

(Note1, Note2)

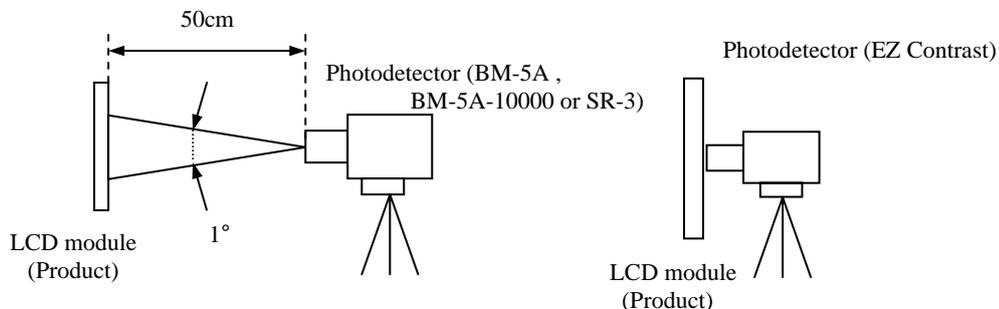
Parameter	Condition	Symbol	min.	typ.	max.	Unit	Measuring instrument	Remarks	
Luminance	White at center $\theta R = 0^\circ, \theta L = 0^\circ, \theta U = 0^\circ, \theta D = 0^\circ$	L	600	(800)	-	cd/m ²	BM5A or SR-3	-	
Contrast ratio	White/Black at center $\theta R = 0^\circ, \theta L = 0^\circ, \theta U = 0^\circ, \theta D = 0^\circ$	CR	TBD	(1000)	-	-	BM5A or SR-3	Note3	
Luminance uniformity	White $\theta R = 0^\circ, \theta L = 0^\circ, \theta U = 0^\circ, \theta D = 0^\circ$	LU	-	1.1	1.25	-	BM-5A	Note4	
Chromaticity	White	x coordinate	Wx	0.250	0.300	0.350	-	SR-3	Note5
		y coordinate	Wy	0.265	0.315	0.365	-		
	Red	x coordinate	Rx	TBD	(0.640)	TBD	-		
		y coordinate	Ry	TBD	(0.330)	TBD	-		
	Green	x coordinate	Gx	TBD	(0.300)	TBD	-		
		y coordinate	Gy	TBD	(0.620)	TBD	-		
Blue	x coordinate	Bx	TBD	(0.150)	TBD	-			
	y coordinate	By	TBD	(0.060)	TBD	-			
Color gamut	$\theta R = 0^\circ, \theta L = 0^\circ, \theta U = 0^\circ, \theta D = 0^\circ$ at center, against NTSC color space	C	65	72	-	%			
Response time	Black to white	Ton	-	(14)	TBD	ms	BM-5A -10000	Note6 Note7	
	White to black	Toff	-	(11)	TBD	ms			
	Ton + Toff	-	-	25	40	ms			
Viewing angle	Right	$\theta U = 0^\circ, \theta D = 0^\circ, CR \geq 10$	θR	70	88	-	BM-5A, EZ Contrast	Note8	
	Left	$\theta U = 0^\circ, \theta D = 0^\circ, CR \geq 10$	θL	70	88	-			
	Up	$\theta R = 0^\circ, \theta L = 0^\circ, CR \geq 10$	θU	70	88	-			
	Down	$\theta R = 0^\circ, \theta L = 0^\circ, CR \geq 10$	θD	70	88	-			

Note1: These are initial characteristics.

Note2: Measurement conditions are as follows.

Ta = 25°C, VDD = 5.0V, VDDB = 12.0V, At the maximum luminance control,
Display mode: SXGA, Horizontal cycle = 1/64.0kHz, Vertical cycle = 1/60.0Hz

Optical characteristics are measured after 20minutes from working the product, in the dark room. Also measurement methods are as follows.



Note3: See "4.11.2 Definition of contrast ratio".

Note4: See "4.11.3 Definition of luminance uniformity".

Note5: These coordinates are found on CIE 1931 chromaticity diagram.

Note6: Product surface temperature: TopF = (35)°C

Note7: See "4.11.4 Definition of response times".

Note8: See "4.11.5 Definition of viewing angles".

4.11.2 Definition of contrast ratio

The contrast ratio is calculated by using the following formula.

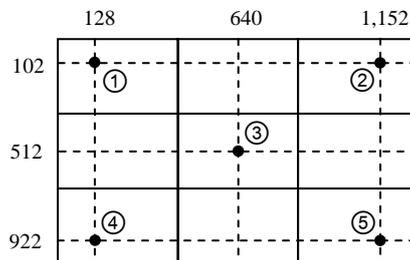
$$\text{Contrast ratio (CR)} = \frac{\text{Luminance of white screen}}{\text{Luminance of black screen}}$$

4.11.3 Definition of luminance uniformity

The luminance uniformity is calculated by using following formula.

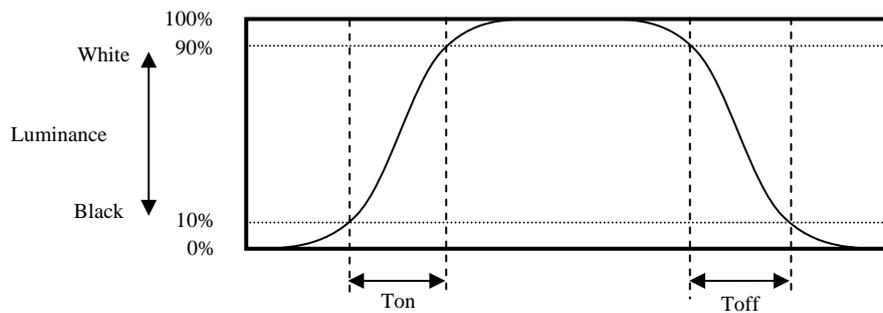
$$\text{Luminance uniformity (LU)} = \frac{\text{Maximum luminance from ① to ⑤}}{\text{Minimum luminance from ① to ⑤}}$$

The luminance is measured at near the 5 points shown below.

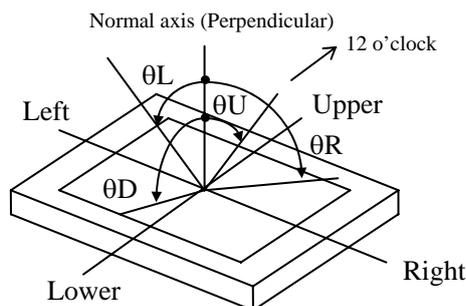


4.11.4 Definition of response times

Response time is measured, the luminance changes from "black" to "white", or "white" to "black" on the same screen point, by photo-detector. Ton is the time it takes the luminance change from 10% up to 90%. Also Toff is the time it takes the luminance change from 90% down to 10% (See the following diagram.).



4.11.5 Definition of viewing angles



5. ESTIMATED LUMINANCE LIFETIME

The luminance lifetime is the time from initial luminance to half-luminance.

This lifetime is the estimated value, and is not guarantee value.

Condition		Estimated luminance lifetime (Life time expectancy) Note1, Note2, Note3	Unit
LED elementary substance	25°C (Ambient temperature of the product) Continuous operation, PWM: Duty 100%	70,000	h

Note1: Life time expectancy is mean time to half-luminance.

Note2: Estimated luminance lifetime is not the value for an LCD module but the value for LED elementary substance.

Note3: By ambient temperature, the lifetime changes particularly. Especially, in case the product works under high temperature environment, the lifetime becomes short.

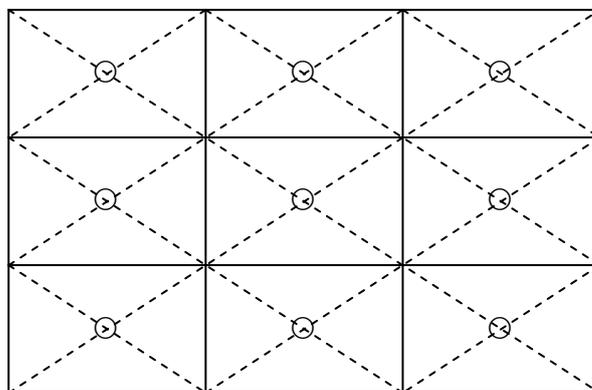
PRELIMINARY

6. RELIABILITY TESTS

Test item	Condition	Judgment	Note1
High temperature and humidity (Operation)	① $60 \pm 2^{\circ}\text{C}$, RH = 90%, 240hours ② Display data is white.	No display malfunctions	
Heat cycle (Operation)	① $-20 \pm 3^{\circ}\text{C}$...1hour $70 \pm 3^{\circ}\text{C}$...1hour ② 50cycles, 4hours/cycle ③ Display data is white.		
Thermal shock (Non operation)	① $-30 \pm 3^{\circ}\text{C}$...30minutes $80 \pm 3^{\circ}\text{C}$...30minutes ② 100cycles, 1hour/cycle ③ Temperature transition time is within 5 minutes.		
Vibration (Non operation)	① 5 to 100Hz, 11.76m/s^2 ② 1 minute/cycle ③ X, Y, Z directions ④ 10 times each directions	No display malfunctions No physical damages	
Mechanical shock (Non operation)	① 294m/s^2 , 11ms ② X, Y, Z directions ③ 3 times each directions		
ESD (Operation)	① 150pF, 150Ω , $\pm 15\text{kV}$ ② 9 places on a panel surface Note2 ③ 10 times each places at 1 sec interval	No display malfunctions	
Dust (Operation)	① Sample dust: No.15 (by JIS-Z8901) ② 15 seconds stir ③ 8 times repeat at 1 hour interval		
Low pressure	Non-operation		
	Operation	① 53.3 kPa ② $-20^{\circ}\text{C} \pm 3^{\circ}\text{C}$...24 hours ③ $70^{\circ}\text{C} \pm 3^{\circ}\text{C}$...24 hours	

Note1: Display functions are checked under the same conditions as product inspection.

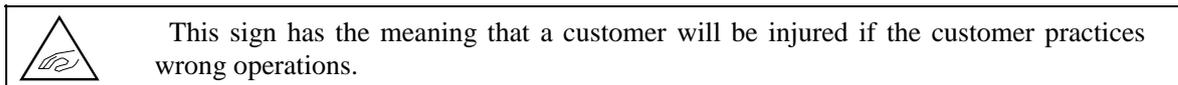
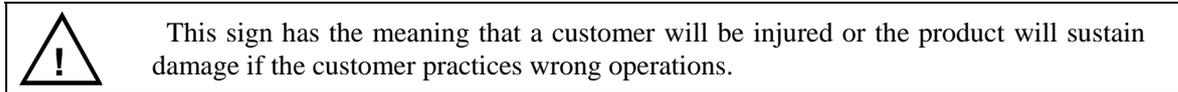
Note2: See the following figure for discharge points



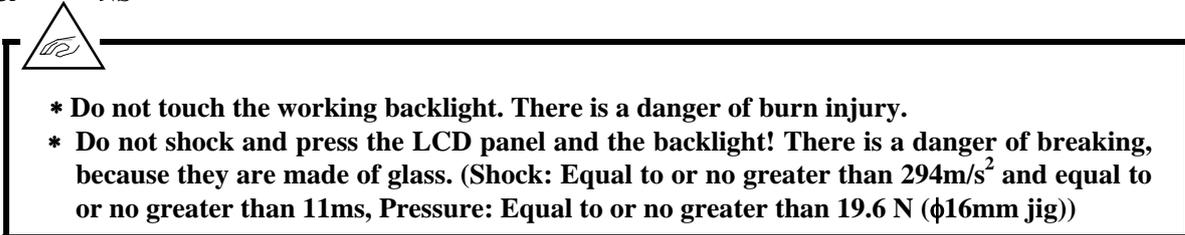
7. PRECAUTIONS

7.1 MEANING OF CAUTION SIGNS

The following caution signs have very important meaning. **Be sure to read "7.2 CAUTIONS" and "7.3 ATTENTIONS"!**



7.2 CAUTIONS



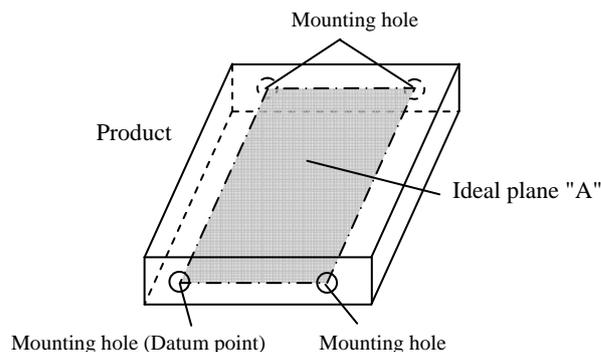
2

7.3 ATTENTIONS



7.3.1 Handling of the product

- ① Take hold of both ends without touching the circuit board when the product (LCD module) is picked up from inner packing box to avoid broken down or misadjustment, because of stress to mounting parts on the circuit board.
- ② When the product is put on the table temporarily, display surface must be placed downward.
- ③ When handling the product, take the measures of electrostatic discharge with such as earth band, ionic shower and so on, because the product may be damaged by electrostatic.
- ④ The torque for product mounting screws must never exceed 0.67N·m. Higher torque might result in distortion of the bezel. And the length of product mounting screws from surface of plate (product side) must be ≤ TBD mm
- ⑤ The product must be installed using mounting holes without undue stress such as bends or twist (See outline drawings). And do not add undue stress to any portion (such as bezel flat area). Bends or twist described above and undue stress to any portion may cause display mura.
 Recommended installing method: Ideal plane "A" is defined by one mounting hole (datum point) and other mounting holes. The ideal plane "A" should be the same plane within ±0.3 mm.



- ⑥ Do not press or rub on the sensitive product surface. When cleaning the product surface, wipe it with a soft dry cloth.
- ⑦ Do not push or pull the interface connectors while the product is working.
- ⑧ When handling the product, use of an original protection sheet on the product surface (polarizer) is recommended for protection of product surface. Adhesive type protection sheet may change color or characteristics of the polarizer.
Usually liquid crystals don't leak through the breakage of glasses because of the surface tension of thin layer and the construction of LCD panel. But, if you contact with liquid crystal by any chance, please wash it away with soap and water.

7.3.2 Environment

- ① Do not operate or store in high temperature, high humidity, dewdrop atmosphere or corrosive gases. Keep the product in packing box with antistatic pouch in room temperature to avoid dusts and sunlight, when storing the product.
- ② In order to prevent dew condensation occurred by temperature difference, the product packing box must be opened after enough time being left under the environment of an unpacking room. Evaluate the storage time sufficiently because dew condensation is affected by the environmental temperature and humidity. (Recommended leaving time: 6 hours or more with the original packing state after a customer receives the package)
- ③ Do not operate in high magnetic field. If not, circuit boards may be broken.
- ④ This product is not designed as radiation hardened.

7.3.3 Characteristics

The following items are neither defects nor failures.

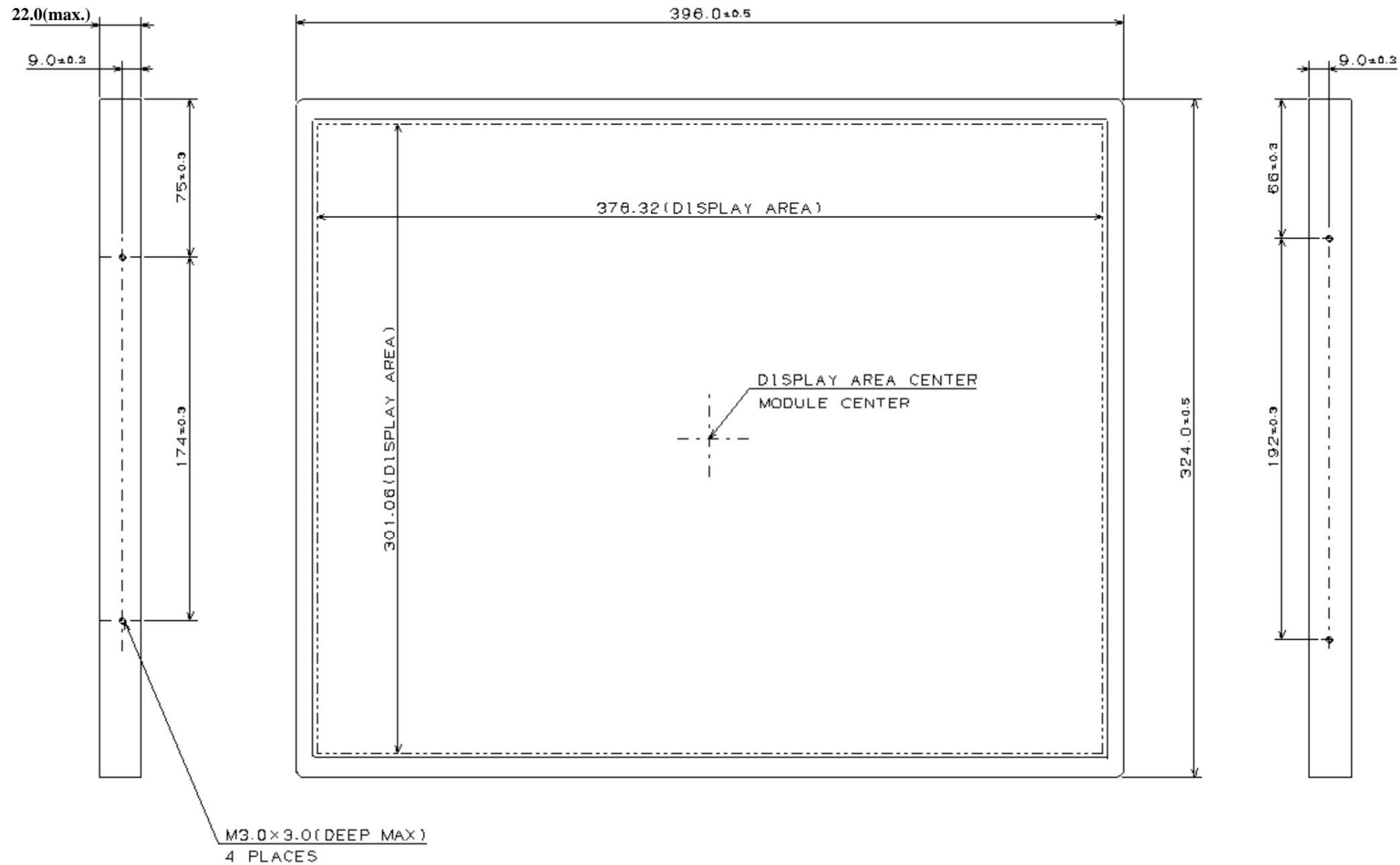
- ① Response time, luminance and color may be changed by ambient temperature.
- ② Display mura, flickering, vertical streams or tiny spots may be observed depending on display patterns.
- ③ Optical characteristics (e.g. luminance, display uniformity, etc.) gradually is going to change depending on operating time, and especially low temperature, because the LCD has cold cathode fluorescent lamps.
- ④ Do not display the fixed pattern for a long time because it may cause image sticking. Use a screen saver, if the fixed pattern is displayed on the screen.
- ⑤ The display color may be changed depending on viewing angle because of the use of condenser sheet in the backlight.
- ⑥ Optical characteristics may be changed depending on input signal timings.
- ⑦ The interference noise between input signal frequency for this product's signal processing board and luminance control frequency of the LED driver board may appear on a display. Set up luminance control frequency of the LED driver board so that the interference noise does not appear.

7.3.4 Others

- ① All GND, VDD, GNDB and VDDB terminals should be used without any non-connected lines.
- ② Do not disassemble a product or adjust variable resistors.
- ③ The LCD module by itself or integrated into end product should be packed and transported with display in the vertical position. Otherwise the display characteristics may be degraded.
- ④ Pack the product with the original shipping package, in order to avoid any damages during transportation, when returning the product to NLT for repairing and so on.

8. OUTLINE DRAWINGS

8.1 FRONT VIEW

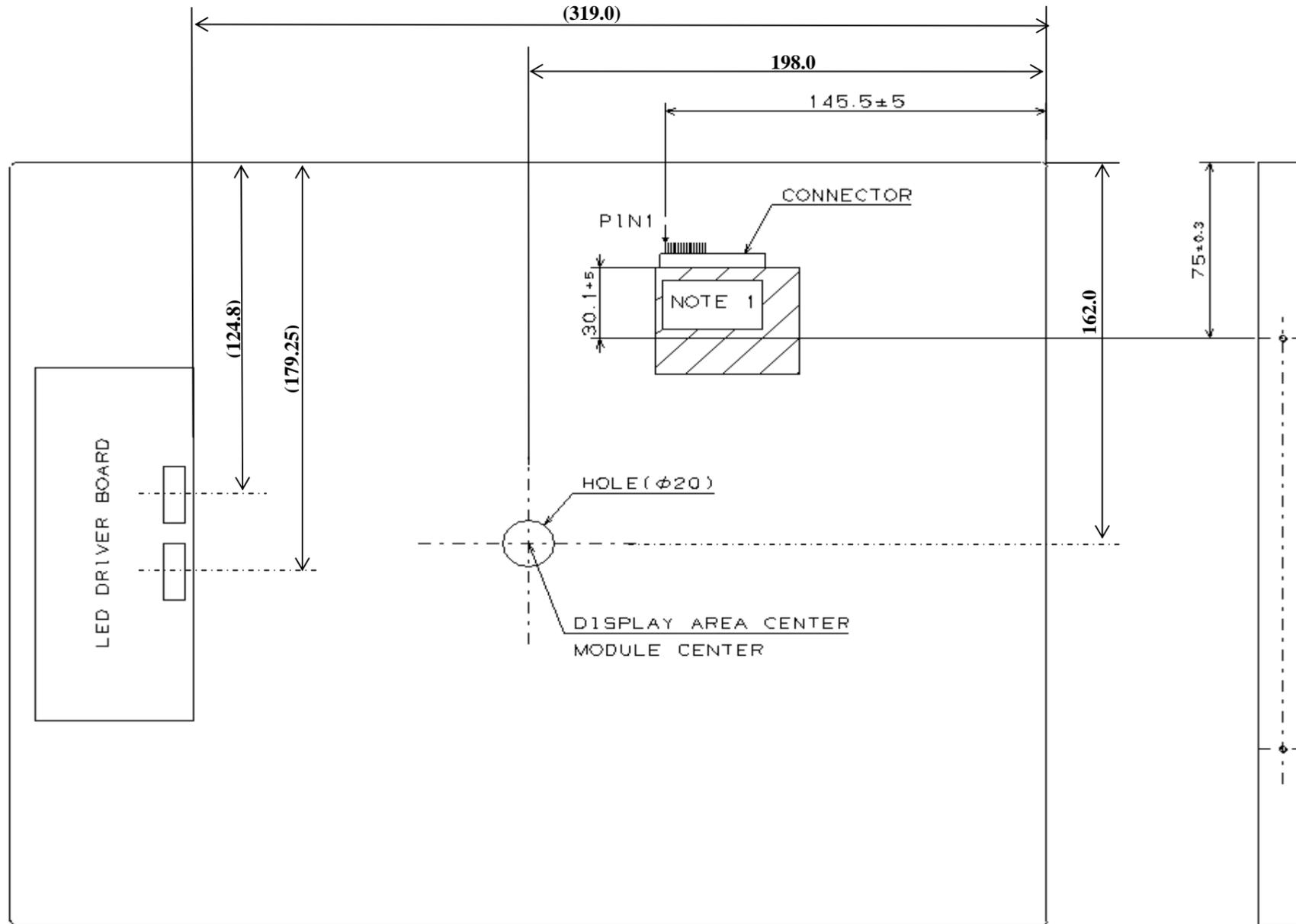


Note1: The values in parentheses are for reference.

Note2: The torque for product mounting screws must never exceed 0.67N·m.

Unit: mm

8.2 REAR VIEW



NOTE:
 1: CONNECTOR KEEP-OUT AREA 55×45MM. EDGE IS LOCATED 4MM FROM P1N 1.
 KEEP OUT AREA IS SHOWN IN CROSS-HATCH.
 2: THE TORQUE FOR PRODUCT MOUNTING SCREWS MUST NEVER EXCEED 0.67N·m.

Unit: mm

